A 0.6V Highly Linear Switched-R-MOSFET-C Filter

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***Abstract*— The design and performance of a switched-R-MOSFET-C filter is presented in this paper. The filter achieves -77dB THD using a 0.6V supply, and -90dB THD using a 0.8V supply, with a 0.6Vpp differential 2kHz sine input. High linearity at a low supply voltage is achieved by the use of duty-cycle controlled tuning inside a feedback loop.**

I. Introduction

The continuous downscaling of transistor dimensions in CMOS technology has enabled digital IC systems to achieve increasingly higher speed and integration density. An important aspect of this downscaling trend is that supply voltages must be decreased along with transistor dimensions. While digital circuits benefit from supply voltage scaling with lower power dissipation, the design of low-voltage analog circuits that must co-exist with digital circuits pose many difficult challenges.

Analog filters are key building blocks in many systems. Like many other analog circuits, traditional filters are adversely affected by a low supply voltage. One of the most fundamental low-voltage issues in analog design is reduction in available signal swing. To achieve the same dynamic range as their high-voltage counterparts, low-voltage circuits must achieve better noise and distortion performance. This is difficult because low-voltage operation exacerbates the non-linearity leading to poor distortion.

Conventional switched-capacitor (SC) filters have difficulty working at low supply voltages because of the floating switch in the signal path. The fundamental limitation of a complementary floating switch in a SC branch occurs when the supply voltage becomes less than or equal to the sum of the absolute values of the pMOS and nMOS threshold voltages. In modern processes this limit is being reached because the threshold voltages are not scaled as aggressively as the supply voltage to avoid excess leakage current. The use of a bootstrapped clock may be used to solve this problem, but it may incur reliability issues [1].

Continuous-time (CT) filters are also strongly affected by a low supply voltage. One of the most critical issues in integrated CT filters is the corner frequency variation caused by variations in process, voltage and temperature (PVT). Both resistor and capacitor values can vary by as much as 25% in modern CMOS processes, which can cause a corner frequency variation of up to 50%. To suppress this time-constant variation, voltage-controlled tunable elements such as MOS resistors or MOS capacitors are used. Problems occur when the supply voltage is lowered because the tuning range of the voltage-controlled elements is lowered as well. For low supply voltages the available tuning range may not be enough to compensate for PVT variation. A decrease in supply voltage may also cause a decrease in linearity if a MOS resistor operating in the triode region is used as the tunable element.

In order to circumvent these low voltage issues the switched-R-MOSFET-C (SRMC) filter has been developed. Several previous works have shown the use of variable timing to adjust circuit time-constants [2][3]. The SRMC filter architecture uses duty-cycle based tuning as a means to achieve accurate time-constants while maintaining high linearity at low supply voltages. This work describes the IC implementation and measurement results of an SRMC filter. Section II describes the SRMC filter architecture, Section III gives details of the circuit design, Section IV discusses modulation effects, and finally Section V presents measurement results of the fabricated IC.

II. System Architecture

The SRMC filter architecture [4] uses the MOSFET as a switch instead of a voltage controlled resistor as is done in continuous-time filters. This MOSFET switch, with on-resistance R_{on}, is put in series with a resistor R to form an R-MOSFET branch. A duty-cycle controlled clock is applied to the MOSFET gate to control the *average* resistance of the R-MOSFET branch. The average equivalent resistance of a duty-cycle controlled R-MOSFET branch is given by:

$$R_{eq} = \frac{R + R_{on}}{d} \cong R/d \quad for \quad R_{on} \ll R. \tag{1}$$

where d is the duty-cycle of the applied clock and is defined as the ratio of on-time to clock period. Because tuning is done in time rather than in voltage, the tuning range is not compromised by a low supply.

To obtain an ideal SRMC filter, the resistors in a conventional active RC filter are replaced by the switched R-MOSFET branches (Fig. 1). The same duty-cycle controlled clock ϕ is applied to both switches such that the resistances of the R-MOSFET branches are controlled concurrently. By keeping the resistances of the R-MOSFET branches equal, tuning only affects the cutoff frequency of the filter but not the gain. The 3dB cutoff frequency of the first-order SRMC filter is given by:

$$\omega_{cutoff} = \frac{1}{R_{eq}C} \cong \frac{d}{RC} \tag{2}$$

Because switches S_1 and S_2 operate with the same clock and connect to the same node, they can be combined into one switch. The complete first-order SRMC filter structure is shown in Fig. 2 with MOSFET M_1 being the combined

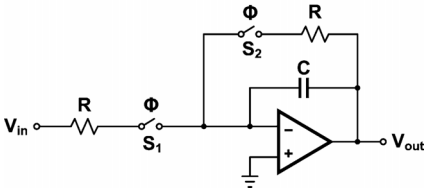

Fig. 1. Ideal first-order SRMC filter.

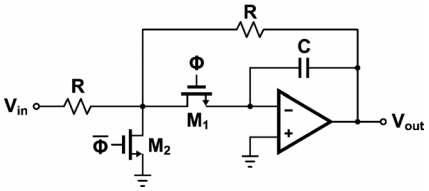

Fig. 2. Complete first-order SRMC filter.

switch. An additional switch M_2 is added which is driven with a complementary clock $\bar{\phi}$. The purpose of this switch is to steer current to ground while M_1 is off such that the current loading through the resistor branches is consistent over both clock phases. This also helps to minimize signal feedthrough while M_1 is off. For M_2 to work properly despite changes in the duty-cycle of ϕ, the complementary clock $\bar{\phi}$ must have a duty-cycle of $1 - d$.

The SRMC structure allows it to operate with high linearity. When M_1 is conducting, its on resistance is much smaller than the branch resistors R. By having the branch resistors in series with the hold transistor M_1, linearity is improved because most of the voltage is dropped across the linear resistors. Including M_1 in the feedback loop further reduces its distortion and increases the filter linearity [5].

The SRMC filter is tuned using a master-slave tuning scheme (Fig. 3). The slave is the SRMC filter. The master contains an R-MOSFET resistor/capacitor set similar to those used in the SRMC filter. A feedback loop, created using the duty-cycle controlled clock ϕ, adjusts the resistance of the R-MOSFET branch in the master such that the R-MOSFET resistor capacitor time constant is equal to a reference time period T_{ref}. This reference time period is the period of an accurate reference clock ϕ_{ref}. Because the duty-cycle controlled clock ϕ is also applied to the slave (SRMC filter), the filter will have time constants proportional to T_{ref}.

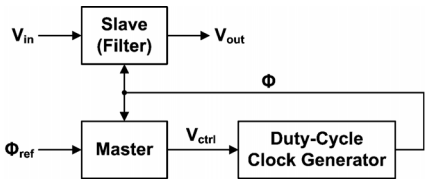

Fig. 3. SRMC master-slave tuning.

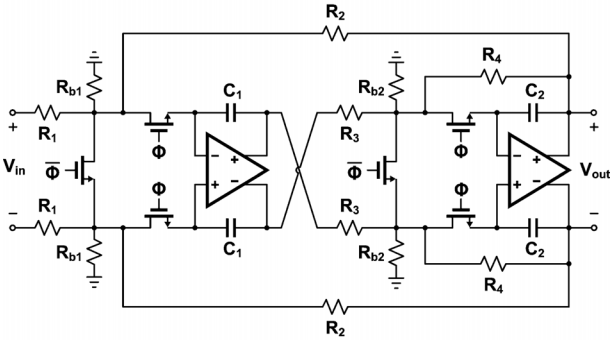

Fig. 4. SRMC biquad filter.

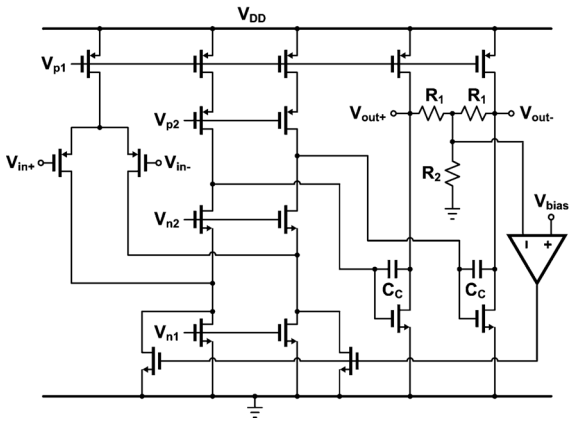

Fig. 5. Filter opamp.

III. Circuit Design

A. Biquad

A 2^{nd}-order Butterworth low-pass filter was designed to test the performance of the SRMC structure under low supply voltages. The SRMC filter was implemented in a biquad form shown in Fig. 4. The biquad is developed using the same methodology as in Section II for the first-order filter. Additional resistors R_{b1} and R_{b2} have been added to bias the inputs of the differential opamps near ground. This allows the opamps with pMOS input pairs to work with a low supply voltage [6]. This also enables the switching MOSFETs to operate with a low-voltage clock. There are no floating switches in the circuit and all terminal-to-terminal voltages are smaller than the supply voltage at all times.

B. Filter Opamp

A low-voltage differential opamp was designed using a 2-stage folded cascode structure (Fig. 5). Cascoding in the first stage is possible because the available output signal swing is reduced by the gain of the second stage. The common-mode feedback circuit is a single stage folded cascode opamp with pMOS inputs. The input pair is biased near ground with a resistive voltage divider made up of R_2 and common mode sense resistors R_1. This biasing is similar to that of the main opamp and allows low-voltage operation.

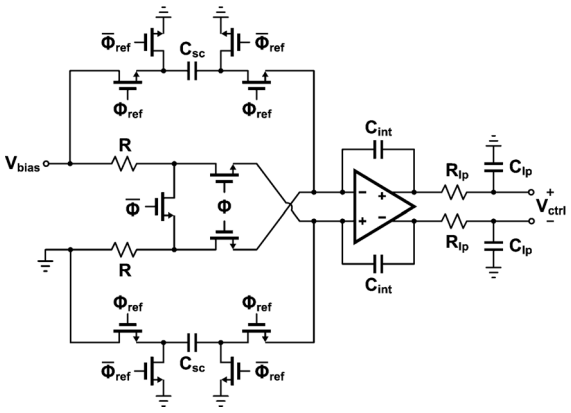

Fig. 6. Master circuit.

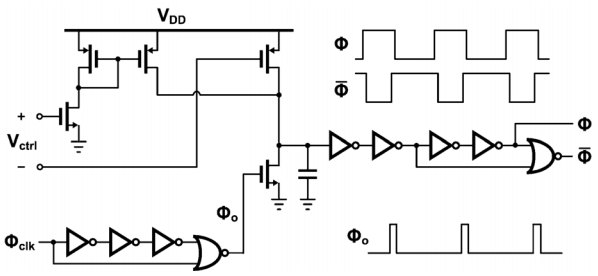

Fig. 7. Duty-cycle clock generator circuit.

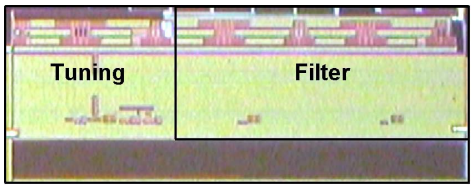

Fig. 8. Die micrograph.

C. Master Stage

Fig. 6 shows the master tuning circuit. Tuning is performed with a differential structure to suppress charge injection and clock modulation. Considering one side of the differential structure, two branches feed into the input of an integrator. The outer branch is a SC resistor with resistance T_{ref}/C_{sc}, where T_{ref} is the period of clock ϕ_{ref}. The inner branch is an R-MOSFET resistor with resistance R/d, where d is the duty-cycle of clock ϕ. Any mismatch between the resistance of these branches causes current to flow into the integrator and the control voltage V_{ctrl} to change. The negative feedback loop controls the duty-cycle of ϕ and adjusts the resistance of the R-MOSFET branch forcing it to be equal to the resistance of the SC branch. Once the feedback loop reaches equilibrium, the resistance of the the branches will be equal. Equating branch resistances gives:

$$T_{ref} = C_{sc}R_{eq} \cong \frac{C_{sc}R}{d}. \tag{3}$$

Equation (3) shows that the time constant $C_{sc}R_{eq}$ can be set precisely if an accurate reference clock is used for ϕ_{ref}. R and C_{sc} are made up of the same unit elements as the resistors and capacitors used in the filter, and therefore the time-constants between the master and slave will track with process and temperature variation. The time constants in the filter can be set as accurately as the matching between the master and slave allows. Note that V_{bias} is set to a low voltage ($\sim$100mV) so there are no floating switches in the circuit.

D. Duty-cycle Clock Generator

The duty-cycle clock generator is shown in Fig. 7. The control voltage V_{ctrl} adjusts the charging of a capacitor via a transconductance stage that was designed to operate at low voltages. An inverter triggers when the capacitor has been charged to approximately $V_{DD}/2$. Depending on the amount of current provided to the capacitor, the time until the inverter triggers can be changed, thereby adjusting the duty-cycle. A large grounding transistor discharges the capacitor at the end of each clock cycle. The clock ϕ_o applied to this transistor defines the minimum duty-cycle of ϕ.

IV. Modulation Effects

In the SRMC architecture, modulation of the input signal occurs similar to that which takes place in a mixer. The input is modulated by the clock, and replicas appear at multiples of the clock frequency with conversion gain determined by the Fourier series components of the clock waveform. Assuming that the clock frequency ω_{clk} is more than twice the filter cutoff frequency ω_{cutoff}, the first-order filter output signal is given by:

$$V_{out}(\omega) \cong \frac{-\sum_{n=-\infty}^{\infty} sinc(nd) \cdot V_{in}(\omega - n\omega_{clk})}{1 + j\omega\frac{RC}{d}} \tag{4}$$

where $V_{in}(\omega)$ is the input signal. Equation (4) shows that modulation occurs before filtering, therefore an anti-aliasing filter is required. Unlike SC filters, the SRMC filter has no opamp/capacitor settling time requirements. The clock frequency can be set arbitrarily high, limited only by the ability of the switching transistors to turn on for a minimum duty-cycle. By making the clock frequency high, the requirements on the anti-aliasing filter are greatly reduced compared to a SC filter.

V. Experimental Results

The prototype IC was fabricated in a 0.18μm CMOS technology. The die micrograph is shown in Fig. 8. The active die area is 0.5×1.4 mm^2. Fig. 9 shows the measured THD of the filter over an input frequency range of 2kHz to 100kHz for 0.6V and 0.8V supply voltages. The input sinusoid was held at 0.6Vpp differential in both cases. The measured filter response over a tuning range of $\pm$50% is shown in Fig. 10. The measured -3dB cutoff frequency has a standard deviation within 5%. Figs. 11 and 12 show the output spectrum at 0.6V and 0.8V supplies with a 0.6Vpp 2kHz input signal. The

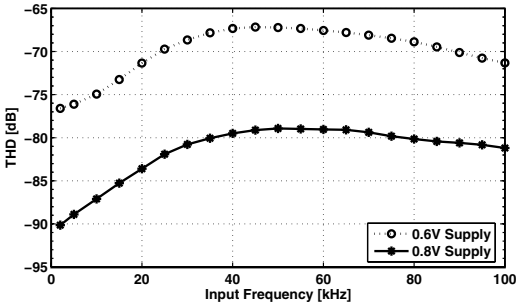

Fig. 9. Measured harmonic distortion.

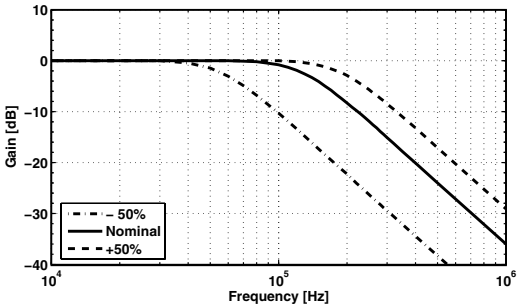

Fig. 10. Measured filter response over a ±50% tuning range.

performance summary of the filter is presented in Table I. This prototype achieves -77dB THD and 64dB SNR with a 0.6V supply voltage and 0.6Vpp differential 2kHz sine input. Noise is integrated from 1kHz to 200kHz. With a 0.8V supply the THD can be as low as -90dB. The filter can operate down to 0.5V supply with some performance degradation. The circuit power consumption is 1mW at 0.6V.

VI. Conclusion

The SRMC filter architecture allows for highly linear operation at low supply voltages through the use of duty-cycle based tuning inside a feedback loop. Because the tuning MOSFET is switched completely on when it is conducting, its non-linear resistance is much lower than that of the linear filter resistors. Most of the voltage drop occurs across the linear resistors. Including the tuning MOSFET into the filter feedback further decreases the distortion. Because tuning is done in the time domain rather than the voltage domain, the tuning range is not compromised by a low supply voltage.

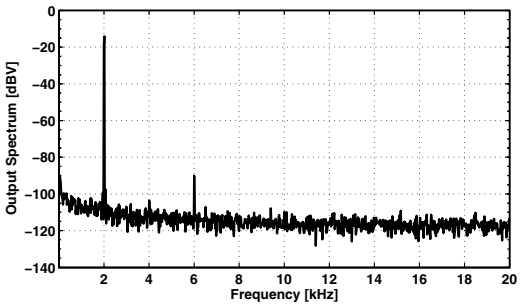

Fig. 11. Measured output spectrum at 0.6V with 0.6Vpp 2kHz input.

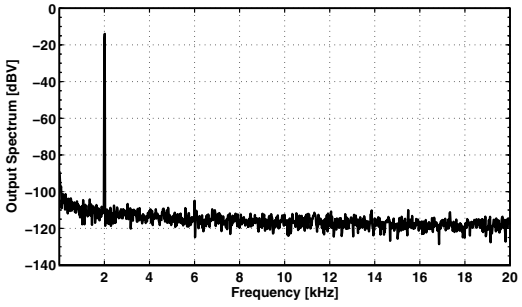

Fig. 12. Measured output spectrum at 0.8V with 0.6Vpp 2kHz input.

TABLE I
Performance Summary

Supply voltage	0.6V (0.8V)
THD Vin = 0.6Vpp diff. @ 2-kHz	-77dB (-90dB at 0.8V)
IIP3	20dBV (27dBV at 0.8V)
SNR Vin = 0.6Vpp diff.	64dB
Power consumption	1mW
Filter type	2^{nd}order Butterworth
Cutoff frequency	135-kHz
Die area	0.5×1.4 mm^2
Technology	0.18μm CMOS

Acknowledgment

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References

[1] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio $\Delta\Sigma$ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, pp. 349-355, March 2001.

[2] J. A. Kaehler, "Periodic-switched filter networks - A means of amplifying and varying transfer functions," *IEEE J. Solid-State Circuits*, vol. SC-4, pp. 225-230, August 1969.

[3] Y. Tsividis, "Signal processors with transfer function coefficients determined by timing," *IEEE Transactions on Circuits and Systems*, vol. CAS-29, no. 12, pp. 807-817, December 1982.

[4] S. Xiao, J. Silva, U. Moon and G. Temes, "A tunable duty-cycle-controlled switched-R-MOSFET-C CMOS filter for low-voltage and high-linearity applications," in *Proceedings of the 2004 International Symposium on Circuits and Systems*, 2004, pp. I-433-I-436.

[5] U. Moon and B. Song, "Design of a low-distortion 22-kHz fifth-order bessel filter," *IEEE J. Solid-State Circuits*, vol. 28, no. 12, pp. 1254-1264, December 1993.

[6] S. Karthikeyan, S. Mortezapour, A. Tammineedi and E. K. F. Lee, "Low-voltage analog circuit design based on biased inverting opamp configuration," *IEEE Transactions on Circuits and Systems II*, vol. CAS-47, no. 3, pp. 176-184, March 2000.