Low-Power and High-Speed Pipelined ADC Using Time-Aligned CDS Technique

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ABSTRACT—**Time-aligned Correlated Double Sampling (CDS) technique, which overcomes the error accumulation problem found in the time-shifted CDS technique [4], is proposed. This technique allows low gain opamp based switched-capacitor operation to achieve the equivalent accuracy that is traditionally possible only in high gain opamp based switched-capacitor operation. This allows simple single stage opamps to be used, leading to low-power and high-speed performance. As a proof of concept, a prototype pipelined analog-to-digital converter (ADC) is fabricated in a 0.18μm CMOS process. Measured results demonstrate 1.8V 10b 100MS/s 50mW ADC.**

I. Introduction

The switched-capacitor pipelined analog-to-digital converter (ADC) is considered suitable for low-power and high-speed applications [1]. The capacitor matching and finite opamp gain, however, limit the resolution of a pipelined ADC. As the CMOS process advances, producing better-matched capacitors is becoming easier, but because of the decreasing supply voltage, designing high-gain and high-bandwidth opamps is becoming more difficult, as cascoding of devices limits output signal swing. Many techniques have been proposed to alleviate the low gain opamp issue. Digital calibration is an attractive approach but it requires a significant digital circuit complexity, and even more so for background calibration [2]. A traditional correlated double sampling (CDS) technique would effectively square (double in dB) the opamp gain, but it needs a three-phase operation, which directly limits the conversion speed [3]. In order to operate CDS with two phases, the time-shifted CDS was proposed in [4]. The time-shifted CDS, however, transfers predicted/estimated residue in place of the true sampled value to the sub/flash ADC, and the process continues down the pipeline for all sub/flash ADC operation. Therefore, the prediction error accumulates as the information is transferred from one stage to the next stage. In this paper, we propose time-*aligned* CDS technique to prevent this accumulation of prediction error. With the time-aligned CDS technique, input sample-and-hold (S/H) stage can also be eliminated to save power, which is becoming a common trend in pipelined ADCs [5]. Additional effort is made to reduce power consumption by scaling capacitors and opamps down the pipeline.

II. Time-Aligned CDS Technique

A typical switched capacitor 1.5bit multiplying digital-to-analog converter (MDAC) operation is shown in Fig. 1. Input signal is sampled during ϕ_1 and amplified/transferred during ϕ_2 to the next stage. The output value is

$$V_{out} = (\frac{C_S + C_F}{C_F})V_{in} - \frac{C_S}{C_F}\{0, \pm V_{ref}\} - \frac{1}{A}(\frac{C_S + C_F}{C_F})V_{out}, \quad (1)$$

where A is the finite opamp gain and one value of $\{0, \pm V_{ref}\}$ is determined by two comparators [1]. The last term is an error term that results due to the finite opamp gain.

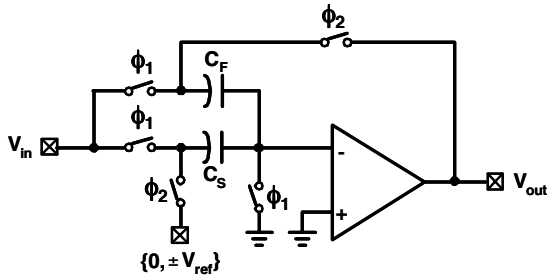

Fig. 1. Typical 1.5bit MDAC operation.

To alleviate the finite gain problem of an opamp, CDS technique was proposed, which can ideally square the opamp gain [3]. However, as shown in Fig. 2, a typical CDS operation needs three phases: for sampling (ϕ_1), prediction (ϕ_2), and amplification to the next stage (ϕ_3). The error value due to the finite opamp gain is stored in capacitor (C_0) in the prediction phase, and the stored value is used in the amplification phase to compensate for the finite opamp gain error.

In order to operate CDS with two phases, which directly improves conversion speed, the time-shifted CDS technique was proposed [4]. In the time-shifted CDS technique, the opamp transfers the predicted output to the next stage during prediction mode (ϕ_2 in Fig. 3) while input value is being sampled onto C_S. In the next phase (ϕ_1 in Fig. 3) the error-compensated output is transferred. In this same phase, the predicted input value from the previous stage is sampled onto C_P in preparation for the next sample. In the very first multiplying digital-to-analog converter (MDAC), the front-end S/H stage needs to provide the input signal over two phases: the first for the prediction and the second for the true input signal. This was done via a double sampled S/H operation in [4], and thus the time-shifted CDS absolutely requires the use a dedicated S/H stage. In the following stages (say 2nd stage), the predicted output from the previous stage

(now 1st stage), which appears one phase before the true output, is used as a predicted input to continue the time-shifted CDS process. Since the predicted value is used to generate the predicted output at the next stage, the prediction error accumulates down the pipeline stages.

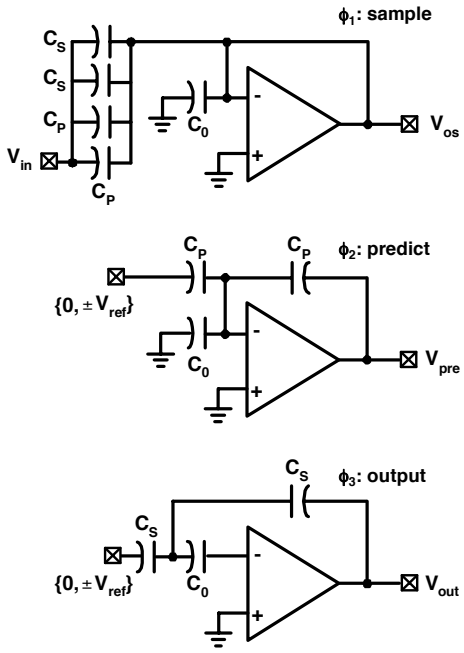

Fig. 2. Conventional CDS operation.

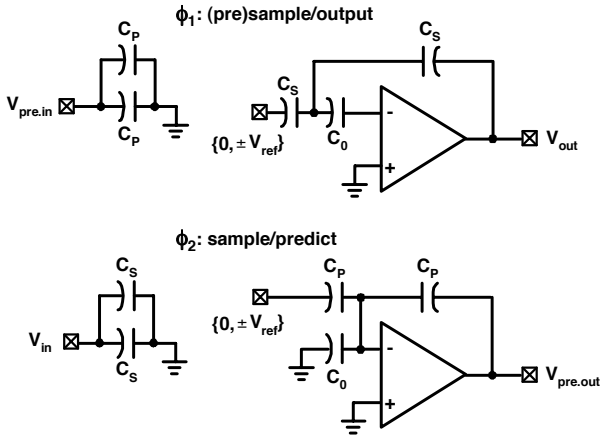

Fig. 3. Time-shifted CDS operation.

The proposed time-*aligned* CDS technique is to overcome this limitation of the time-shifted CDS. While still maintaining two-phase operation, time-aligned CDS operation is able to reset the accumulation of prediction error. Time-aligned CDS is illustrated in Fig. 4 (single-ended illustration is used for simplicity). Instead of providing the prediction signal and the true signal over two phases as in time-shifted CDS, the time-aligned CDS provides only the true signal (for use in both prediction as well as signal amplification) once during ϕ_1 onto the two sets of capacitors (C_P and $C_{A\text{ or }B}$ in Fig. 4). After the prediction in ϕ_2 (using C_P), the input signal capacitor (say C_A) is used to amplify/transfer the signal/residue to the next stage (now with improved accuracy because prediction information from the previous phase is being used). During this same phase, the other input capacitor (now C_B) samples the new input value. These two pairs of sampling capacitors ($C_{A/B}$) exchange their roles from one conversion cycle to the next. In summary, the time-aligned CDS technique has three sets of capacitors C_P, C_A and C_B. Two of them are used in each input sampling, {C_P} and {C_A or C_B}. The two sets of capacitors, C_A and C_B, are used alternately to generate the error-compensated output. This does limit the resolution due to alternating capacitor mismatch, but this is expected to be sufficient for 10bit resolution with a careful layout.

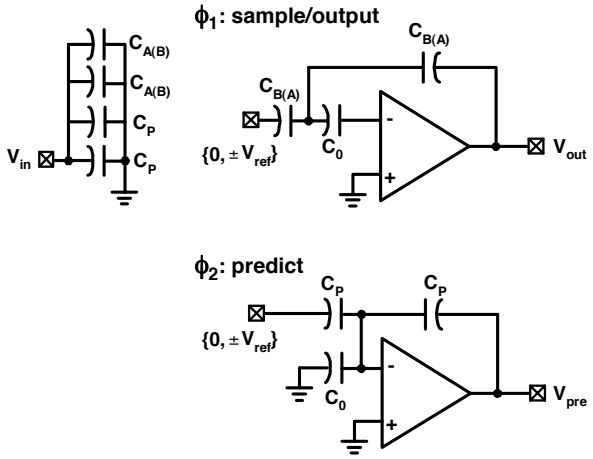

Fig. 4. Time-aligned CDS operation.

The time-aligned CDS technique is similar to opamp sharing technique [6] in that the opamp is used in all phases, during both the amplifying/transferring and the sampling phases. Since the opamp is never reset, memory effect may also limit accuracy. Once again, this was determined sufficient for 10bit resolution.

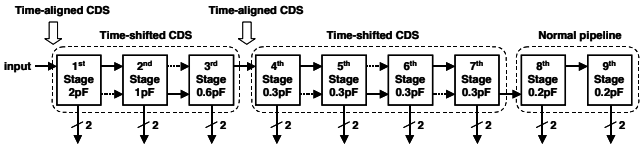

Fig. 5. Proposed pipelined ADC structure.

Shown in Fig. 5 is the proposed pipelined ADC structure and sampling capacitance values. Time-aligned/shifted CDS stages are used except in the last two stages. To reduce power, a dedicated S/H stage (which was required in time-shifted CDS) is removed and the time-aligned CDS is used in the first stage. The capacitor values of C_P, C_A, and C_B are all 2pF each. Since the two sets of capacitors are used in the time-aligned CDS, the previous stage is required to drive two times larger loading (the external signal source drives the very first stage).

To minimize this capacitive loading, time-shifted CDS (rather than time-aligned) is used in the second and the third stages. And the time-aligned operation is once again invoked in the fourth stage to reset the accumulating prediction error. Note that the predicted output is not transferred from the third to fourth stage. In view of the accumulating prediction error, which is found to be tolerable to about four stages [4], use of time-shifted CDS in the second and third stages of pipeline is deemed efficient for reducing power consumption and leaves enough room for any unanticipated prediction error. After time-aligned CDS is invoked in the fourth stage, time-shifted CDS is used down to 7th stage, before returning to standard pipelined ADC operation, where the prediction value is no longer transferred or needed.

III. Circuit Design

Shown in Fig. 6 is a simple telescopic opamp that is used in this design. Output common mode voltage is set to 1V and the single-ended signal swings from 0.65 to 1.35V, equaling 1.4Vpp differential signal swing. The advantage of using a single-stage opamp is that the transistor size of the opamp and bias current are linearly scaled with the load capacitor size, which is straightforward and attractive for low-power ADC implementation. With the bias current of 3.8mA, the simulated DC-gain is 50dB, and the simulated unity gain frequency is 1.5GHz with a 2pF load. Because our initial intent was for a higher resolution ADC, the capacitor values were over designed for the performance achieved. A proper redesign with reduced capacitor values would significantly reduce our present power consumption. Reducing the bias current and device sizes by half (and with half the size of loading capacitor), the simulated DC-gain and the unity gain frequency remained unchanged.

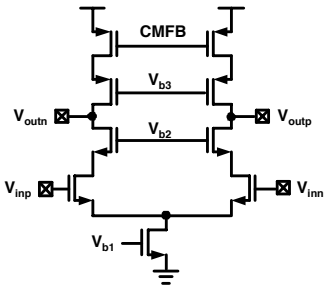

Fig. 6. Telescopic opamp.

All other circuits implemented in the prototype IC were conventional ones similar to [4], including standard two-stage preamp-latch comparators, distributed clock drivers, and standard digital error correction logic. A standard CMOS input sampling switch (optimized for size and ratio) is used.

IV. Measurement Results

The ADC was fabricated in a 0.18μm 2-poly 4-metal CMOS process. The active die size is 0.9mm x 2.2mm as shown in Fig. 7. Total power consumption is 50mW at 1.8V supply. Analog (opamps and comparators) power consumption is 36mW.

Shown in Fig. 8 is the measured differential (DNL) and integral (INL) nonlinearity plots. This was measured with 10MHz input signal and 100MHz sampling frequency. Peak DNL and INL are –0.97/+1.09 LSB and –3.437/+3.721 LSB.

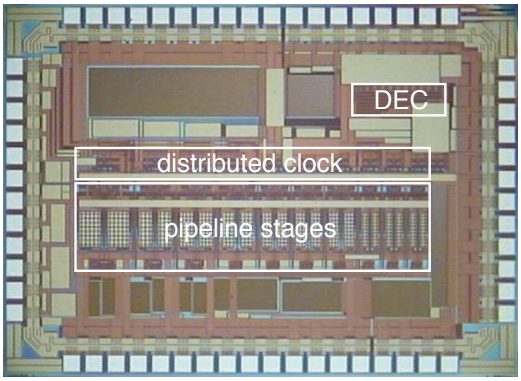

Fig. 7. Die photograph of the fabricated IC.

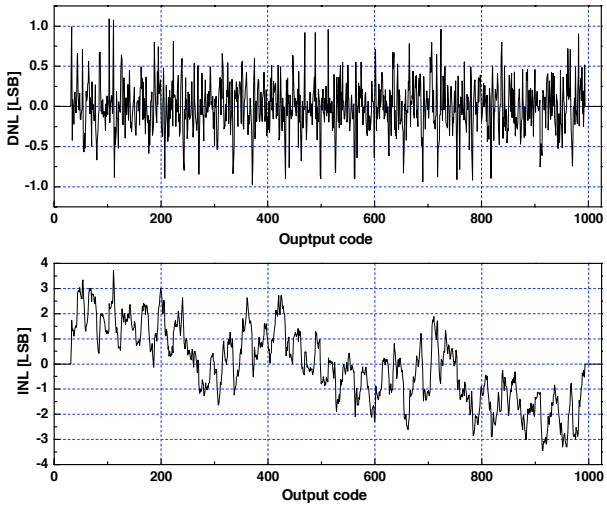

Fig. 8. Measured DNL and INL.

Shown in Figs. 9 and 10 are measured output spectrums of 1MHz and 49MHz input signals with 100MS/s sampling frequency. Digital output code is decimated/down-sampled by four on-chip (for testing purposes) right before they are brought out via the digital output buffers. At the input signal frequency of 1MHz, the measured spurious-free dynamic range (SFDR) and the measured signal-to-noise-and-distortion ratio (SNDR) are 60.6dB and 50.3dB. For 49MHz input, the measured SFDR and SNDR are 58dB and 47.6dB. The dynamic performance measured for various input signal frequencies is shown in Fig. 11. The SFDR and SNDR at the 99MHz input frequency are 56.8dB and 44.3dB. Fig. 12 shows the dynamic performance for various signal amplitudes with a 1MHz input signal.

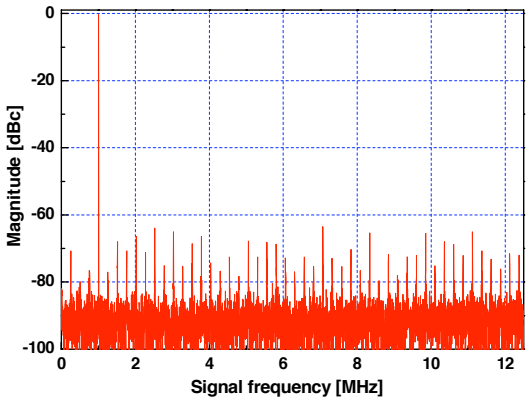

Fig. 9. Measured output spectrum (input signal frequency=1MHz).

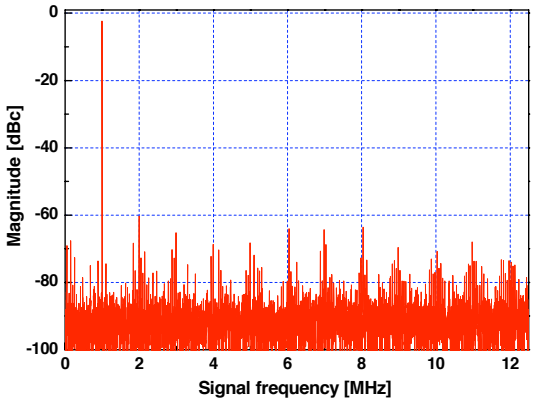

Fig. 10. Measured output spectrum (input signal frequency=49MHz).

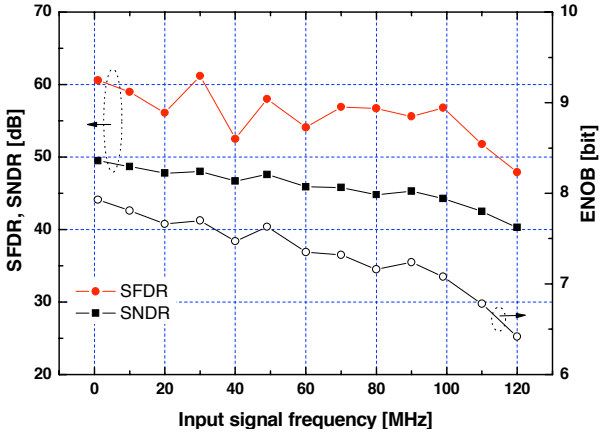

Fig. 11. Measured dynamic performance vs. input signal frequency.

V. Conclusion

A time-aligned CDS technique is proposed. The time-aligned operation alleviates accumulating prediction errors found in time-shifted operation [4]. Efficient combining of time-aligned and time-shifted operation results in the elimination of a dedicated sample-and-hold input stage and allows use of low gain opamps which enables low power and high speed operation. No additional clock phases (which are needed in conventional CDS techniques) are required in the proposed technique. The gain error typically resulting from low gain opamps is eliminated without the use of any calibration techniques. As a proof of concept, a prototype IC was fabricated. Measured results demonstrate that the above goals are achievable. There is still much room for design improvement to attain better performance and significantly lower power consumption.

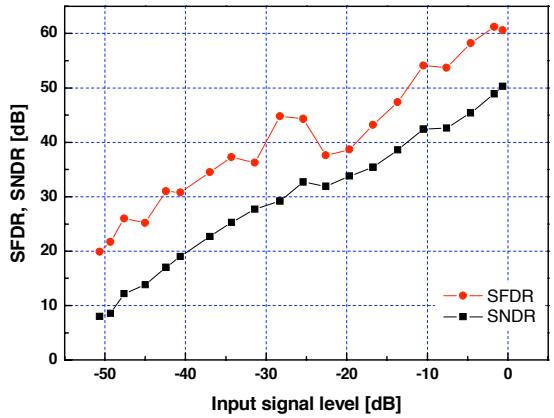

Fig. 12. Measured dynamic performance vs. input signal level.

Acknowledgments

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References

[1] S. Lewis, H. Fetterman, G. Gross, R. Pamachandran, T. Viswanathan, "A 10bit 20MS/s Analog-to-Digital Converter," *IEEE J. Solid State Circuits*, vol. 27, pp. 351-358, Mar. 1992.

[2] B. Murmann and B. Boser, "A 12bit 75MS/s Pipelined ADC Using Open-Loop Residue Amplification," *IEEE J. Solid State Circuits*, vol. 38, pp. 2040-2050, Dec. 2003.

[3] K. Nagaraj, T. Viswanathan, K. Singhal, J. Vlach, "Switched Capacitor Circuits with Reduced Sensitivity to Amplifier Gain," *IEEE Trans. Circuits and Systems*, vol. CAS-34, pp. 571-574, May 1987.

[4] J. Li and U. Moon, "A 1.8V 67mW 10bit 100MS/s Pipelined ADC Using Time-Shifted CDS Technique," *IEEE J. Solid State Circuits*, vol. 39, pp. 1468-1476, Sep. 2004.

[5] T. Nortvedt, B. Hernes, A. Briskemyr, F. Telstø, J. Bjørnsen, T. Bonnerud, Ø. Moldsvor, "A Cost-Efficient High-Speed 12bit Pipeline ADC in 0.18μm Digital CMOS," *IEEE J. Solid State Circuits*, vol. 40, pp. 1506-1513, July 2005.

[6] B. Min, P. Kim, F. Bowman, D. Boisvert, A. Aude, "A 69mW 10bit 80MSample/s Pipelined CMOS ADC," *IEEE J. Solid State Circuits*, vol. 38, pp. 2031-2039, Dec. 2003.