# LOW-VOLTAGE SWITCHED-CAPACITOR RESONATORS

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## 1. ABSTRACT

This paper presents the low-voltage (LV) implementations of two well-known switched-capacitor resonators, namely the "lossless-discrete integrator" and the "two-delay-loop" stages. Two new architectures, "integrating-two-path" and "voltage-mode pseudo-N-path" are also described.

## 2. INTRODUCTION

The recent explosion of interest in wireless personal communication systems motivates the development of fully integrated radio receivers. The parallel reduction of the feature sizes in CMOS technology, and hence higher levels of integration, enable the combined integration of a bandpass or baseband analog-to-digital converter with the traditional front-end receiver building blocks. While this trend advances the digital technology, one of the key analog limitations of state-of-the-art submicron CMOS technologies remains the restricted power-supply voltage, limited by the low junction breakdown voltage of the high density CMOS process and by the thin gate oxide, prone to voltage stress.

There exist many resonator circuits to implement SC bandpass $\Delta\Sigma$ modulators and filters for high-frequency communication applications, such as the "lossless-discrete integrator" (LDI) and "forward-Euler" (FE) types [1], two-delay loop (TDL) [2], [5], low-pass filter [3], high-pass filter based [4] and pseudo-two-path (P2P) types [6]. The most recent ones use P2P and TDL techniques, with double sampling to increase the sampling frequency. In these previous implementations, the minimum available power supply voltage was 3 V.

In our previous work [7], we have shown the LV implementations of SC ADCs and low-pass filters based on the *unity-gain-reset* (UGR) technique. Compared to the switched-opamp technique [8], this technique is suitable for operating at higher speeds, by keeping the opamp in its active operating region at all times.

In this paper, we present four different LV resonator circuits, which are functional with supply voltages down to 1 V. They are compared based on their robustness with respect to the finite gain and bandwidth of the opamps used. SWITCAP2 simulations have been performed to see the effects of the analog imperfections on their frequency responses. [1]

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[1]There are switches in dashed boxes in the figures of the following sections. These switches are conceptual switches to show the full-operation.

## 3. THE IDEAL RESONATOR TRANSFER FUNCTION

The typical resonator transfer function for a band center at $f_{clock}/4$ with unit delay from input to output is given by

$$H(z) = \frac{z^{-1}}{1+z^{-2}} \tag{1}$$

This leads to the time-domain relation

$$v_o(n) = v_{in}(n-1) - v_o(n-2) \tag{2}$$

which involves a delay by $2T$ and the inversion of $v_o(n)$.

## 4. THE LOSSLESS-DISCRETE-INTEGRATOR RESONATOR

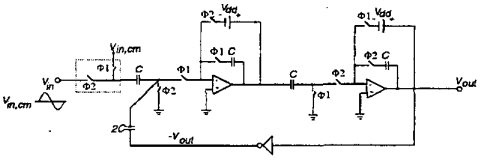


Figure 1: Single-ended low-voltage LDI resonator

The LV lossless-discrete integrator (LDI) resonator which can be implemented with two cascaded half-delay integrator in a positive feedback loop is shown in Fig. 1.

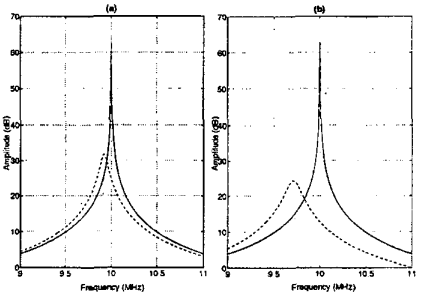


Figure 2: Simulation results of the LDI type resonator from SWITCAP2 with $f_{clock}$=40 MHz (a) for different opamp DC gains: $A_{dc}$=120 dB (solid), 50 dB (dashed); (b) for different opamp bandwidths: $f_u = \infty$ (solid), $f_u$=160 MHz (dashed).

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The circuit is shown in single-ended configuration for illustration purpose only; in fact, it is fully- or pseudo-differential when realized.

The LV LDI type resonator was simulated in SWITCAP2 for different DC gains and bandwidths of the opamps used. Simulation results are shown for $f_{clock}$ = 40 MHz in Fig. 2.

The effects of the finite gain and bandwidth of the opamps will be severe in this resonator circuit. This resonator will not only exhibit gain error but also a shifted center frequency. The positive feedback from the output of the resonator to its input will integrate the errors due to the opamp imperfections.

## 5. THE TWO-DELAY-LOOP RESONATOR

The two-delay-loop (TDL) resonator is preferred over LDI resonator because of its relaxed settling time requirements [2], [5]. The LV TDL resonator architecture is shown in Fig. 3.

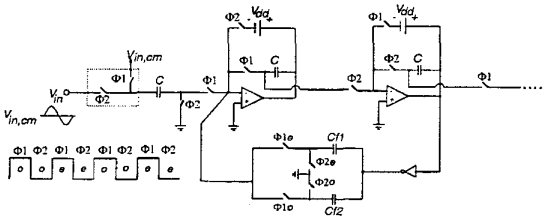

Figure 3: Single-ended low-voltage TDL resonator

In this circuit, a half-clock-cycle ($T/2$) delay is provided by the sample-and-hold (SH) circuit. Hence, a full ($T$) delay is introduced by the two cascaded SHs in the forward path. The feedback capacitors $Cf1$ and $Cf2$ keep the charge for a full clock cycle, consecutively, and hence add a full clock delay in the feedback path to insure the resonator operation.

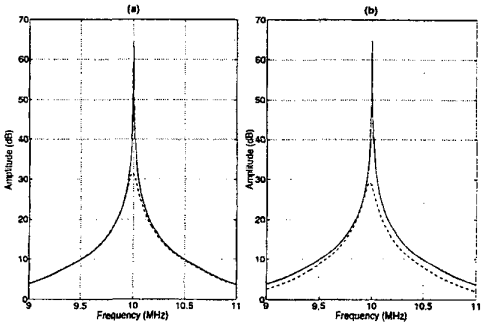

Figure 4: Simulation results of the TDL type resonator from SWITCAP2 with $f_{clock}$=40 MHz (a) for different opamp DC gains: $A_{dc}$=120 dB (solid), 50 dB (dashed); (b) for different opamp bandwidths: $f_u = \infty$ (solid), $f_u$=160 MHz (dashed).

As seen from the simulation results, the integration of the error terms are eliminated since, unlike in the LDI resonator, there is no integration at any time either at the forward or at the feedback path. Hence, there is very small shift in the center frequency location. On the other hand, the resonant gain is degraded almost by 36 dB. This configuration thus requires opamps with high DC gain.

## 6. THE INTEGRATING-TWO-PATH RESONATOR

The integrating-two-path (I2P) LV resonator architecture [10] is shown in Fig. 5. I2P is in a pseudo-differential configuration for LV operation. There are two paths from the input to the output in this scheme. The upper two opamps form the first path and one of the pseudo-differential pairs. The lower two opamps form the second path and the other pseudo-differential pair.

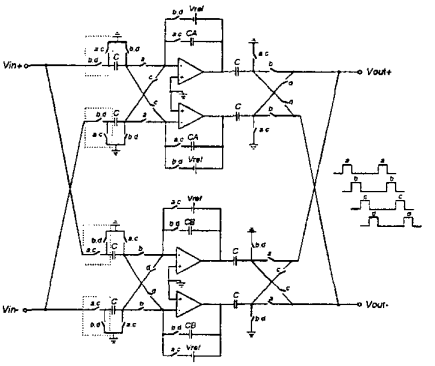

Figure 5: The low-voltage I2P resonator

The technique used for providing the two clock cycle ($2T$) delay in the previous circuits [1-6] was to apply positive feedback from the output to the input of a resonator. In all these circuits, there is charge transfer from the output to the input to realize the resonator transfer function. This charge transfer also integrates some error charges with a delay $T$. Hence, there is always a $z^{-1}$ term in the denominator of the resonator transfer functions. This creates a shift in the center frequency, with different amounts from one architecture to the other. Additionally, there was severe gain loss in some of the previous implementations.

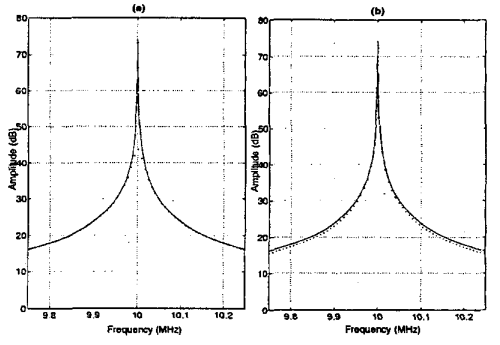

Figure 6: Simulation results of I2P type resonator from SWITCAP2 with $f_{clock}$=40 MHz (a) for different opamp DC gains: $A_{dc}$=120 dB (solid), 50 dB (dots); (b) for different opamp bandwidths: $f_u = \infty$ (solid), $f_u$=160 MHz (dots).

In this I2P structure, during odd clock phases, the differential output voltage delayed by $2T$ is stored in capacitors $CA$. Then the output of the differential pair is commutated to realize the resonator transfer function. The same operation is performed by the other pair containing $CB$ in the even clock phases.

Because of the LV operation, the commutation operation is done at both the input and the output, instead of the feedback branch [11] every two clock cycles. This will change the sign of the stored voltage on the path and hence effectively introduce positive feedback in the voltage domain.

The simulation results from SWITCAP2 are shown in Fig. 6. There is no change in the center frequency location when decreasing the DC gain or the bandwidth of the opamp. The gain at resonance peak is also much better than for the LDI and TDL resonators.

## 7. THE VOLTAGE-MODE PSEUDO-N-PATH RESONATOR

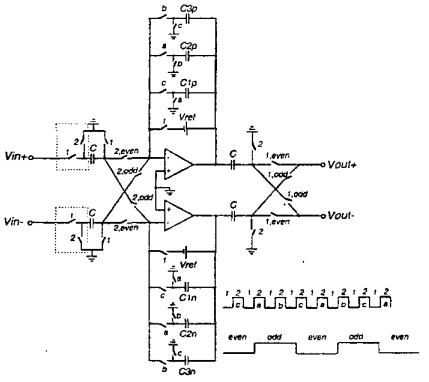


Figure 7: The low-voltage VPNP resonator

In the *voltage-mode*-pseudo-N-path (VPNP) resonator, to be described next, feedback is provided in the voltage rather than charge domain. That means there no charge transfer is needed through the virtual ground from the output of the resonator to its input to realize the resonator transfer function. The VPNP was originally proposed in our previous work [12], and is insensitive to capacitor mismatches. This current structure is adapted for UGR low-voltage structure. It is mismatch sensitive similarly to the improved charge-mode PNP architecture shown in [13].

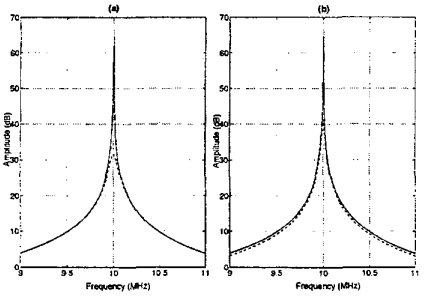


Figure 8: Simulation results of VPNP type resonator from SWITCAP2 with $f_{clock}$=40 MHz (a) for different opamp DC gains: $A_{dc}$=120 dB (solid), 50 dB (dots); (b) for different opamp bandwidths: $f_u = \infty$ (solid), $f_u$=160 MHz (dots).

In this structure, $C1p$ and $C1n$ hold the differential output voltage $v_{out}(n) = vin(n - 1/2) - v_{out}(n - 2)$ during clock phase 'c'. At the same time, $C3p$ and $C3n$ are connected between the output of the resonator and the ground, and hence they are charged to $v_{out}(n)$. Two clock periods later, the $C3$ capacitors are connected as feedback capacitors during clock phase 'b', thus providing $v_{out}(n + 2)$. At the same time the input and output of the resonator are commutated to provide sign change as described previously for the I2P structure.

This operation does not integrate error charges and hence there is no center frequency shift.

The drawback of this architecture is the limited signal swing due to the need not to forward bias the switches in the feedback path of the opamps. When the voltage at the output of the opamp drops, the voltage at the left plates of the feedback capacitors will also drop. This may forward bias the pn junctions of the switches in the feedback path. Therefore, the signal range will be reduced compared to the previous implementations.

## 8. SIMULATION RESULTS

Simulation results for the four different resonators are presented in Fig. 9 for comparison purposes. The resonators are the lossless-discrete-loop (LDI) [1], two-delay-loop (TDL) [2], integrating-two-path resonator (I2P), and voltage-mode-pseudo-N-path (VPNP) circuits.

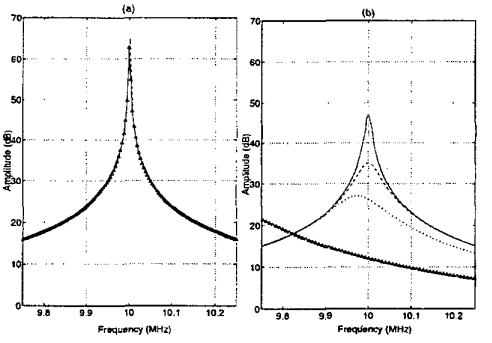


Figure 9: Simulation results of the LDI (triangle), TDL (dotted), VPNP (dashed), I2P (solid) for $f_{clock}$=40 MHz (a) $f_u = \infty$ and $A_{dc}$ = 120 dB (b) $f_u$ = 160 MHz and $A_{dc}$ = 60 dB

The peak resonances of all four resonators are obtained at 10 MHz for the ideal case where $f_u = \infty$, $A_{dc}$ = 120 dB, and $f_{clock}$ = 40 MHz.

In Fig. 9 (b), the finite bandwidth and gain limitation of the opamp are simulated with $f_u$ = 160 MHz and $A_o$ = 60 dB. I2P and VPNP have almost 16 dB and 28 dB gain loss, respectively, but no shift in the center frequency. TDL has 37 dB gain loss and 55 kHz center frequency shift. As seen in the figure, the LDI circuit resonance is far off from the 250 kHz bandwidth around the center frequency.

From the SWITCAP2 simulations, it can be seen that SC resonator circuits can be designed for high gain (Q) and selective frequency response which is insensitive to analog circuit imperfections. The LV I2P and VPNP structures not only demonstrate performance enhancements, but also allow the operation to remain functional down to a 1 V supply voltage.

## 9. CONCLUSIONS

In this paper, four different LV resonators were compared, based on SWITCAP2 simulations. I2P shows the best performance when there are finite gain and bandwidth limitations of the opamps. The LDI, TDL, and I2P require four single-ended opamps to realize the resonator function; on the other hand VPNP can realize the resonator operation with just two single-ended opamps. This work thus verifies possible implementations for high-frequency SC circuits with low supply voltages.

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