Analog (S)witchcraft, or How to Perform Accurate and Linear Data Conversion Using Inaccurate Nonlinear Elements

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Abstract. This paper provides a tutorial overview of some recently developed methods for enhancing the accuracy and linearity of data converters (analog-to-digital as well as digital-to-analog) by introducing auxiliary digital circuitry which calibrates, cancels and/or corrects the errors introduced by the unavoidable inaccuracy of the analog components used in the conversion. Simple but practical examples are used to illustrate the various improvement techniques.

I. Introduction

Conventional high-accuracy data converters require extreme accuracy in the matching of analog components, which cannot be achieved in an integrated circuit. In this paper, three strategies: analog correction, error cancellation and spectral shaping are described for achieving accurate dynamic component matching. Switched-capacitor (SC) DACs will be used to illustrate the techniques.

II. Analog Correction Techniques

Fig. 1 shows the conceptual diagram of a DAC constructed using SC circuitry. The operation of the circuit is as follows. The input binary word is converted into a thermometer code with bits $x_1,\ x_2,\ \ldots,\ x_M$ such that if the integer value of the input word is m, the bits $x_1,\ x_2,\ \ldots,\ x_m$ are 1, and the rest are 0. During the reset phase ($\phi_1 = 1$), the feedback capacitor C_f is discharged and all input capacitors are charged to the reference voltage V_{ref}. Next, during the conversion phase ($\phi_2 = 1$), the first m input capacitors are discharged into C_f, resulting in an output voltage $V_{out} = (mC/C_f)V_{ref} = (m/M)V_{ref}$.

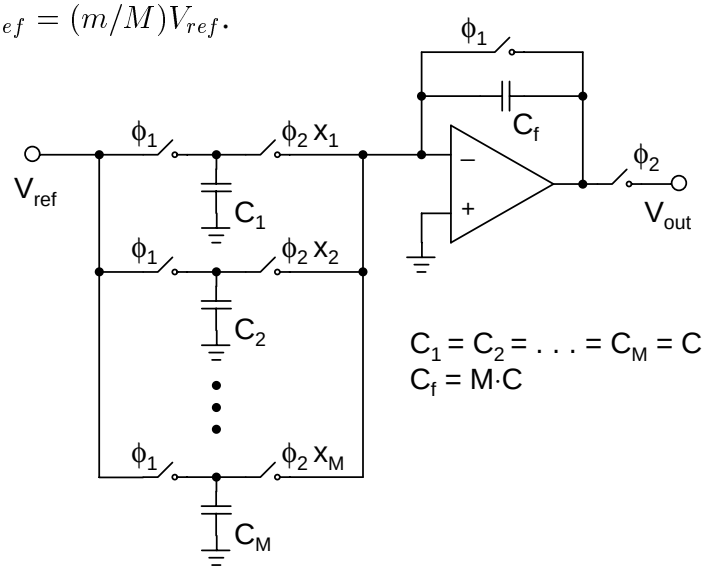

Figure 1: A switched-capacitor DAC

Analog correction of the matching error may be achieved by using the system shown in Fig. 2, where each capacitor C_i is split into a coarse and a fine part, C_{ci} and C_{fi}, respectively, and a separate buffered reference voltage V_{refi} is introduced for each the C_{fi} [1]. When ϕ_2 is high, capacitors C_{ci} and C_{fi} are discharged into C_f if $x_i = 1$, otherwise they hold their charges. A calibration stage, consisting of a transconductor and a reference capacitor C_{ref}, is used to

readjust the V_{refi} sequentially when the i-th calibration clock phase ϕ_{ci} is high, so as to make the combined charges stored in C_{ci} and C_{fi} equal to $C_{ref}V_{ref}$. To replace the capacitor being calibrated, an extra set of C_c and C_f is also needed. The resulting conversion accuracy can then be as high as 15 bits. The process is similar to that proposed earlier for current-mode DACs by Groenewald et al. [2].

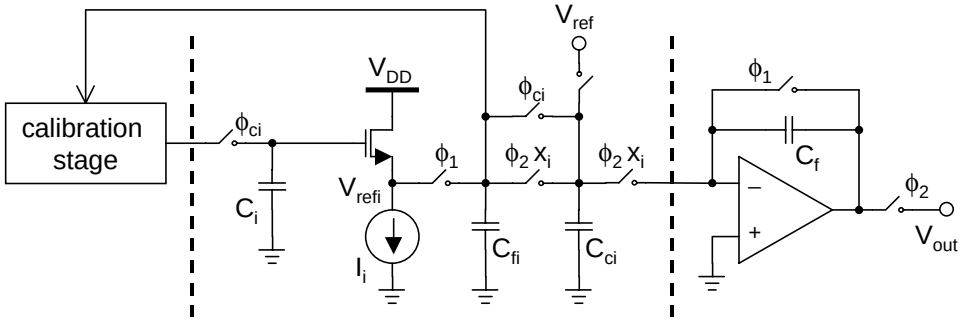

Figure 2: The DAC of Fig. 1 with analog mismatch correction

III. Error Cancellation Techniques

Error cancellation techniques are similar to analog correction in the sense that analog quantities (charge, voltage, etc.) are manipulated under digital control to achieve error cancellation.

Consider the DAC stage containing two equal-valued capacitors, shown in Fig. 3 [3]. Its operation under ideal conditions is as follows. The digital input words are entered serially, with the least significant bit (LSB) first. Before each word enters, both capacitors are discharged by the reset switches. Then, when $\phi_1 = 1$, C_1 is charged to a voltage V_{ref} or 0, depending on the LSB. Next, as $\phi_2 = 1$, C_1 and C_2 share charges. Afterwards, C_1 is disconnected from C_2, and again is charged to V_{ref} or 0, depending on the value of the second LSB. This procedure is repeated for each bit, until the MSB has been processed. At this point the charge stored in both C_1 and in C_2, and hence the voltage across them, represents the converted value of the input digital word.

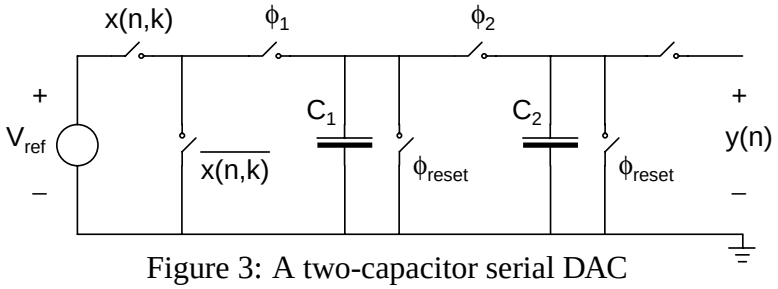

Figure 3: A two-capacitor serial DAC

In practice, the capacitors used cannot be made exactly equal, and hence the conversion becomes inaccurate. This introduces a deterministic nonlinearity into the process, which gives rise to harmonic distortion. We can quantify the imperfect capacitor matching property by defining the error coefficient $\delta = (C_1 - C_2)/(C_1 + C_2)$ for the nominally matched capacitors C_1 and C_2. Analyzing in detail the charge transfers that occur for the N clock cycles, an explicit formula can be found for the error err of the final DAC output.

A simple way to perform capacitor mismatch error cancellation is to repeat the conversion for the same input word with the roles of capacitors C_1 and C_2 interchanged. This changes the sign of δ, while leaving the rest of the formula giving err unchanged. Hence, when the two outputs obtained in the two conversions for the same input word are added together, the effect of the capacitor mismatch error cancels. Thus, at the cost of doubling the conversion time, the accuracy is much enhanced. Capacitor mismatch error cancellation schemes using this property were suggested for a number of different architectures [4]-[5].

IV. Spectral Error Shaping

In spectral error shaping, the error signal generated by the mismatch of nominally equal-valued elements gets filtered so as to suppress its in-band spectral energy. Since the filtering is usually only first or second order, this technique will only be effective if the signal band occupies only a relatively small part of the 0 to $f_s/2$ range, where f_s is the sampling frequency, i.e., if the oversampling ratio $R = f_s/(2f_b)$ is much greater than 1. Here, f_b denotes the bandwidth of the signal being converted. The filtering action can be obtained by appropriately choosing the indices of the matched elements participating in the conversion of each signal sample. One option is to choose the capacitors used in converting each input sample randomly, rather than deterministically as described above [6]. Now the error will be in general different each time a fixed code is entered into the DAC, and hence the matching errors introduce random noise, rather than distortion. Thus, using this strategy, the mismatch error is converted into a wide-band noise, only a fraction of which falls in the signal band. This process can be regarded as zero-order spectral shaping.

First-order spectral shaping can be achieved based on the following considerations. Consider the input/output characteristics of an ideal SC DAC (Fig. 1). It is possible to choose the elements used during conversion such that the *average* value of the output for each code falls on a straight line. This suppresses harmonic distortion, and eliminates the dc error for any input. Specifically, if all input elements are used with equal frequency for each code, then the average outputs will fall on a straight line, and hence the element-value errors will result in a noise with a zero mean value. This indicates that the power spectral density (PSD) of the mismatch noise has a zero at dc, and the PSD is nonuniform. This process thus provides a first-order mismatch-noise shaping.

There exist numerous techniques for achieving the required equal average usage for the individual capacitors. In one (called barrel shifting [7]), the capacitors used for the first sample with value m_1 are $C_1,\ C_2,\ \ldots,\ C_{m1}$; for the second sample with value m_2, the set $C_2,\ C_3,\ \ldots,\ C_{m2+1}$ is used, etc., and the selection wraps around to C_1 once the last of the C_i has been used. Another averaging technique (called individual level averaging [8]) keeps track of the past usage of each element C_i for each input code, and assigns them so as to keep the average usage uniform. Yet another (named data-weighted averaging [9]) uses the set $C_1,\ C_2,\ \ldots,\ C_{m1}$ for the first sample, $C_{m1+1},\ C_{m1+2},\ \ldots,\ C_{m1+m2}$ for the second, etc., with wrap-around to C_1 after the last C_i (C_M) has been used. These techniques have various relative advantages and disadvantages; the barrel-shifting method is simple to perform, but it can generate undesirable tones in the pass-band for some input frequencies, while individual level averaging, which is not susceptible to tone generation, requires more elaborate digital circuitry, and takes longer to achieve the desired averaging. Data-weighted averaging is relatively simple, and achieves rapid averaging since no element will be used twice until all others are used. Other techniques have also been proposed for achieving first-order noise shaping [10]-[11].

To achieve higher-order noise shaping, the binary logic signal $x_i(n)$, which decides whether or not V_i will contribute to V_{out} in the n-th sampling period, can be forced to assume the form

$$x_i(n) = f(n) + h(n) * [e_i(n) - r(n)] \tag{1}$$

Here, the asterisk denotes the discrete-time convolution; also, $f(n)$ is a bounded function, independent of i, and $h(n)$ is the impulse response of the desired shaping filter. Finally, the $e_i(n)$ are pseudo-random bounded functions, in general different for each i. Then, the output error in the n-th period is

$$err(n) = \sum_i x_i(n) dV_i = [f(n) - h(n) * r(n)] \sum_i dV_i + h(n) * \sum_i e_i(n) dV_i \tag{2}$$

where dV_i is the output error introduced by the i-th mismatched capacitor. If the full-scale output is accepted as correct, the first term on the RHS is zero, and the second term contains the desired filter function. Hence, if we can generate a set of binary logic sequences x_i such that in each sampling period they satisfy eq.(1) and their sum equals the input value m, the error shaping is accomplished.

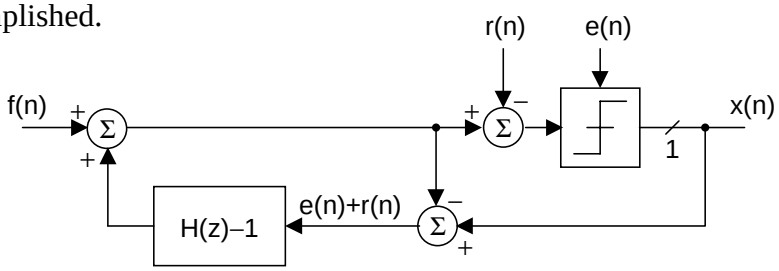

Figure 4: Digital delta-sigma loop for generating the $x_i(n)$ sequence of eq.(1)

Consider next the digital delta-sigma loop shown in Fig. 4 [12]. Analysis shows that its single-bit output sequence $x_i(n)$ is given exactly by eq.(1), if the truncation error of the comparator is denoted by $e_i(n)$, and if $H(z)$ is the z-transform of $h(n)$. Hence, M such structures (one for each capacitor C_i) can be used to generate the $x_i(n)$ sequences for the operation of the DAC.

For a positive integer system, the common input $f(n)$ of the loops can be chosen so that the input of the truncation block in one of the loops is zero, and in all others it is positive. This will minimize the signals in the loops, and hence helps to keep their operation stable. The sequence $r(n)$ is essentially a time-variable threshold for the comparators. It is chosen such that exactly $m(n)$ of the M loops have outputs $x_i(n) = 1$ during period n.

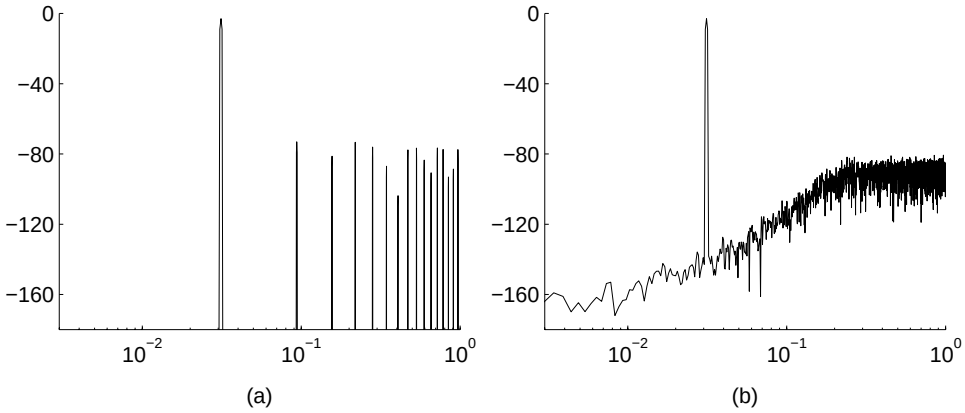

Figure 5: Unshaped (a) and shaped (b) output spectra of the two-capacitor DAC

The mismatch error shaping process can be applied to other structures, such as the two-capacitor serial DAC described above and shown in Fig. 3 [5],[13]. Whereas in the case of the M-element DAC of Fig. 1 the degree of freedom which allowed spectral error shaping without changing the signal processing function was the arbitrary choice of the C_i in generating the analog output, here there is the option of interchanging the roles of C_1 and C_2 in each clock cycle when $\phi_1 = 1$. By generating a binary sequence $t(n,k)$ which decides the role of the capacitors during the conversion of the k-th bit of the n-th input word with a digital delta-sigma loop, a filtered mismatch error can be obtained. Fig. 5 compares the unshaped and shaped output spectra of the DAC for a sinewave input with a peak-to-peak amplitude of $0.7V_{ref}$, an oversampling ratio of 10 and an assumed mismatch of $\delta = 0.1\%$. A third-order noise shaping and dithering was used in the loop generating $t(n,k)$. The unshaped error gives a S/THD ratio of only 70 dB; the S/(N+THD) for the mismatch-shaped spectrum is around 96 dB, a gain of

26 dB. Note that unlike the error-cancelling scheme discussed earlier for this structure, mismatch shaping does not double (or change in any way) the conversion time; the only cost is the added digital circuitry, which is insignificant.

VI. Conclusions

In this tutorial paper, it was shown that very high accuracy and linearity may be obtained in data conversion even when using inaccurate analog components, by introducing additional digital logic which takes advantage of the hidden degrees of freedom in the operation of the converter circuit to achieve cancellation, calibration or frequency shaping of the error introduced by the analog imperfections. This enables the designer of mixed-mode interface circuits to satisfy the increasing demands for ever faster and more accurate fully integrated data converters.

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