To couple power into the antenna, the printed conductors were connected by probes (x_{psi}, y_{psi}) relative to the centre of the overall size $L \times W$, onto the feed network located beneath the ground plane. This is done here by connecting pins through the dielectric material from the feed network ports (similar to [6] but without the phase shifts) onto the antenna ports labelled (x_{pi}, y_{pi}). The printed spirals were designed for an input impedance of 50Ω, so transformers were required on the feed network to transform the input port into the radiators. A dielectric constant material (RT/Duroid 6010©, ε_r = 10.2) was used for the feed network to maintain the small size of the antenna.

Results and discussion: Fig. 2 shows the measured return loss bandwidth of the proposed shorted spiral antenna. The 10dB return loss bandwidth of the antenna is 9.2%. This value is slightly higher than a standard circular and rectangle probe-feed shorted patch mounted on the same substrate, 6.7 and 7%, respectively. The larger bandwidth is due to the previously mentioned mutual resonance phenomenon between the spirals, which is evident in the plot of Fig. 2. To put these results into perspective, for a fixed frequency, the proposed spiral antenna is 28% smaller in physical length compared to a shorted circular patch (radius = 7mm). A greater reduction is achieved (~33%) when compared to a standard rectangular shorted patch (15 × 10mm) using the same dielectric materials. An interesting factor to note is that, although the antenna is smaller, the bandwidth has not been compromised due to the two radiators interacting. It should be further noted that a larger reduction in size could have been readily achieved, although at the expense of bandwidth and ease of fabrication. The far-field radiation patterns were measured at 2.35GHz. It can be observed from Fig. 3 that the antenna has an omni-directional pattern (note that broadside is 0 degrees in this plot). The cross-polarisation levels evident in Fig. 3 are typical for electrically small printed antennas mounted on small ground-planes [5]. Here the ground-plane extends 8mm past the printed spiral conductors. The measured gain of the antenna was 0.2dBi.

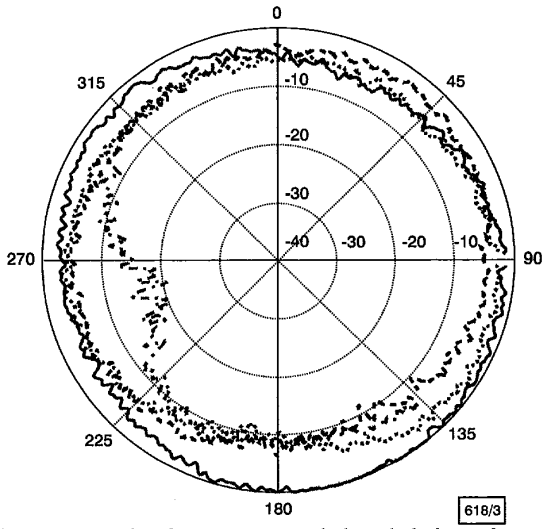

Fig. 3 *Measured radiation patterns of shorted dual spiral printed antenna*

——— H-plane (cross)
····· H-plane (co)
– – – – E-plane (cross)
–·–·– E-plane (co)

Conclusions: We have presented a small printed spiral antenna. The measured 10dB return loss bandwidth is 9.2%. The proposed antenna is 28% smaller than a standard shorted printed antenna and yields a higher bandwidth.

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1V input sampling circuit with improved linearity

D. Chang and U. Moon

A highly linear low-voltage sampling circuit is proposed. Operation under 1V power supply is possible without compromising linearity. Performance limiting nonlinear MOS switch resistance characteristics are suppressed by a combination of three novel design techniques.

Introduction: In keeping with the down-scaling trend of submicron CMOS process where the allowed maximum voltage supply/swing and the feature size are becoming smaller with technology advancements, a few low-voltage architectures have shown 100% low-voltage compatibility – they are switched-opamp [1] and unity-gain-reset (UGR) structures [2]. However, for these low-voltage circuits to be effective in all applications, they require a fast and accurate input sampling circuit that is able to sample and transfer signals from sources external to the IC. One such circuit exists in the context of a switched-opamp structure [3].

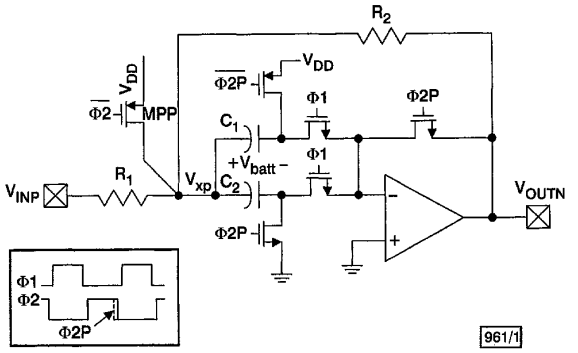

Fig. 1 *Conventional input sampling circuit*

One signal path shown for simplicity
Φ1 amplification phase
Φ2 output reset phase

Fig. 1 shows a modified version of the low-voltage switched-opamp input sampling circuit reported in [3]. The modifications include conversion to UGR structure and pseudo-differential configuration. The primary focus of this circuit is to operate within a given supply voltage without using clock-voltage boosters, which may violate the maximum allowed voltage for a given CMOS technology. Since all switches need to be driven by either maximum ($\simeq V_{DD}$) or minimum ($\simeq GND$) voltages, series switches in the input and output signal paths are eliminated. During the reset phase (Φ2), V_{xp} is pulled up to V_{DD} while C_1 is precharged to V_{DD} and C_2 discharged. During the amplification phase (Φ1), V_{xp} becomes $V_{DD}/2$ (i.e. V_{batt}) due to charge sharing between C_1 and C_2. V_{xp} acts as an intermediate virtual ground. Assuming that the input common-mode (CM) voltage is $V_{DD}/2$, the output CM volt-

age also becomes $V_{DD}/2$. During Φ2 (ignoring the body effect for simplicity) the resistance of the PMOS switch *MPP* is

$$R_{MPP} = \frac{1}{\beta[(V_{SG} - |V_{TH}|) - V_{SD}]} \quad (1)$$

where $\beta = \mu_p C_{OX}(W/L)$. The voltage division between R_1 and R_{MPP} introduces nonlinear voltage fluctuation at V_{xp}:

$$V_{xp} = \left(\frac{R_{MPP}}{R_1 + R_{MPP}}\right)V_{INP} + \left(\frac{R_1}{R_1 + R_{MPP}}\right)V_{DD} \quad (2)$$

Owing to this nonlinear resistance R_{MPP}, signal distortion results. The level-shifting voltage V_{batt} is a function of V_{xp}, and V_{OUTN} is a function of V_{batt}. Assuming that the opamps have finite open-loop gain A, those voltages are given by

$$V_{batt} = \frac{V_{xp}(C_1 + C_2) - (C_1 V_{DD} + C_2 GND)}{C_1 + C_2} \quad (3)$$

and

$$V_{OUTN} = \left(1 + \frac{1}{A}\left(1 + \frac{R_2}{R_1}\right)\right)^{-1} \times \left(\left(1 + \frac{R_2}{R_1}\right)V_{batt} - \left(\frac{R_2}{R_1}\right)V_{INP}\right) \quad (4)$$

It can be observed that the output harmonic distortion results from the distortion at V_{xp} caused by R_{MPP} nonlinearity.

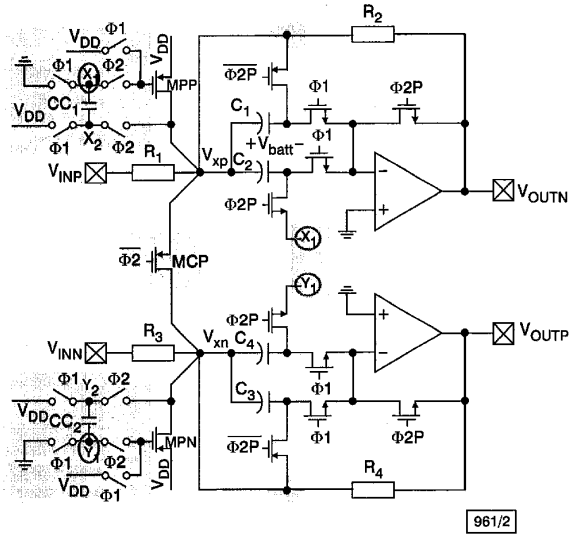

Fig. 2 *Proposed input sampling circuit*

Φ1 amplification phase
Φ2 output reset phase

Proposed circuit: Three design techniques are proposed to minimise this nonlinearity problem. They are depicted in shaded areas in Fig. 2. During Φ2, the capacitor CC_1, which was precharged to V_{DD} during the previous clock phase, is connected between the PMOS gate and V_{xp}, so that the gate voltage of *MPP* can track the variation of V_{xp}. This makes R_{MPP} constant:

$$R_{MPP} = \frac{1}{\beta(V_{DD} - |V_{TH}|)} \quad (5)$$

Similar to the previous voltage-boostrapping techniques [4], this work focuses on the linearisation of R_{MPP} by putting a precharged capacitor between gate and drain/source. Note that V_{xp} is slightly lower than V_{DD} during Φ2, and X_1 may go below *GND*, which can cause a latch-up condition. Careful design requires proper sizing of CC_1 with respect to C_2. We have used CC_1 = 2pF and C_2 = 0.6pF in our design. To cancel the remaining distortion at the output, V_{xp} and X_1 are sampled to C_1 and C_2, respectively, instead of sampling V_{DD} and *GND*. In doing so, the nonlinear fluctuation at V_{xp} is cancelled during amplification:

$$V_{batt} = \frac{V_{xp}(C_1 + C_2) - (C_1 V_{xp} + C_2(V_{xp} - V_{DD}))}{C_1 + C_2} = \frac{C_2 V_{DD}}{C_1 + C_2} \quad (6)$$

The output voltage is no longer a function of V_{xp} or R_{MPP}, but a linear function of V_{INP} only:

$$V_{OUTN} = \left(1 + \frac{1}{A}\left(1 + \frac{R_2}{R_1}\right)\right)^{-1} \times \left(\left(1 + \frac{R_2}{R_1}\right)\left(\frac{C_2 V_{DD}}{C_1 + C_2}\right) - \left(\frac{R_2}{R_1}\right)V_{INP}\right) \quad (7)$$

Because the devices/elements will never match perfectly in circuit implementation, incorporating both techniques will minimise distortion. Another straightforward way to improve the linearity of R_{MPP} is to increase the device size, so that the fluctuation at V_{xp} (V_{xn}) is as small as possible. However, this increases the chip area. In the proposed circuit, we have incorporated a differential resetting switch *MPC*. The differential resetting switch can be made half the size of *MPP* and *MPN*, and will achieve the same result as doubling the sizes of *MPP* and *MPN*. Using *MPC* also helps to suppress even harmonics, that are due to device mismatches in the two pseudo-differential signal paths.

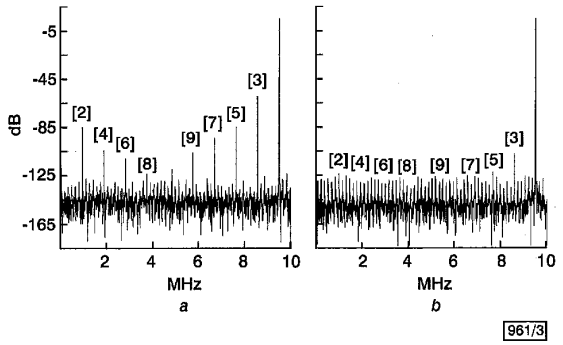

Fig. 3 *FFT plot of conventional and proposed circuit*

a Convertional circuit
b Proposed circuit

Simulation results: The circuits were simulated in Spectre using 0.18μm CMOS BSIM3 models. The threshold voltages were 0.45 and 0.6V for NMOS and PMOS transistors, respectively. Fig. 3 shows an FFT plot of the conventional (Fig. 1) and proposed (Fig. 2) circuits with sampling frequency of 20MHz, input frequency of 9.53125MHz ((61/128) × 20MHz), and 1V supply voltage. Resistors, capacitors, and PMOS switches (*MPP* and *MPN*) include 1% random mismatches, and modelled opamps with finite gain-bandwidth are used for simulation. Since the fundamental frequency is chosen to be nearly at Nyquist, all harmonics have been folded. The conventional circuit shows a total harmonic distortion (THD) of –40dB, while the proposed circuit shows –100.5dB. The proposed techniques reduced both the odd and even harmonics. There is little variation of THD when the input signal is swept over the entire Nyquist bandwidth.

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CMOS circuit for readout of microbolometer arrays

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A CMOS circuit for the readout of microbolometer arrays is presented. It provides a pulsed bias for the microbolometers, signal amplification and multiplexing to a common output. The chip can be used with linear and small two-dimensional arrays of microbolometers realising a hybrid infrared sensor.

Introduction: Thermal infrared (IR) sensors are very attractive devices in comparison with narrow-bandgap photon detectors in applications where detector cooling must be avoided. In recent years there has been a wide interest in the development of surface micromachined bolometers [1]. This technology allows the fabrication of structures with very good thermal isolation, therefore high sensitivity to IR radiation. Microbolometers based on thin film VO_x [2], poly Si-Ge [3], metals [4] and amorphous semiconductors [5] have been developed.

The effect of the IR radiation is a resistance change on a microbolometer. This change must be detected from the readout circuitry and in the case of a microbolometer array the produced signal must be multiplexed to a common output. The readout circuit can be fabricated on the same substrate as the bolometers (monolithic sensors) or as a different chip (hybrid sensors). Various readout schemes have appeared in the literature as the integration of the current flowing through the microbolometer [1, 4], the modulation of the phase of an RC-oscillator due to the resistance change [6] and a chopper stabilisation technique for noise reduction [7].

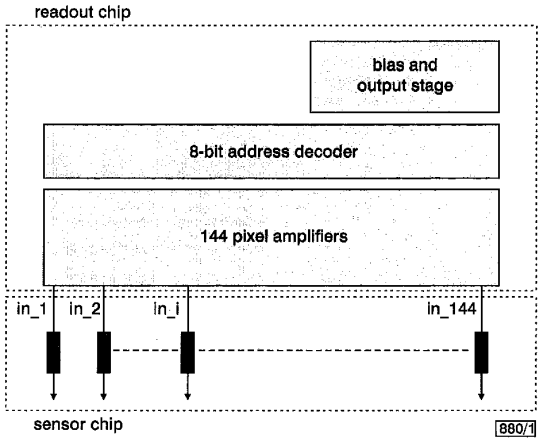

Fig. 1 *General architecture of readout chip and connectivity with microbolometer array (sensor chip)*

In this Letter we propose a new readout scheme that provides a pulsed current bias, measures and amplifies the voltage drop across each microbolometer and multiplexes this signal to a common output. With this scheme and in contrast to integrating readout, a continuous time measurement of the voltage drop across the microbolometer is performed. The advantage of this circuit is the high dynamic range that allows the accommodation of the large signal swings due to the self-heating effects of the microbolometers without adding extra circuitry [8]. Based on that scheme, a CMOS chip capable of reading linear arrays or small two-dimensional arrays of microbolometers with pixel counts up to 144 has been fabricated and tested. The technology used is CMOS with 0.7μm minimum feature size and 0–5V power supply. The readout chip is connected with the sensor by means of a ceramic substrate using a multi-chip-module (MCM) technology. The same design can be used for monolithic sensors when integrated on the same substrate with the microbolometers.

General architecture of readout chip: Each microbolometer has its own dedicated readout circuit, referred to as pixel amplifier. The chip contains 144 pixel amplifiers, an 8 bit address decoder, an output driver and the bias stages. The general architecture is shown in Fig. 1 together with the connectivity with the sensor chip on the MCM. The pixel amplifiers are designed on a pitch of 50μm in order to match the pitch of the bolometers to be tested. This simplifies the connectivity and, most importantly, minimises the design effort for a future integration with the microbolometer array.

Employing an address decoder instead of a shift register for the multiplexing allows for dynamic windowing and, most importantly, eases the connection when a two-dimensional microbolometer array is used.

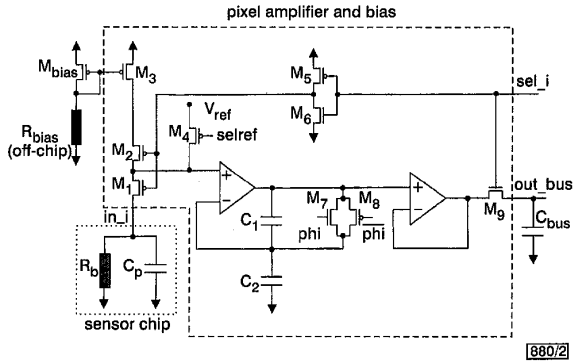

Fig. 2 *Schematic diagram of pixel amplifier*

Connectivity with the microbolometer is also shown. Transistor M_{bias} is common for all the pixel amplifiers. Capacitance Cp accounts for parasitics introduced from bonding wires and MCM substrate

Pixel amplifier: Fig. 2 is a schematic diagram of a pixel amplifier. Before the readout of a line a calibration phase proceeds. During calibration no pixel is selected (signal *sel_i* that is generated from the address decoder is low for every pixel). When *sel_i* is low, transistors M_1 and M_2 are cut-off and the bolometers are not connected with the amplifiers. Signal *phi* which is applied to M_7 is pulsed high while signal *selref* is pulsed low. The complementary of *phi* is applied to M_8. Therefore, voltage V_{ref} is sampled on the capacitor C_2 neglecting the opamp offset. The readout phase then takes place. Pixels are selected according to the digital addresses that are applied in the address decoder. When a certain pixel is selected, the signal *sel_i* corresponding to that pixel goes high. Therefore, the microbolometer is biased with a current determined from the current source that consists of M_3, M_{bias} and the off-chip resistor R_{bias}. In this way a pulsed current biasing is performed that minimises the self-heating of the microbolometer owing to the power dissipated from the bias current. Signal *selref* is now high and *phi* is pulsed low, setting the gain of the amplifier in the frequency domain as

$$H(s) = \frac{1}{\frac{1}{A(s)} + \frac{C_1}{C_1+C_2}} \qquad (1)$$

where $A(s)$ is the open-loop gain of the opamp. The output of the amplifier is

$$V_o = V_{ref} - |H(0)|(V_{ref} - V_{bol}) \qquad (2)$$

where $H(0)$ is the low frequency gain of the amplifier and V_{bol} is the voltage drop across the bolometer. This voltage V_o is available after a period determined from the gain-bandwidth product of the opamp. The second opamp that is placed in a unity-gain configuration drives the output bus that exhibits a parasitic capacitance C_{bus}, at the desired speed. Transistor M_9 is switched on and therefore connects the amplifier output to the common output (out_bus). The opamps are realised using differential pairs.

Eqn. 2 implies that the signal difference between two pixels is the difference in the voltage drops across the two microbolometers multiplied by the low frequency gain of the amplifier, i.e. the pixel