els (Fig. 1). The input CM level was set to 700mV, so that the minimum input voltage is at V_{SS} and the integrator output CM level was set to mid-supply.

The operational amplifiers were BiCMOS folded cascode OTAs with PMOS input devices for a low 1/f-noise. NPN bipolar transistors were used as cascode devices on the NMOS current sources to push the first parasitic pole to a high frequency. The opamp was allowed to slew since it was found to be more power efficient even though the settling error becomes nonlinear. At a low supply voltage it is difficult to design the input differential pair for sufficiently high V_{GS} to ensure that the amplifier does not slew.

The input switch of an SC circuit distorts a high frequency input signal since its on-resistance is signal dependent. Usually CMOS switches are used at the input to reduce the variation of the switch conductance. However, the conductance is not a smooth function of the input voltage which produces higher-order distortion products for a high frequency input.

Alternatively, the input switch can be arranged so that the gate-to-channel voltage becomes constant. This reduces the tracking distortion by reducing the input voltage dependency of the switch on-conductance. The on-conductance depends also on the V_{DS}-voltage, but as long as the corner frequency of the RC loop formed by the input switch and the sampling capacitor is much higher than the input frequency, the voltage drop over the switch is small and the signal is not distorted.

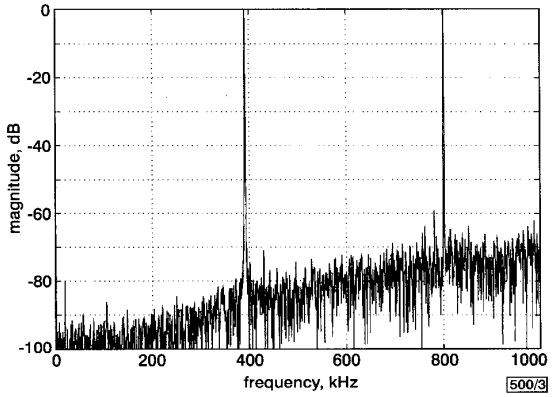

Fig. 3 *Measured IM3 with –5.5dBV 50.38MHz and 50.8MHz interferers*

A number of circuits to achieve a constant gate-to-channel voltage have been presented in the literature [2]. A simple circuit arrangement which generates a constant $V_{DD} - V_T$ gate-to-channel voltage was used in this design (Fig. 2). During the integration phase (I) the gate of the input switch $M1$ is pulled low by $M4$ and the capacitor $C1$ is loaded to $V_{DD} - V_T$ by $M5$ and $M6$. At the onset of the sampling phase (S) $C1$ is connected between the input and the gate of $M1$ by the transistors $M2$ and $M3$. Because the common-mode level of the input is at 700mV, the gate voltage of $M1$ will rise roughly to V_{DD} and follow the input signal.

The tracking bandwidth of the constant gate-to-channel voltage circuit is determined by the on-resistances of $M2$ and $M3$, together with the gate capacitance of $M1$. In most cases, the gate capacitance is significantly smaller than the sampling capacitor, which makes the tracking bandwidth of the constant gate-to-channel voltage circuit wider. However, the performance already starts to degrade one decade earlier, because the signal phase at the gate starts to lag with respect to the input.

Experimental results: In a radio application the receiver has to operate in the presence of large interfering signals. In the GSM standard this is characterised by introducing a large blocking signal with a 3MHz offset from the carrier and measuring the noise power over the desired channel.

The measured SNR over a 100kHz signal band for a 53MHz blocking signal rises steadily to 81dB and then saturates. The saturation is probably caused by noise coupling through the substrate or package pins and the sampling jitter. The dynamic range is estimated to be 88dB by extrapolating the SNR curve to lower signal levels.

The linearity in a radio receiver is characterised by the intermodulation distortion products from the neighbouring channels that fall on the desired channel. Tones at 50.38 and 50.8MHz were combined and passed through a passive 100MHz filter before the balun and the ΔΣ modulator, to cut the third harmonic generated by the signal sources. The resulting spectrum with –5.5dBV interferers is shown in Fig. 3. With –6dBV interferers, the measured IMD3 was –92dBV, which gives an IIP3 of +36.9dBV. At lower interferer levels the IMD3 was quickly buried under the noise floor.

The measured power consumption, excluding the output buffer, was 22mW from a 2.7V supply. The performance is summarised in Table 1.

Table 1: Performance summary

Technology	0.35μm BiCMOS
Core area	0.42mm²
Supply voltage	2.7V
Power consumption	22mW
Clock and input frequency	50MHz
Full scale input	0dBV
Peak SNR (100kHz)	81dB
Dynamic range	88dB
IIP_3	+36.9dBV

Conclusion: The implemented ΔΣ modulator demonstrates the feasibility of IF sampling, even with a low supply voltage of 2.7V. A very high IIP3 of +36.9dBV at the input frequency of 50MHz was achieved by optimising the internal common-mode levels and by generating a constant channel-to-gate voltage for the input switches. The peak SNR for a 53MHz blocking signal was measured to be 81dB over a 100kHz bandwidth, which is somewhat lower than expected. The degradation could be due to noise coupling through the substrate or the package pins and from the sampling jitter.

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Correlated double sampling integrator insensitive to parasitic capacitance

T. Kajita, G.C. Temes and U.-K. Moon

A new correlated double sampling (CDS) scheme is proposed which improves the operation of an integrator with a large parasitic capacitor at the input node of an op-amp. It suppresses the effects of the $1/f$ noise and offset voltage of the op-amp, as well as the kTC charge noise from the parasitic capacitor. It also reduces charge injection and clock feedthrough effects.

Introduction: CDS techniques can reduce the effects of the offset voltage of an op-amp, increase the effective op-amp gain and reduce the $1/f$ noise in switched-capacitor (SC) circuits [1]. Because it provides higher accuracy, CDS is often used in converters based on the delta-sigma modulation. When such a converter is used as a front end for a capacitive sensor, e.g. an accelerometer or a pressure sensor, the sensor may be used as the input-sampling capacitor. Sometimes, the sensor must be on a separate chip [2]. In such cases, the large (~20pF) parasitic capacitance of the connection between the sensor and the circuit will have detrimental effects on the operation. To minimise the problems due to the large parasitic capacitance, the following basic rules must be followed: (i) the floating terminal of the parasitic capacitor should not be reset to a DC potential in any clock phase; (ii) no series switch is allowed between the parasitic capacitor and the input terminal of the op-amp; (iii) the front-end circuit block should not be an amplifier, but an integrator.

The first rule holds because switching or resetting the large parasitic capacitor creates a large error charge flow, since the input potential of the op-amp is not exactly at ground. (It contains an offset voltage, random noise dominated by the $1/f$ effect at low frequencies, some signal voltages due to the finite op-amp gain, and also sampled kTC charge noise.) This large error charge will cause a large error voltage at the output. The second rule must be satisfied in order to minimise the kTC charge noise caused by the resistance of the switch. The switch between the parasitic capacitor C_p and the input terminal creates a noise voltage with a mean-square value kT/C_p, which leads to an RMS noise charge $\sqrt{[kTC_p]}$. This is large if C_p is large. The third rule is based on the consideration of the op-amp noise. The op-amp noise is amplified to the output greatly due to the large parasitic capacitor of either the amplifier or the integrator. However, the input-referred noise of the integrator is first-order shaped, and hence its noise power is much smaller than that of the amplifier at low frequencies. Hence, for the measurement of low-frequency signals, it is better to use the integrator for the front-end circuit block.

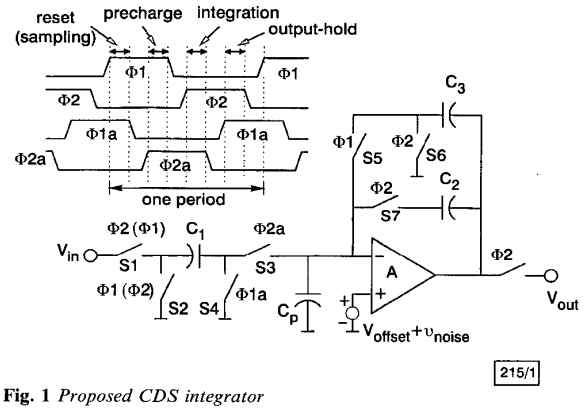

Fig. 1 *Proposed CDS integrator*

Proposed circuit: Fig. 1 shows the proposed CDS circuit. It can be used as an inverting integrator with the phases without the parentheses. Also using the clock phases shown in parentheses, the circuit of Fig. 1 performs as a noninverting integrator.

The basic principle of operation [3] is that if the input and feedback capacitors C_1 and C_2 are connected to the virtual ground node while S_1 and S_2 switch the input-side terminal of C_1 between V_{in} and ground, then the magnitude of the charge entering C_2 will be (to a very good approximation) $C_1 \cdot V_{in}$, independent of the slowly varying components (offset, $1/f$ noise, and signal) of the op-amp input error voltage. If afterwards a grounded switch (S_3 or S_7) disconnects C_2, then its charge injection causes only a small constant offset in V_{out}. Thus, the charge integration is nearly ideal.

The detailed operation of the inverting integrator is as follows. Before S_1 and S_2 are toggled, C_1 is reset by S_2 and S_4, while C_2 is disconnected, but the holding capacitor C_3 holds the previous op-amp output. When S_4 opens, S_5 remains closed until S_3 closes. During this period, the input node voltage of the op-amp (due to offset voltage, noise, and finite op-amp gain) is stored in C_1. Hence, the sampled charge delivered by C_1 to C_2 when S_2 opens and S_1 closes is not affected by the voltage at the input node. Finally, when S_1 and S_7 open, S_3 is already open, so there is no signal-dependent charge injection into C_1 and C_2 from S_1. Note that this circuit can function well with a large parasitic capacitor C_p at the input node of the op-amp, since it has neither any reset switch for the parasitic capacitor, nor any switch between C_p and the op-amp input node. There are several switches connected to the integrating capacitor C_2 or the holding capacitor C_3. Those switches create kTC charge noise. However, their effects are not increased by the large parasitic capacitor C_p.

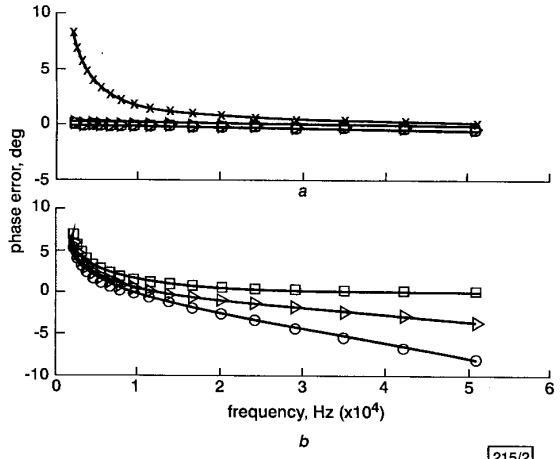

Fig. 2 *Phase error against frequency*

—□— proposed CDS integrator
—○— CDS integrator [4]
—▷— CDS integrator [5]
—×— uncompensated integrator
a Without parasitic capacitor
b With parasitic capacitor C_p = 20pF

Simulation result: The proposed CDS integrator (Fig. 1) and some previously published CDS circuits ([4], Fig. 2 and [5], Fig. 1) were simulated, along with a standard integrator without CDS for comparison. Since all simulated CDS integrators follow the rules described in the previous Section, the error charge due to resetting C_p and the kTC error-charge noise were not simulated here. The phase error due to the parasitic capacitor was simulated using SWITCAP2. We used an input capacitor C_1 = 0.2pF, a feedback capacitor C_2 = 1pF, and a holding capacitor C_3 = 1pF, as well as a clock frequency f_c = 1MHz and a DC gain A = 100 for all integrators. A parasitic capacitance C_p = 20pF was assumed.

Fig. 2*a* shows that each CDS circuit improves the phase error compared to a non-CDS integrator without the parasitic capacitance. Our proposed circuit, however, shows a better performance than [4] or [5] for phase error with large parasitic capacitors at the input nodes (Fig. 2*b*). Even for C_p = 2pF, the circuits described in [4, 5] give a large negative phase error. The reason why both CDS circuits have degraded performance when they have C_p is the following. In the circuit of [5], the holding capacitor and the parasitic capacitor are in parallel during the sampling phase, but they are in series during the charge transfer, which means that error charge flows through the holding capacitor, and this increases the phase error. Similarly, error charge flows in the circuit of [4] also. Note that our proposed CDS circuit improves the offset and $1/f$ noise performance also, and that the phase error performance is as good as for the uncompensated integrator.

Conclusion: A new CDS integrator has been proposed. It provides improved performance over earlier circuits, particularly when a large parasitic capacitance is present at the op-amp input. The new integrator is thus useful when large op-amp input devices are used for low noise applications, and/or in sensor interface circuits.

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Guaranteed recall of all training pairs for exponential bidirectional associative memory

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Several methods of guaranteeing the recall of all training pairs for exponential bidirectional associative memory are presented. If the minimum Hamming distance between patterns is known, the radix can be determined to provide a certain basin of attraction. Otherwise the statistical minimum distance can be applied. A weight learning algorithm based on a pseudo-relaxation algorithm is also developed to make all training pairs recallable with a small radix.

Introduction: Exponential bidirectional associative memory (eBAM), proposed by Jeng *et al.* [1], has been widely used in applications such as pattern recognition and data compression owing to its stability, exponential storage capacity, and high error-correction capability [2]. Moreover, eBAM is suitable for VLSI implementation using the exponential drain current dependence of an MOS transistor on the gate voltage in the subthreshold region. In the analogue eBAM design proposed in [3], the limited dynamic range requires an algorithm which searches the smallest radix, making all patterns recallable. The radix searching algorithm (RSA) proposed by Wang *et al.* [4] is computationally difficult although it includes a radix learning procedure which guarantees the recall of all training pairs. This Letter presents an equation which determines a radix for perfect recall by using deterministic and statistical minimum distance information. It also provides additional weight learning, which guarantees the recall of all training pairs with a radix smaller than that of the RSA. These methods are useful for the analogue as well as the digital design [5] of eBAM.

Radix determination: Assume that there are p stored pattern pairs $\{(\mathbf{x}^i, \mathbf{y}^i)\}_{i=1}^{p}$, where $\mathbf{x}^i \in \{-1, 1\}^n$ and $\mathbf{y}^i \in \{-1, 1\}^m$. Each bipolar element of the patterns is randomly generated with equal probability. The bidirectional recall process of the eBAM in one cycle is thus

$$\mathbf{y} = f(\mathbf{x}) = \mathrm{sgn}\left(\sum_{i=1}^{p} \mathbf{y}^i b^{\mathbf{x}^{iT}\mathbf{x}}\right) \tag{1}$$

$$\mathbf{x}' = g(\mathbf{y}) = \mathrm{sgn}\left(\sum_{i=1}^{p} \mathbf{x}^i b^{\mathbf{y}^{iT}\mathbf{y}}\right) \tag{2}$$

where $b > 1$ and $\mathrm{sgn}(u) = 1$ if $u \geq 0$ and $\mathrm{sgn}(u) = -1$ otherwise.

Applying a radius-r noisy pattern, $\bar{\mathbf{x}}^h \in \{\mathbf{x} | d_H(\mathbf{x}, \mathbf{x}^h) = r\}$, to the forward association (eqn. 1), $y_k^h y_k$ should be greater than zero $\forall h$ and $\forall k$:

$$y_k^h y_k = \mathrm{sgn}\left(b^{n-2r} + \sum_{i \neq h} y_k^h y_k^i b^{\mathbf{x}^{iT}\bar{\mathbf{x}}^h}\right) > 0 \tag{3}$$

A sufficient condition to satisfy the inequality (eqn. 3) is

$$\left|\sum_{i \neq h} y_k^h y_k^i b^{\mathbf{x}^{iT}\bar{\mathbf{x}}^h}\right| < b^{n-2r} \tag{4}$$

and the following inequalities hold:

$$\left|\sum_{i \neq h} y_k^h y_k^i b^{\mathbf{x}^{iT}\bar{\mathbf{x}}^h}\right| \leq \sum_{i \neq h} b^{\mathbf{x}^{iT}\bar{\mathbf{x}}^h} \leq (p-1) b^{n-2(s_h - r)} \tag{5}$$

where $s_h = \min_{\forall i \neq h} d_H(\mathbf{x}^i, \mathbf{x}^h)$ and $r < s_h/2$.

Now, equating the right-most terms of eqns. 4 and 12, the radix which guarantees direct attraction inside radius-r is obtained from the minimum Hamming distance:

$$b = (p-1)^{\frac{1}{2(s_{min} - 2r)}} \tag{6}$$

where $s_{min} = \min_{\forall h} s_h$ and $r < s_{min}/2$. Moreover, by choosing $b = (p-1)^{1/2}$, we can guarantee that all noisy patterns with $r < s_{min}/2$ are directly attracted without needing information regarding s_{min}.

The radix calculated using eqn. 6 is actually very large compared to that obtained from searching using the RSA. However, in low dimensional applications (small n and p) or digital implementation [5], the radix can be chosen instantly by investigating the minimum Hamming distance. A radix for the backward association (eqn. 2) can be obtained similarly.

Statistical minimum distance: If the minimum distance information is not available, the expected value can be used instead. Using the probability

$$\Pr(s_h = r) = \Pr(s_h \geq r) - \Pr(s_h \geq r+1) \tag{7}$$

$$= \left(\sum_{j=r}^{n} C_j^n / 2^n\right)^{p-1} - \left(\sum_{j=r+1}^{n} C_j^n / 2^n\right)^{p-1} \tag{8}$$

the expected value of the minimum Hamming distance is

$$E[s_{min}] = E[s_h] = \sum_{r=0}^{n} r \Pr(s_h = r) = \sum_{r=1}^{n} \left(\frac{\sum_{j=r}^{n} C_j^n}{2^n}\right)^{p-1} \tag{9}$$

$$< \sum_{r=1}^{n} \left(\frac{\sum_{j=0}^{n} C_j^n - \sum_{j=0}^{r-1} C_j^{r-1}}{2^n}\right)^{p-1} = \sum_{r=1}^{n} \left(1 - \frac{1}{2^{n-r+1}}\right)^{p-1} \tag{10}$$

$$\simeq n - (p-1)(1 - 2^{-n}) \tag{11}$$

Substituting one of these expected values into s_{min} in eqn. 6 is, statistically, one feasible solution, although recall of all training pairs is not deterministically guaranteed. If this method fails to attract some training pairs, the errors are compensated for by the following learning algorithm.

Learning algorithm: If we define $\mathbf{u}^h = [b^{\mathbf{x}^{1T}\mathbf{x}^h}, ..., b^{\mathbf{x}^{pT}\mathbf{x}^h}]$, the inequalities (eqn. 3) are converted to linear inequalities:

$$y_k^h \lambda_k^T \mathbf{u}^h > 0 \qquad \forall h, \forall k \tag{12}$$

where $\lambda_k = [y_k^1, ..., y_k^p]$. If the matrix $U = [\mathbf{u}^1] ... [\mathbf{u}^p]$ has full rank, we can find a solution $\lambda_k^{*T} = [y_k^1 \varepsilon, ..., y_k^p \varepsilon] U^{-1}$ for $\exists \varepsilon > 0$ by setting $y_k^h \lambda_k^T \mathbf{u}^h = \varepsilon \ \forall h$. This reflects the possibility of λ_k learning algorithm to satisfy eqn. 12 instead of the RSA. As radix b increases, U becomes similar to the identity matrix, and λ_k^* goes