ble, flanks instead of complete pulses are counted during the phase error. This enables use of the output from the NCO instead of implementing an extra oscillator. However, using flank counting and a faster oscillator gives a shorter lock time (step response) and less phase noise.

The circuit of Fig. 3 is used for gating a clock signal when 'EVENT' is low. The clock pulses at the output 'clk_out' are always complete pulses.

Two three bit counters are equipped with the circuit of Fig. 3. One counter is clocked with the gated version of the clock and the other counter is clocked with the gated version of the inverted clock. Fig. 4 is a simulation showing the 'EVENT' signal, the clock signal and the clock bursts counting up the two counters. The result from the two counters is then added to obtain the number of clock flanks during the phase error.

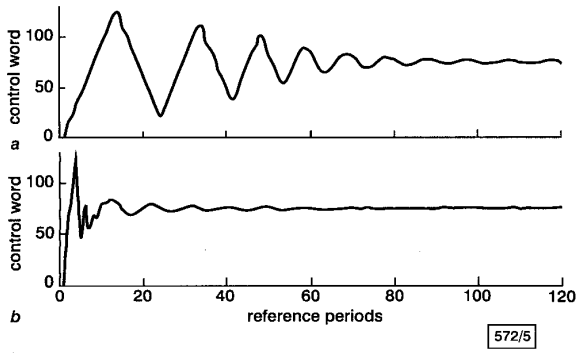

Fig. 5 *Step response*

a Before improvement
b After improvement

Since the counters are only three bit wide, they will often saturate during the initial phase of an impulse response. To achieve a faster impulse response and thereby a shorter lock time for the PLL, the output from the counters is multiplied by 4 whenever both counters are saturated. The effect of this is shown in Fig. 5, where the lower plot shows the improvement in step response.

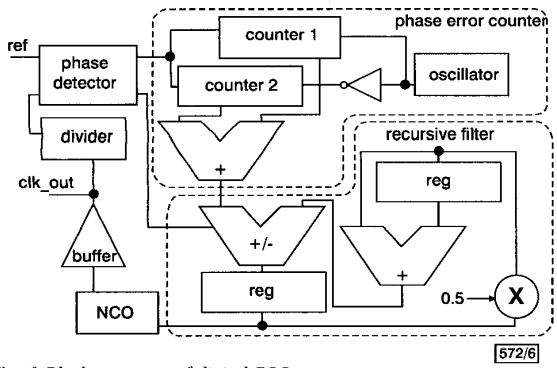

Fig. 6 *Block structure of digital PLL*

Design overview: Fig. 6 shows the block structure for the digital PLL. The phase detector is controlling the two counters, which in this configuration are clocked by an extra oscillator. The sum of the two counters is added to the output of the digital filter once each reference period. The output of the NCO is divided by the multiplication factor and then contrasted in phase to the reference.

Conclusions: A prototype of a standard-cell digital PLL clock multiplier is designed using a 0.35μm CMOS process. The digital PLL is designed for a frequency range of 170 to 360MHz and occupies 0.06mm^2 of on-chip area. Instead of a charge pump and an analogue filter, two three bit counters and a recursive digital filter are used as a loop filter. A numerically-controlled oscillator with high resolution is made from a ring oscillator with additional tri-state gates. The high resolution enables accurate frequency control and low phase noise. The digital PLL is implemented using cells found in an ordinary commercial standard cell library, which makes it portable between technologies in a netlist format.

30 November 2000
Electronics Letters Online No: 20010160
DOI: 10.1049/el:20010160

T. Olsson and P. Nilsson (*Department of Applied Electronics, Lund University, PO Box 118, SE-22100, Lund, Sweden*)

E-mail: ton@tde.lth.se

References

1 NILSSON, P., and TORKELSON, M.: 'A monolitic digital clock-generator for on-chip clocking of custom DSPs', *IEEE J. Solid-State Circuits*, 1996, **31**, (5), pp. 700–706
2 OLSSON, T., NILSSON, P., MEINCKE, T., HEMANI, A., and TORKELSON, M.: 'A digitally controlled low-power clock multiplier for globally asynchronous locally synchronous designs'. Proc. ISCAS'2000, Geneva, May 2000
3 BEST, R.E.: 'Phase-locked loops' (McGraw-Hill, 1984)

Switched-capacitor resonator structure with improved performance

M. Keskin, Un-Ku Moon and G.C. Temes

A novel switched-capacitor resonator circuit is proposed. Its centre frequency is insensitive to the finite bandwidth and gain of the opamps used.

Introduction: Bandpass ΔΣ modulators are used for the direct digitisation of the IF signals in wireless personal communication systems. They are usually implemented using switched-capacitor (SC) resonators [1 – 3]. These resonator circuits suffer from analogue circuit limitations when the clock frequency (f_{clk}) is high. The limitations include the finite unity-gain-bandwidth (f_u) and DC gain (A_{dc}) of the opamps used. If these two design parameters are not adequate, there will be both resonator gain loss and shift in the centre frequency location. The gain may be boosted with circuit techniques such as correlated-double-sampling (CDS) [4]; conversely, the shift in centre frequency will introduce large out-of-band noise into the desired signal band. Thus, it is desirable to have a resonator structure with a centre frequency that is insensitive to opamp nonidealities. The novel architecture proposed herein has two integrating paths. Hence, we named it integrating-2-path (I2P) structure. Its performance is contrasted, below, with three other well-known SC resonator structures, i.e. the pseudo-N-path (PNP) [1], the two-delay loop (TDLL) proposed by Longo and Hong [2], and the two-delay loop (TDLB) by Bazarjani and Snelgrove [3].

Resonator transfer function: The ideal transfer function of the resonator discussed is

$$H(z) = \frac{z^{-1}}{1 + z^{-2}} \tag{1}$$

This translates into the input-output relation; $v_o(n) = v_{in}(n-1) - v_o(n-2)$. Nonidealities of the opamp act to modify $H(z)$ into

$$H(z) = \frac{(1-a)z^{-1}}{(1-d) + bz^{-1} + (1-c)z^{-2}} \tag{2}$$

The peak gain loss results from error terms c and d, which affect the quality factor Q of the resonance peak. The shift in centre frequency is introduced by the error term b. The error term a also introduces a gain loss but this is very small contrasted to that caused by terms c and d.

Resonator structures: The I2P circuit is shown in Fig. 1. In this structure, the differential voltage occurring two clock periods before is stored in the C_1 capacitors during odd clock phases. This pair is then interchanged in the next clock phase to realise the resonator transfer function. The same operation is performed by the other pair (C_2) in even clock phases. This operation prevents the introduction of odd-order terms in the denominator of $H(z)$ and the mixing of the gain and leakage errors. The actual transfer function becomes

$$H(z) = \frac{(1-a)\cdot z^{-1}}{1+(1-c)\cdot z^{-2}} \quad (3)$$

The error term a is due to the forward path of the resonator, while the error term c is introduced in the feedback path. Detailed analysis shows that the PNP, the TDLB and the TDLL have larger error terms, and the actual transfer function is given by eqn. 2.

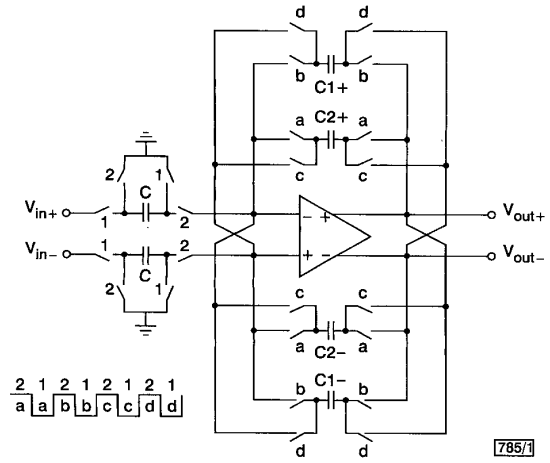

Fig. 1 *Proposed integrating-two-path resonator*

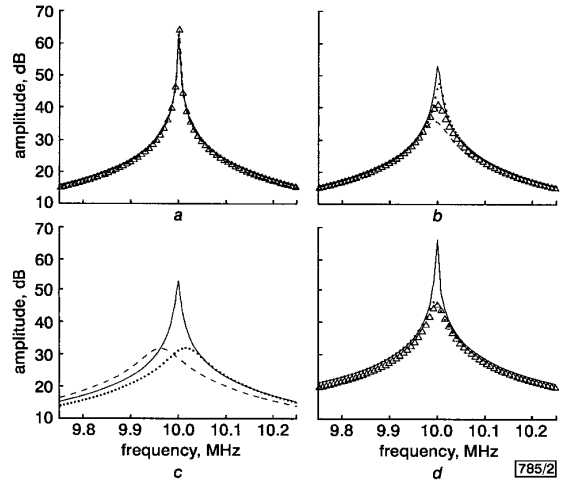

Fig. 2 *Simulation results from SWITCAP2*

a A_o = 120dB, $f_u = \infty$ and f_{clock} = 40MHz
b A_o = 60dB, $f_u = \infty$ and f_{clock} = 40MHz
c A_o = 120dB, f_u = 160MHz and f_{clock} = 40MHz
d A_o = 120dB, f_u = 100MHz and f_{clock} = 20MHz
——— I2P
····· P2P
– – – – TDLL
△ TDLB

Simulation results: The simulation results obtained using SWITCAP2 are shown in Fig. 2. The peak resonances of four resonators occur at $f_s/4$ in Fig. 2*a* for the (nearly) ideal case with $f_u = \infty$ and A_o = 120dB. In Fig. 2*b*, the effects of the finite gain limitation of the opamp are shown, with $f_u = \infty$ and A_o = 60dB. The I2P has some peak gain loss, less than the others, and no centre frequency shift. P2P and TDLL have both gain loss and frequency shift. In Fig. 2*c*, the effects of the finite bandwidth of the opamp are shown with f_u = 160MHz, A_o = 120dB, and f_{clk} = 40MHz. The I2P has a 10dB gain loss but it is 20dB better than the P2P and TDLL. In addition, P2P and TDLL also have a 50kHz frequency shift. In this simulation, TDLB was not shown because of its inherent double-sampling feature. Fig. 2*d* compares I2P, P2P and TDLB when A_o = 120dB, f_u = 100MHz, and f_{clk} = 20MHz (double sampling) are used. As seen from the Figure, I2P is again 20dB better than the other two. Note that TDLB does not show any centre frequency shift, but it suffers from severe gain loss. In this simulation, the TDLL could not be shown, since its opamps are used in both phases.

Second-order effects: There are second-order effects in the I2P owing to the four signal paths. Random mismatches (1%) between capacitors will introduce mirror images in the passband. From the SWITCAP2 simulations, it appears that the mirror image in the I2P structure is 80dB lower than the input signal, compared to typical –40dB level tones in any double-sampling structures. The suppression is due to the swapping of capacitors in the I2P operation. Another second-order effect is due to the offset voltage and $1/f$ noise. These will be shifted to the centre frequency, since I2P uses clock signals with $f_s/4$ frequency. Implementing the CDS technique in the architecture with four additional holding capacitors cancels the effects of offset voltage and $1/f$ noise. We simulated a fourth-order bandpass $\Delta\Sigma$ modulator with 1% capacitor mismatches and with 12mV offset voltage. The SWITCAP2 simulation showed that there is a mirror image owing to path mismatches. In addition, there is a tone at the centre frequency. When the CDS technique was implemented, the SFDR was restored to 80dB.

Conclusions: A novel SC resonator is proposed and contrasted with three other resonator structures. This new architecture allows the use of higher clock frequency without suffering from finite opamp bandwidth effects. It also alleviates the finite gain effects.

16 October 2000
Electronics Letters Online No: 20010158
DOI: 10.1049/el:20010158

M. Keskin, Un-Ku Moon and G.C. Temes (*Department of Electrical and Computer Engineering, Owen Hall, Oregon State University, Corvallis, OR 97331-3211, USA*)

E-mail: keskin@ece.orst.edu

References

1 SCHREIER, R., TEMES, G.C., YESILYURT, A.G., ZHANG, Z.X., CZARNUL, Z., and HAIRAPETIAN, A.: 'Multibit bandpass delta-sigma modulators using pseudo-N-path structures'. ISCAS Dig., 1992, pp. 593–596
2 LONGO, L., and HONG, B.-R.: 'A 15b 30kHz bandpass delta-sigma modulator'. ISSCC Dig., 1993, pp. 226–227
3 BAZARJANI, S., and SNELGROVE, W.M.: 'A 160-MHz fourth-order double-sampled SC bandpass sigma-delta modulator using half-delay integrators', *IEEE J. Solid-State Circuits,* 1998, **SC-45**, pp. 547–555
4 BETTS, A.K., and TAYLOR, J.T.: 'Finite-gain-insensitive circulating-delay type pseudo-N-path filter', *Electron. Lett.,* 1990, **23**, pp. 1941–1942

Application of PML to open boundary problem using TLM method

G.N. Mulay and K.S. Jog

Numerical results obtained by directly applying the perfectly-matched layer (PML) to an open boundary problem, i.e. the calculation of PCB crosstalk using the TLM, are presented. While evanescent waves cannot be absorbed even by a large number of PML layers, a single layer is sufficient provided it is placed sufficiently far away.

Introduction: Recently, several direct and indirect methods of applying the perfectly-matched layer (PML) absorbing boundary condition (ABC), originally developed for the finite-difference time-domain (FDTD) method, to the transmission line matrix (TLM) method have been reported, mostly for closed structures [1, 2].

This Letter describes the simulation results obtained by applying the direct method proposed in [1] to a typical open-boundary problem, i.e. modelling of crosstalk between tracks in a module-on-backplane arrangement.