

# Frequency detector for fast frequency lock of digital PLLs

V. Kratyuk, P.K. Hanumolu, U.-K. Moon and K. Mayaram

A new frequency detector, which allows for a fast frequency lock of phase-locked loops (PLLs), is presented. It uses the feedback divider that already exists in a PLL to determine the frequency difference. The proposed frequency detector provides frequency difference information at each reference cycle, and thus guarantees fast frequency acquisition.

**Introduction:** A wide tuning range for a PLL can be achieved by incorporating a frequency-locked loop (FLL) in parallel with the PLL. The key building block of an FLL is the frequency detector (FD) that determines the difference between the oscillator's divided clock (CKV) and the reference clock (REF). There are many ways to accomplish frequency lock in digital PLLs, but all of them suffer from a major drawback—slow frequency acquisition. In [1] an up-down counter (UPD) triggered by the edges of REF and CKV was used for frequency acquisition. The advantage of this method is that the up-down counter serves not only as a frequency detector but also as an accumulator, and thus it can directly control a digitally controlled oscillator (DCO) without the need for additional hardware. Another way to design an FD is to use two separate counters to count edges of the oscillator's divided clock and the reference clock [2]. The values in those counters are compared after a certain number of reference periods, which makes it extremely slow. The frequency locking capability can be incorporated into a phase-locked loop by using a phase-frequency detector (PFD) [3]. This approach is simple to implement but also suffers from slow frequency acquisition. In this Letter, a new frequency detector, which allows for fast frequency locking of digital PLLs, is described.

**Operation of new frequency detector:** The frequency detector uses the divider that usually exists in the feedback path of a PLL. The operation of the frequency detector is based on the observation that the feedback divider is an asynchronous counter, which counts the edges in the oscillator output. By sampling the value of this counter at each reference cycle and postprocessing the obtained data, the frequency difference can be determined.

A simplified block diagram of the proposed frequency detector is shown in Fig. 1. It consists of a PLL's feedback divider, two registers, and a modulo arithmetic adder. The feedback divider in a PLL divides an oscillator's frequency by  $2^N$  and is a modulo- $2^N$  counter, where  $N$  is the number of divide-by-two stages. It counts from zero to  $2^N - 1$ , and then rolls back to zero. The value of the feedback divider counter is sampled on each rising edge of the reference clock. Since the DCO output is not synchronous with the reference, the reference clock has to be re-sampled with a DCO edge. The feedback divider (counter) changes states upon arrival of the DCO rising edges. To allow the counter to settle, the falling (not rising) edge of the DCO has to be used for re-sampling. Various re-sampling techniques can be used in this design to reduce the possibility of entering a metastable state. The simplest solution is to employ two cascaded flip-flops in the reference clock re-sampling. In Fig. 1, register 1 stores the recent value of the counter (R1), while register 2 stores the value of the previous sample (R2). The difference between these two registers defines how many full DCO periods are in one reference period ( $T_{REF}/T_{DCO}$  or  $F_{DCO}/F_{REF}$ ). The  $F_{DCO}/F_{REF}$  ratio is determined by subtracting the value of the second register R2 from the value of the first register R1 using modulo- $2^N$  arithmetic. To widen the frequency detection range, the counter can have more stages (denoted by  $M$  in Fig. 1) than those required for the DPLL feedback divider (denoted by  $N$  in Fig. 1). The divided oscillator clock  $F_{CKV}$  is taken after  $N$  stages in this case. The digital output of the frequency detector  $D_{OUT}$  is given by (1), where the subtraction from  $2^N$  ensures that in the lock condition the  $F_{DCO}/F_{REF}$  ratio is exactly equal to  $2^N$ :

$$D_{OUT} = 2^N - \frac{F_{DCO}}{F_{REF}} = 2^N - (R1 - R2) \text{ mod } 2^M \quad (1)$$

The proposed frequency detector can operate with an arbitrary low DCO frequency that can be even less than the reference frequency. In

this case two consecutive counter readings might be the same, and thus the upper limit of  $D_{OUT}$  is  $2^N$ . The detection of high DCO frequencies is limited by the counter maximum value, which is  $2^M - 1$ . Thus the lower limit of  $D_{OUT}$  is  $2^N - 2^M + 1$ . The limits for the FD digital output  $D_{OUT}$  and  $F_{DCO}/F_{REF}$  ratio are summarised by (2) and (3), respectively:

$$2^N - 2^M + 1 \leq D_{OUT} \leq 2^N \quad (2)$$

$$0 \leq \frac{F_{DCO}}{F_{REF}} \leq 2^M - 1 \quad (3)$$

**Suggested frequency synthesiser architecture:** The proposed frequency detector can be used in a frequency synthesiser as shown in Fig. 2. The frequency synthesiser consists of two loops: a frequency-locked loop and a phase-locked loop, and a lock detector (LD). Frequency detection in the FLL is accomplished by the FD. The output of the FD  $D_{OUT}$  is accumulated by a digital accumulator (ACC). The output of the ACC can be interfaced with an oscillator by using a digital-to-analogue converter. The LD detects frequency lock, freezes the FLL and activates the PLL that accomplishes phase locking.

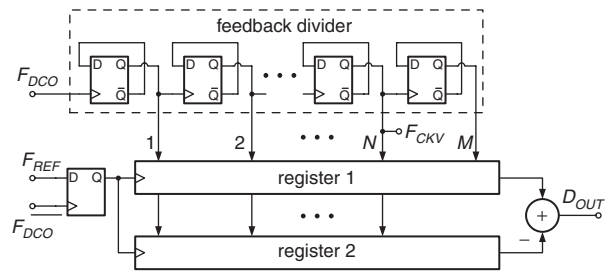


Fig. 1 Proposed frequency detector

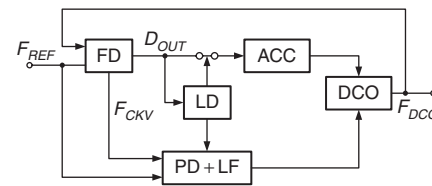


Fig. 2 Suggested PLL architecture; phase detector (PD) and loop filter (LF) are used for phase-locking

The stability of the FLL with the proposed frequency detector was analysed using a z-domain model, as shown in Fig. 3. The input of the system is the reference frequency  $F_{REF}$ , which is assumed to be constant, and the output of the system is the oscillator frequency  $F_{DCO}$ . From Fig. 3, the oscillator frequency is given by:

$$F_{DCO} = -\frac{F_{DCO}}{F_{REF}} K_{DCO} \frac{z^{-1}}{1 - z^{-1}} + N K_{DCO} \frac{z^{-1}}{1 - z^{-1}} \quad (4)$$

To simplify derivations, the  $F_{DCO}/F_{REF}$  ratio was not treated as an integer number. The transfer function of the FLL can be derived from (4) and is:

$$\frac{F_{DCO}}{F_{REF}} = \frac{N(K_{DCO}/F_{REF})}{z + ((K_{DCO}/F_{REF}) - 1)} \quad (5)$$

Equation (5) shows that the FLL is a one-pole system. Therefore, it is stable if the only pole is located inside the unit circle. The stability criteria obtained from (5) is given by:

$$0 < K_{DCO} < 2F_{REF} \quad (6)$$

This inequality can be easily satisfied in the design of an FLL.

**Simulation results:** An FLL with the proposed frequency detector was implemented and compared to the FLLs with existing frequency-locking techniques. Three FLLs have been implemented: (i) with the proposed frequency detector; (ii) with an up-down counter as a frequency detector; and (iii) with a PFD embedded in a bang-bang digital PLL. All FLLs have been designed for the same reference frequency, oscillator free-running frequency and DCO resolution. The

results from Simulink simulations are shown in Fig. 4, which shows the outputs of the loop filters of all three FLLs. As can be seen from Fig. 4, the FLL with the new FD approaches the lock state very quickly. It locks to the required frequency approximately 2.5 times faster than the PLL with a PFD and almost 8 times faster than the FLL with the up-down counter.

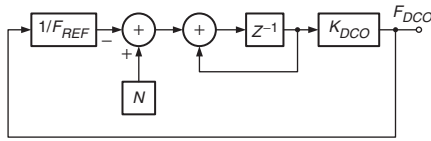


Fig. 3 z-domain model of FLL

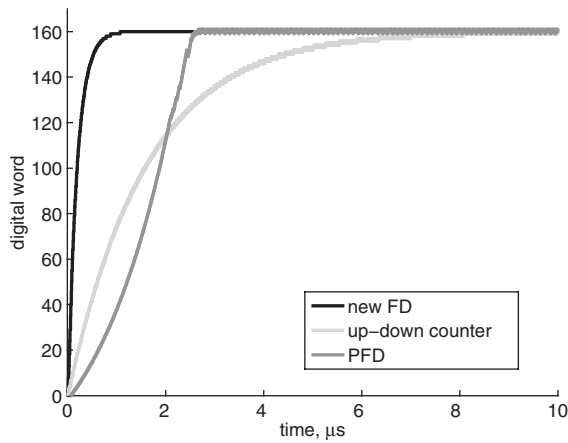


Fig. 4 Loop filter output

**Conclusions:** A new frequency detector has been proposed, which allows for fast frequency locking of a PLL. It uses the feedback divider that already exists in a PLL to determine a frequency difference. The proposed frequency detector can be implemented by using standard logic available in any process and, therefore, is suitable for digital as well as for analogue PLLs.

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