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High-speed ΔΣ ADC with error correction

P. Kiss, U. Moon, J. Steensgaard, J.T. Stonick and G.C. Temes

A digital error correction scheme is described for ΔΣ ADCs with multibit quantisers. It operates in the background and remains effective even for very low oversampling ratios.

Introduction: The use of multibit quantisers in delta-sigma (ΔΣ) analogue-to-digital converters (ADCs) has great advantages over single-bit ones, such as increased signal-to-noise ratio (SNR), relaxed opamp specifications, improved stability, etc. However, the performance bottleneck is usually the linearity of the internal digital-to-analogue converter (DAC), which needs to be at least as good as that of the overall ADC. Off-line [1, 2] as well as on-line [3] digital calibration, and mismatch shaping [4 – 6] have been used to solve this problem for operation with a large oversampling ratio (OSR). An analogue correction technique was also recently proposed [7].

In this Letter, a digital on-line correction method is described. Unlike earlier techniques, it remains effective for low oversampling ratios. It is also able to follow drift caused, e.g. by temperature variations during operation.

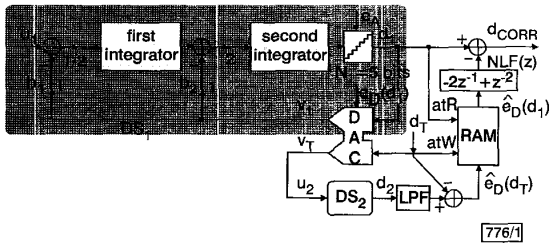

Fig. 1 *Delta-sigma ADC with error correction*

Correction system: A second-order ΔΣ ADC (DS_1) will be used to illustrate the proposed correction technique. As shown in Fig. 1, the internal DAC has two outputs: v_1 is input to the loop filter, and v_T is input to the calibration ADC (DS_2). The calibration ADC is used to derive a digital estimate, $\hat{e}_D$, of the DAC errors, e_D, for all output levels and stores these in a RAM. During conversion, internal DAC errors are corrected by filtering the RAM outputs via the FIR filter $NLF(z)$ and subtracting the result from the digital output d_1 of DS_1. The details of the acquisition process for $\hat{e}_D$, and the analysis of the system, are given in the following Section.

The system shown in Fig. 1 assumes that a single DAC provides feedback signals to both integrators. Mismatch of coefficients b_1 and b_2 does not affect the linearity of the system.

It should be noted that the nonlinearity errors of the internal ADC are not corrected by the system. However, these are suppressed by the same noise transfer function as the quantisation noise (typically, $(1 - z^{-1})^2$ for a second-order ΔΣ ADC), and hence rarely present a problem. However, this may be insufficient when very low OSR is used, and high linearity is required. In this case, a second stage (as in the MASH configuration) may be added, or ADC element mismatch shaping [8] may be used.

Correction process: The on-line acquisition of the actual DAC output level errors can be tailored to the DAC structure. If the DAC can provide multiple inputs and outputs, such as the resistor-string DAC described in [1], then the off-line calibration proposed in [1] can be transformed into a background process. In that case, a digital calibration signal d_T will provide a staircase waveform sequentially providing every possible input to the DAC. Each DAC output level v_T is converted to digital form d_2 by the calibration ΔΣ converter DS_2, and lowpass filtered by LPF (Fig. 1) to remove the quantisation noise of DS_2. Then, d_T is subtracted to recover the level errors e_D in a digital representation. The estimates $\hat{e}_D$ thus obtained are stored in the RAM, and recalled for each output d_1 to correct it. During operation, the calibration can be periodically repeated to track any drift in the DAC output levels, e.g. due to temperature effects.

For low oversampling ratios and for low-order loop filters, the transfer function from the DAC output v_1 to the output d_1 of DS_1 cannot be approximated accurately by $NLF(z) = -1$, as was done in [1, 3]. The RAM output needs to be filtered by the actual $NLF(z)$ (here, $-2z^{-1} + z^{-2}$) to achieve accurate error cancellation, as shown in Fig. 1.

In some DAC implementations, N equal-valued unit elements (current sources, capacitors, resistors, etc.) are used. The algorithm described above may still be used [Note 1], if $N + 1$ elements are implemented in the DAC, and their errors are measured sequentially one-by-one using DS_2. Alternatively, the output signal d_1 may be used also as the calibration signal d_T. For a d_1 value calling for the use of n unit elements to produce v_1, the remaining $N - n$ unit elements are utilised to generate v_T. If, as is usual, DAC gain and offset errors are acceptable, so that the sum of all unit-element errors can be regarded as zero, then the error present in v_T is the negative of that in v_1. Hence, by sorting the analogue samples in v_T into channels, with one channel dedicated to each possible input (d_1) code and its complement (full scale code - d_1), DS_2 can be used to produce the digital form of the individual DAC levels. The operation of DS_2 can easily be multiplexed among the channels, with only the memoried elements (feedback capacitors) replicated for each DAC level.

For linear operation, the calibration ADC (DS_2) must itself be highly linear. This may require the use of a single-bit internal quantiser in DS_2. However, linear effects (gain and offset errors) are acceptable in DS_2 because the DAC nonlinearity information is preserved. Also, the matching errors between the actual DAC error transfer function (from v_1 to d_1) and its digital replica $NLF(z)$ (Fig. 1) can be shown to have only a minor effect on the linearity of the overall conversion.

Simulation results: The operation of the digitally corrected ADC shown in Fig. 1 was simulated under the following conditions. 5 bit (32 level) internal ADC and DAC were assumed, with a 0.1%

Note 1: This method was suggested by Professor G. Cauwenberghs of Johns Hopkins University.

linear gradient error in the DAC. This corresponds to a midrange error of 0.4%. Finite (54dB) DC gain for all opamps and randomly mismatched capacitors (with 0.1% standard deviation) were assumed in all circuits. OSR = 4 was used. A 0.45V peak midband two-tone input signal u_1 was applied to DS_1, and a second-order single-bit ΔΣ ADC realised DS_2. To demonstrate the high linearity achievable with the proposed correction, DS_1 was embedded in a 2-0 MASH containing a 10 bit ADC as its second stage. The mismatch between the MASH stages was not considered; it can also be corrected by digital methods [9].

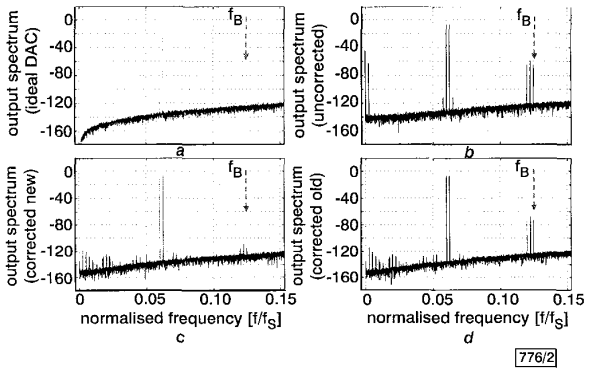

Fig. 2 *Output spectra of MASH (computed using 64× averaged FFTs for 2^{15} samples)*

a For ideal DAC
b For nonlinear DAC without correction
c For nonlinear DAC with proposed correction
d With correction, but using $NLF(z) = -1$
– – – $f_B = f_S/8$, inband limit for OSR = 4

The computed spectrum of the system operating with an ideal DAC but with nonideal opamps and capacitors (described above) is shown in Fig. 2*a*. Fig. 2*b* shows the spectrum using the nonlinear DAC without error correction. Large harmonics are generated and the spur-free dynamic range (SFDR) is only 52dB. Fig. 2*c* shows the result when using the digital correction described in this Letter; an SFDR > 100dB was achieved. To obtain sufficiently accurate estimates of e_D needed for such a high SFDR, DS_2 processed 2^{18} samples for each level of the DAC (a complete background calibration cycle then needs about 4s if DS_2 is clocked with f_S = 5MHz). Finally, Fig. 2*d* shows the detrimental effect of using $NLF(z) = -1$ (as carried out in earlier work [1, 3]), the drop in the SFDR being from 101 to 60dB.

Conclusions: An on-line digital correction method was proposed for ΔΣ ADCs with multibit internal quantisers. It is applicable even for ADCs with very low oversampling ratios, where the commonly used mismatch-shaping techniques become less effective. Simulations indicate that excellent linearity can be obtained using the proposed process.

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Reconfigurable phase-locked loops on FPGA utilising intrinsic synchronisability

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A new digital phase-locked loop (PLL), utilising the intrinsic synchronisability of electrical oscillators, on a field-programmable gate array has been developed. By interconnecting such PLLs, a dynamically reconfigurable clock network was formed, which has been difficult with conventional PLL techniques.

Introduction: Digital LSIs have generally been based on a synchronous scheme in which a global clock signal is distributed throughout the chip. However, circuit size and clock frequencies are increasing, therefore it is harder to distribute the clock signal (hereafter 'the clock') within an allowable phase delay. Asynchronous circuit design or locally synchronous circuits is a reasonable way to avoid this difficulty. Clock networks using distributed voltage-controlled oscillators [1, 2] can also be used. In contrast to these designs, we have developed a new digital phase-locked loop (PLL) which was tested on a field-programmable gate array (FPGA). This PLL utilises intrinsic synchronisability of electrical oscillators, and it can be simply implemented on an FPGA. It can provide dynamically reconfigurable clock networks, which have not been realised by conventional PLL techniques.

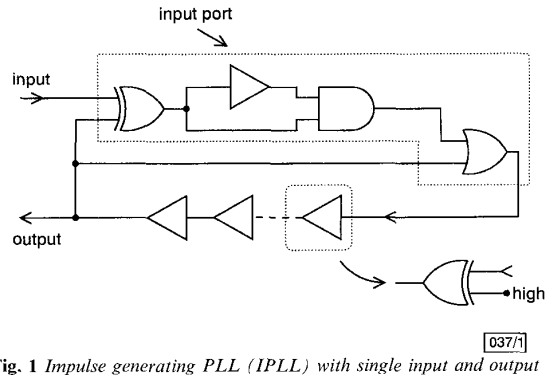

Fig. 1 *Impulse generating PLL (IPLL) with single input and output*

Impulse generating PLL (IPLL): Experimental results on the distributed clock oscillators for high-performance circuits show they have some advantages over conventional (H-tree like) clock networks [1, 2]. Such distributed oscillators are based on the conventional PLLs and require analogue elements in the circuits. We