Synthesis of PLA core: The PLA core has been synthesised from behavioural VHDL using the Synopsys Design Analyzer and Alcatel's 0.35 μm MTC45000 technology library. To determine the scalability of our PLA core, the architecture was synthesised at clock frequencies of 10, 25, 50, 80, 90 and 100 MHz, with all data widths set at 16 bits. These frequencies were chosen to reflect typical timing constraints required on high speed SoC bus architectures, which range from 60 to 100 MHz. The resulting logic area (in NAND gates) can be seen in Fig. 4. The area remains relatively constant up to 50 MHz. Between 50 and 100 MHz area increase is approximately linear. For technologies smaller than 0.35 μm, faster throughput could be achieved.
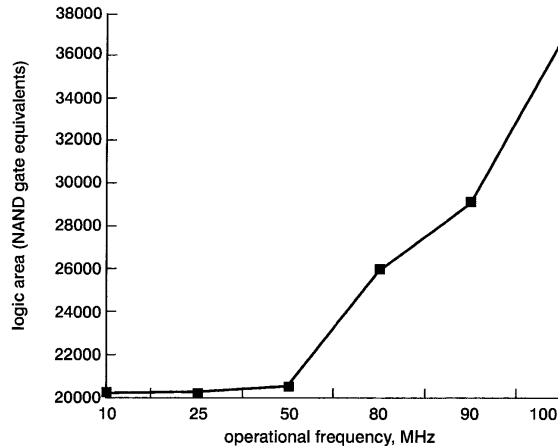

Fig. 4 *Logic area of PLA core against synthesis for increasing operational speeds*

■ synthesised area

Conclusions: We have presented a novel, high performance programmable logic array for the implementation of multiplierless digital filters. Coefficients are generated within a distributed, highly parallel architecture providing component redundancy, desirable in fault tolerant applications. High data throughput is achieved at speeds of up to 100 MHz and with a latency of seven clock cycles.

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Wideband low-distortion delta-sigma ADC topology

J. Silva, U. Moon, J. Steensgaard and G.C. Temes

A ΔΣ topology with reduced sensitivity to opamp nonlinearities is described. The technique is effective even for very low oversampling ratios, and can be used for any modulation order. Techniques for reducing other nonideal effects are also proposed.

Introduction: ΔΣ ADCs have been used predominantly in low bandwidth applications such as digital telephony and digital audio [1]. These applications rely on high oversampling ratios, typically between 32 and 256, to achieve the desired SNR and linear performance.

With the continuing advancement of technology, oversampled data conversion is becoming attractive for use in wideband applications, such as in xDSL modems and digital video. However, at very low oversampling ratios (for example, 4 or 8) required for such applications, these ADCs are increasingly sensitive to circuit imperfections, and require high-quality analogue components.

In this Letter, a second-order ΔΣ topology with low sensitivity to integrator nonlinearities is described. The technique is effective for any oversampling ratio, and can be applied to ΔΣ topologies of any order.
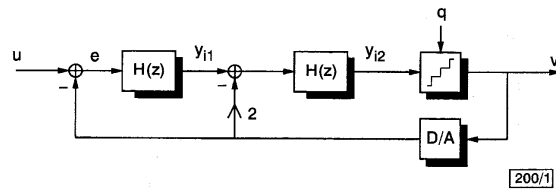

Fig. 1 *Traditional topology*

Distortion in traditional topology: Fig. 1 shows the topology of a traditional second-order ΔΣ modulator. The integrator blocks, denoted by $H(z)$, are typically realised as forward-Euler structures, i.e.:

$$H(z) = \frac{z^{-1}}{1 - z^{-1}} \qquad (1)$$

In this structure, the quantisation noise q is filtered by a second-order highpass function. The signal transfer function, from the input u to the output v, is just a delay of two clock cycles, so $STF(z) = z^{-2}$.

The way distortion is created and processed in this topology will be explained next. The error signal e is the difference between the input u and the output v, and the ΔΣ loop tries to minimise this difference in the desired frequency band. However, the delay introduced by the STF causes e to contain a highpass-filtered version of the input signal u, which is restored to its full amplitude by the integrators. Because of nonlinear opamp gain and slew-rate effects, harmonic components of the input signal are created at the outputs of the integrators, in y_{i1} and y_{i2}, and will appear at the output of the modulator in v, shaped by first- and second-order highpass transfer functions, respectively. The attenuation provided is satisfactory if a high oversampling ratio is used. For example, if $OSR = 128$, harmonics in y_{i1} are reduced by at least 32.2 dB. However, if $OSR = 8$, the attenuation is only 8.2 dB. In wideband applications, where high-speed analogue processing blocks are required, designing a sufficiently low distortion opamp to deal with this problem can be impractical.
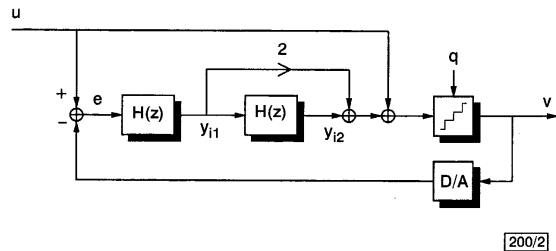

Fig. 2 *Proposed reduced distortion topology*

Proposed topology: The nonlinearity problem can be solved by cancelling the transfer functions from u to y_{i1} and y_{i2}. This is achieved by making $STF(z) = 1$.

One possible implementation is shown in Fig. 2 [1, 2]. The noise transfer function is unaffected, but the integrators will now process quantisation noise only. Therefore, their performance requirements can be significantly relaxed. Another advantage is that only one DAC is required in the feedback loop. For multibit quantisation, this reduces the circuit complexity and chip area significantly.

The described concept can be extended to noise-shaping of any order. The only requirement is to make the signal transfer function *STF* exactly equal to 1, without changing the noise transfer function.

In practice, the cancellation of u and v will not be perfect. As indicated before, v is an estimate of u, and its accuracy depends on the matching of electrical parameters. Hence, there will be some residual signal component in e and at the outputs of the integrators, but this will be normally negligible.
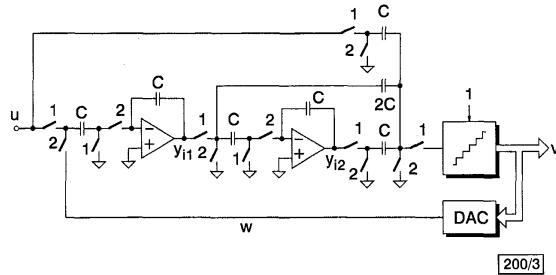

Fig. 3 *Circuit diagram implementation*

Circuit level implementation: The forward paths in Fig. 2 can be implemented by connecting a passive switched-capacitor network to the input of the quantiser. This network can also be used to apply a dither signal, an essential feature at low oversampling ratios. A complete circuit diagram, shown in single-ended form for simplicity, is shown in Fig. 3.

In practice, there will always be a small delay between u and v. However, as it will be explained next, this delay can be cancelled. The input signal u is sampled by a non-inverting (delaying) SC branch during phase Φ_1, and integrated during phase Φ_2 when the feedback signal w is entered using an inverting (non-delaying) branch in the DAC. The quantiser evaluates the input signal at the end of Φ_1, and provides the feedback signal during Φ_2. The end result is that there is no effective delay between the input signal sample which the first integrator is processing and the feedback signal associated with that sample.
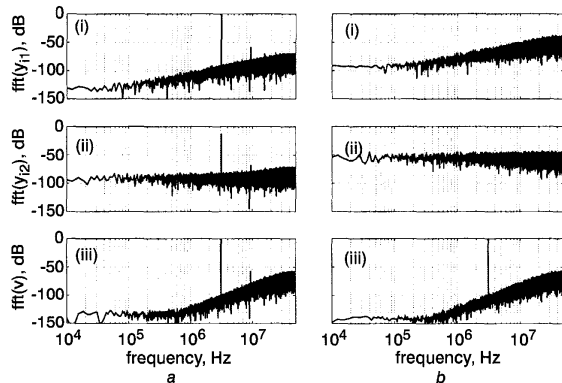

Fig. 4 *Simulation results for the traditional and proposed topologies*

a Traditional topology
b Proposed topology
(i) spectrum of $y_{i1}(n)$
(ii) spectrum of $y_{i2}(n)$
(iii) spectrum of $v(n)$

Simulation results: The proposed structure, shown in Fig. 2, was simulated with MATLAB and its linearity performance compared with that of the traditional scheme (Fig. 1). The model used for the integrators incorporated a nonlinear opamp input-output transfer curve, in the form of a hyperbolic tangent with a maximum gain of 50 dB.

Both structures were simulated with a sampling frequency of 100 MHz, a 6 bit quantiser, and with a uniformly distributed random dither signal. The sine-wave input signal u had an amplitude 0.9 V (for a voltage reference of 1 V) and a frequency 3.125 MHz. Scaling factors were included in each structure to ensure that the integrator output voltages were comparable.

The spectra of the signals $y_{i1}(n)$, $y_{i2}(n)$ and $v(n)$ for the two topologies were computed using 32768-point FFTs, and are shown in Fig. 4. The traditional topology shows the presence of input signal at the integrator outputs, together with harmonics created due to the nonlinear function. The modulator output v shows a third harmonic with an amplitude of –57.3 dBc. The proposed topology shows only shaped quantisation noise at these nodes (and therefore no harmonics of the input signal), and so the modulator had an undistorted output.

Note that both simulations show an increased noise floor compared to the ideal response. Part of this is caused by finite opamp gain. The other part is caused by the nonlinearities, which fold energy from high-frequencies down into the signal band. However, due to the absence of signal components, the proposed topology has a lower noise floor.

Additional remarks: The nonlinearities of the DAC in the feedback path are not addressed by the proposed topology. Analogue mismatch correction [3] can be used to linearise the DAC independently of the oversampling ratio.

The proposed structure can be used as the first stage of a cascaded $\Delta\Sigma$ structure. Since the quantisation noise is processed separately from the input signal, it can be tapped directly from the output of the second integrator, y_{i2}. This configuration has the added advantage of cancelling the quantiser (ADC) nonlinearities in the output v.

Conclusions: A $\Delta\Sigma$ topology with reduced sensitivity to nonlinear opamps has been described. The technique is effective for any oversampling ratio, and can be applied to any modulator order.

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Iterative FEM for characterising radiating slot in broad wall of rectangular waveguide

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It is shown that the iterative finite element method with the radiation-type boundary condition can give an efficient and accurate solution to the radiation problem. The proposed method is applied to the characterisation of a radiating slot on the broad wall of a rectangular waveguide. The result is compared with those of other conventional methods, and shows a good agreement.

Introduction: Recently an efficient iterative finite element method (iterative FEM) has been proposed [1], applied to a two-dimensional scattering problem [2], and extended to the characterisation