Parallel correlated double sampling technique for pipelined analogue-to-digital converters

T. Musah, B.R. Gregoire, E. Naviasky and U.-K. Moon

A new correlated double sampling technique that avoids the additional thermal noise penalty is presented. The new technique employs a low-gain two-stage opamp with the second stage made up of multiple gain stages in parallel. The superior noise performance of the proposed technique to correlated double sampling is shown.

Introduction: In a switch-capacitor realisation of the multiplying digital-to-analogue converter (MDAC) used in algorithmic and pipeline analogue-to-digital converters (ADCs), the settling behaviour of the opamp determines the speed and accuracy of the ADC. Fast settling requires high unity gain bandwidth, while accurate settling requires a high DC gain. As gate lengths continue to shorten, high gain opamp design becomes complex and thus limits the speed of the ADC. One way of overcoming this limitation is by designing a low-gain, high-speed opamp and using correlated double sampling (CDS) to double the effective gain (in dB) [1]. However, the CDS technique increases the kT/C noise power of the ADC [2], requiring larger capacitance values. The proposed MDAC structure allows use of a low-gain opamp to achieve high settling accuracy without the noise penalty.

Parallel correlated double sampling technique: Fig. 1 shows a conceptual realisation of the parallel correlated double sampling (PCDS) technique using two parallel second stages. The MDAC is configured for a 1.5 bit pipeline stage. The input signal (V_i) is sampled onto C_s and C_f during ϕ_1. The amplification phase, ϕ_2, is split into two phases ϕ_{21} and ϕ_{22}. During ϕ_{21}, the first stage and the upper second stage are in closed loop. The output voltage settles with a settling accuracy similar to that of an opamp with a gain of $A_1A_2/2$, where A_2 is G_mR_o. When ϕ_{21} opens and ϕ_{22} closes, C_P maintains the previous output current. The lower second stage needs only to settle to the error voltage from the previous phase and it does so with a settling accuracy similar to that of an opamp with a gain of $A_1A_2/2$. At the end of the amplification phase, the MDAC settles to the output voltage with an accuracy equivalent to using an opamp with a gain of $(A_1A_2/2)^2$. This can be extended to more parallel gain stages with the effective gain expressed as $(A_1A_2/n)^n$, where n is the number of second stages in parallel. The output voltage at the end of ϕ_{2n} when n parallel second stages are used is

$$V_o = \left(1 - \left(\frac{1}{1+A\beta}\right)^n\right)\left[V_i\left(1+\frac{C_s}{C_f}\right) - \frac{C_s}{C_f}DV_R\right]$$

where

$$\beta = \frac{C_f}{C_s + C_f}; \quad A = \frac{A_1A_2}{n}$$

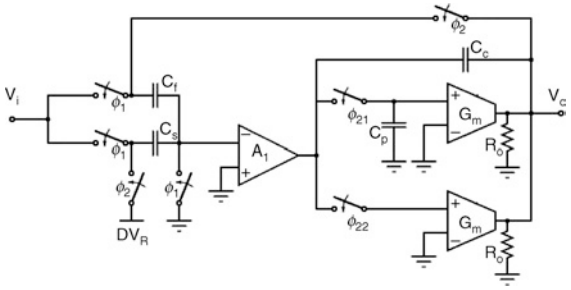

Fig. 1 *Two-parallel correlated double sampling MDAC*

The factor of $(1/2)^2$ in the effective gain of the two-parallel PCDS ($(1/n)^n$ in n-parallel PCDS) is due to the degradation of the effective output impedance when multiple amplifiers are put in parallel. For the two-parallel realisation, this attenuation can be overcome by using the second stage shown in Fig. 2. During ϕ_{21}, the output of the first stage is applied to the gate of M1, with the M2-M3 combination forming an active load. The previous output current is maintained during ϕ_{22} by C_P. M2 is connected to the output of the first stage and M1 acts as the load. The effective gain of the opamp now becomes $(A_1A_2)^2$, where A_2 is the gain of the second stage.

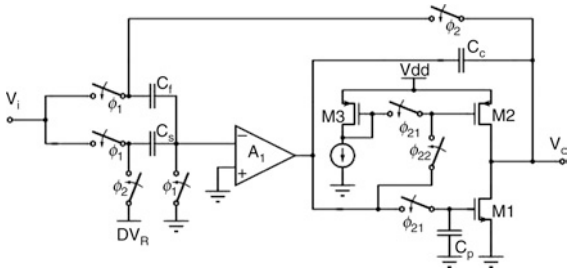

Fig. 2 *Two-parallel correlated double sampling MDAC with improved gain*

Comparison of kT/C noise performance: kT/C noise power is calculated assuming the opamps have infinite bandwidth. For a 1.5 bit multiply by 2 MDAC, $C_s = C_f$. The expressions for the output referred kT/C noise for the conventional MDAC, CDS MDAC [3] and the parallel CDS MDAC are shown in (1), (2) and (3), respectively:

$$V_{on}^2 = \frac{2kT}{C_s} \tag{1}$$

$$V_{on}^2 = \frac{2kT}{C_s} + \frac{4kT}{C_I} \tag{2}$$

$$V_{on}^2 = \frac{2kT}{C_s} + \frac{4kT}{C_P}\frac{1}{A_1^2} \tag{3}$$

In all three MDACs, the sampling capacitors C_s and C_f produce a noise power of kT/C each giving the common $2kT/C_s$ in each equation. The noise voltage sampled on C_I in Fig. 3*a* sees a gain of 2 to the output, hence giving an additional noise power of $4kT/C_I$. In the case of the PCDS MDAC, the noise voltage on C_P sees an attenuation of $2/A_1$ to the output, and thus the additional noise power is only $4kT/(C_PA_1^2)$. For a given ADC accuracy, the PCDS MDAC can be operated at a higher sampling rate or lower power than its CDS counterpart.

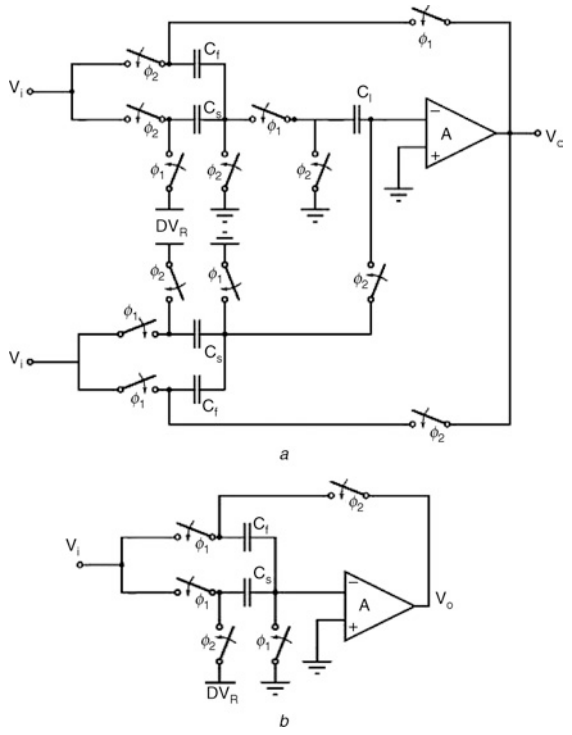

Fig. 3 *1.5 bit stage MDAC for correlated double sampling and conventional multiply 2*

a Correlated double sampling
b Conventional multiply 2

Simulation results: Simulations were run to compare the settling accuracy of a two-parallel PCDS MDAC to a CDS MDAC with similar gain. The opamps used were designed to have enough

bandwidth for 10-bit settling. The effectiveness of each MDAC to double the DC gain is visually shown by plotting the settling behaviour of a conventional MDAC (see Fig. 3*b*) with double the CDS MDAC gain. Generally, CDS achieves better settling accuracy than PCDS which experiences mild output impedance degradation. When the impedance attenuation is avoided in two-parallel CDS, the settling accuracy becomes higher than that of CDS. From Fig. 4, the effective gains of the CDS, PCDS and improved PCDS are 52, 44 and 56.7 dB, respectively.

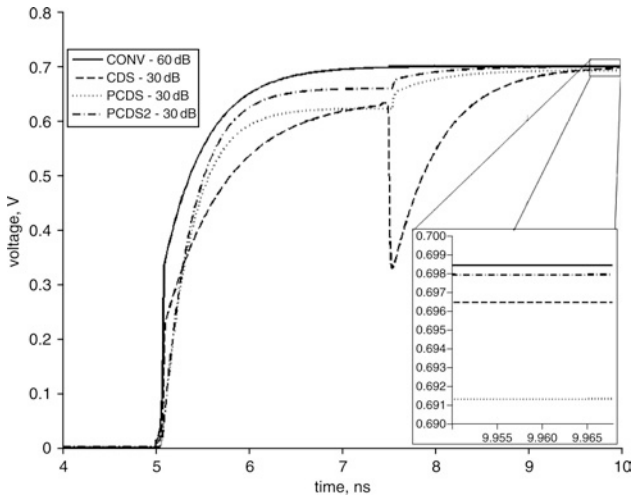

Fig. 4 *Simulated settling response of different MDAC topologies to 350 mV input (700 mV ideal output)*

Conclusion: A parallel correlated sampling technique is proposed. It achieves gain enhancement with insignificant noise penalty. Simulation results show comparable settling accuracy to CDS. The technique has been explained for pipeline/algorithmic ADCs MDACs but can be extended to other switch-capacitor applications.

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