Switched-capacitor DAC with analogue mismatch correction

Un-Ku Moon, J. Silva, J. Steensgaard and G.C. Temes

A background calibration method for enhancing the accuracy and linearity of a switched-capacitor digital-to-analogue converter is described. The method can be used alone or in combination with mismatch shaping to achieve very high accuracy and linearity combined with high speed.

Introduction: In a number of important applications such as delta-sigma ADCs or DACs as well as pipelined or segmented data converters, low-resolution but high-linearity DACs are required. Since the linearity of the DAC is limited by the matching accuracy of its nominally equal-valued analogue circuit elements (resistors, capacitors, or current sources), for more than 12 bit linearity the required matching precision is difficult to obtain. Alternative techniques have recently been developed which utilise digital circuitry to filter out the errors generated by the mismatch errors of the DAC elements [1]. However, these mismatch-shaping techniques are effective only if the sampling rate is much higher than the signal bandwidth, i.e. if the signal is greatly oversampled.

In this Letter, a switched-capacitor (SC) DAC using a straightforward analogue calibration process is described. The calibration process is applicable even if the signal is not oversampled, and can be combined with mismatch shaping if it is.

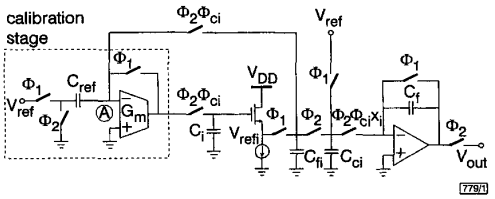

Fig. 1 *Switched-capacitor DAC with analogue mismatch correction*

SC DAC with analogue calibration: Fig. 1 shows the conceptual diagram of a DAC constructed using SC circuitry. For an M-level DAC, M–1 identical input branches need to be connected to the virtual ground node; the ith branch, the only one shown in the Figure, contains a coarse input capacitor C_{ci} which can deliver a charge $C_{ci}V_{ref}$ into C_f, and a fine input capacitor C_{fi} which can deliver $C_{fi}V_{refi}$, where V_{refi} is an adjustable DC voltage.

The operation of the circuit is as follows. The input word is in a thermometer code with bits x_1, x_2, ..., x_M such that if the integer value of the input word is m, the bits x_1, x_2, ..., x_m equal 1, and the rest are 0. During the reset phase ($\Phi_{1=1}$), the feedback capacitor C_f is discharged and all input capacitors are charged to the reference voltages: C_{ci} to V_{ref} and C_{fi} to V_{refi}. Next, during the conversion phase ($\Phi_2 = 1$), the capacitors in the first m input branches are discharged into C_f, resulting in an output voltage $V_{out} = -(mC/C_f)V_{ref}$. To correct for the mismatch of the nominally equal-valued input capacitors, a calibration stage is used. It contains a transconductor G_m and a reference capacitor C_{ref}, and is shared by all input branches. It readjusts the ith reference voltage V_{refi} once every M clock periods, when the ith calibration clock phase Φ_{ci} is high, so as to make the combined charges stored in C_{ci} and C_{fi} equal to $C_{ref}V_{ref}$. To replace the branch being calibrated, an extra input branch is needed, raising the total number of input branches to M.

The calibration principle is somewhat similar to that proposed earlier by Groeneveld *et al.* [2], who used current copiers to calibrate the current sources of a DAC. Since it is a background process, it remains active during operation, and is able to correct for a slow drift caused, for example, by thermal effects.

Analysis of calibration process: The calibration process may be analysed by applying the law of charge conservation to input node Ⓐ of the G_m block in the circuit of Fig. 1, at the time of transition between the $\Phi_1 = 1$ and $\Phi_2 = 1$ intervals. Assume that the source follower providing V_{refi} has a constant offset voltage and a gain $(1 + a)$, where a is a small gain error. Then the pole z_p of the calibration system is given by

$$z_p = 1 - \frac{(1+a)C_{fi}G_mT/2}{C_i \cdot (C_{ref} + C_{ci} + C_{fi})} \quad (1)$$

where $T = 1/f_c$ is the clock period. For stability, $|z_p| < 1$. This sets upper and lower bounds on G_m:

$$0 < G_m < 4C_i\frac{(C_{ref} + C_{ci} + C_{fi})}{C_fT} \quad (2)$$

The calibration is carried out as a background operation during the data conversion, so that the speed of its convergence is of only secondary importance. It can be shown, however, that the relative error of V_{refi} decreases by a factor $|z_p|$ in each calibration cycle. Thus, for reasonable pole values ($|z_p| < 0.9$), convergence occurs within a few hundred cycles even for very high specified accuracy.

The effect of the offset voltage V_{os} of G_m on the DAC linearity can also be found analytically. V_{os} introduces a charge error $V_{os}(C_{ci} + C_{fi})$. Since typically $V_{os} \simeq V_{ref}/1000$, and the mismatch error of $C_{ci} + C_{fi}$ is ~0.1–0.2%, the charge mismatch due to V_{os} is of the order of only a few parts per million, which is negligible in most cases.

Another parasitic effect, which may introduce nonlinearity even for accurately matched capacitors, is the mismatch of the clock feedthrough and charge injection charges from the switches. Using the formulas given in [3], it can easily be shown that the ratio between the injected charge q_i of a switch and the signal charge is

$$\frac{q_i}{C_{ref}V_{ref}} \simeq \frac{10f_cL^2}{\mu V_{ref}} \quad (3)$$

where L is the channel length of the switch, and μ is the carrier mobility in the channel. For typical values (say f_c = 10MHz, V_{ref} = 1V, L = 0.6μm, μ = 100cm²/Vs), this ratio can be found to be ~3.5×10^{-4}. Since only the mismatch of these charges between the input branches affects the linearity, assuming a 10% mismatch the resulting error will be at least 90dB below the signal level. This corresponds to a 15 bit performance, and is acceptable for many applications.

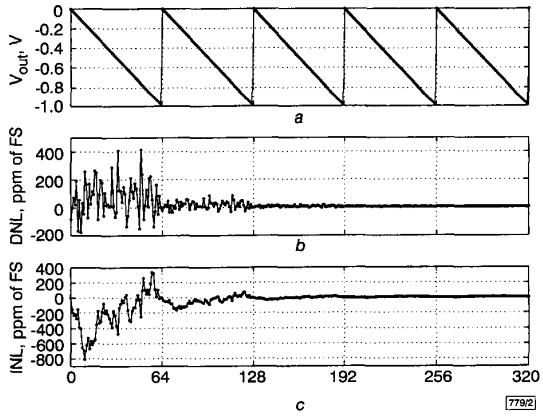

Fig. 2 *Simulation*

a Output voltage
b DNL
c INL

Practical considerations: The above discussion was aimed at explaining the basic concepts of the proposed calibration process for a simplified circuit. Thus, only single-ended circuits were shown, although for high accuracy and dynamic range a fully differential circuitry is needed. The nonideal effects owing to the finite gain, offset and $1/f$ noise of the op-amp used in the DAC were also ignored; they can readily be corrected by using correlated double sampling techniques [4]. Finally, the circuits shown are stray sensitive, i.e. the parasitic capacitances loading the top plates of C_i, C_{ci} and C_{fi} have an influence on the operation. However, if these stray capacitances are fairly well matched, then their values and linearity are not critical to the conversion accuracy. If necessary, the circuit may also be modified for stray-insensitive operation. Finally, as mentioned earlier, the proposed technique may be combined with dynamic element matching [1] which

assigns the x_i so as to suppress the remaining mismatch errors in the signal band.

Design example: To confirm the validity of the proposed technique, a DAC circuit containing 64 elements was simulated with HSPICE. The circuit used C_{ref} = 1.1pF, C_i = 1pF, C_f = 0.2pF and C_c = 1pF, for a clock rate of 50MHz. A random mismatch with a standard deviation of 1% was introduced into the C_{fi} and C_{ci} values. From eqn. 1, the maximum G_m is 2.2mA/V; for this simulation, G_m = 0.88mA/V was chosen, setting the calibration behaviour to a slightly overdamped response.

A full-scale digital ramp was applied to the DAC. Fig. 2*a* shows the DAC output voltage, Fig. 2*b* the differential nonlinearity (DNL), and Fig. 2*c* the integral nonlinearity (INL) characteristics. During the first 64 clock periods the circuit operated without correction, and the DNL and INL were large: referred to full scale, they were 130ppm and 258ppm, respectively. After only four calibration periods, they became DNL = 0.72ppm and INL = 3.71ppm. This is approximately equivalent to an 18 bit performance.

Conclusions: A simple analogue background calibration technique has been described for switched-capacitor DACs. It compensates for the mismatch of the capacitors, and should allow the realisation of fast and accurate data conversion, alone or in combination with a mismatch-shaping algorithm. Although the technique was described for unit-element DACs, it can be extended also for binary-weighted converters.

Acknowledgment: The authors are grateful to P. Ferguson for useful discussions.

9 August 1999
Electronics Letters Online No: 19991288
DOI: 10.1049/el:19991288

Un-Ku Moon, J. Silva, J. Steensgaard and G.C. Temes (*Department of Electrical and Computer Engineering, Owen Hall, Oregon State University, Corvallis, OR 97331-3211, USA*)

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Very low-voltage class AB CMOS and bipolar precision current rectifiers

J. Ramírez-Angulo, R.G. Carvajal, J. Tombs and A. Torralba

Simple class-AB CMOS and bipolar precision rectifier circuits that operate from a single supply close to a transistor's threshold voltage are introduced. These circuits have output voltage swings comparable to the supply voltage. Results from simulations of MOS and bipolar precision rectifiers at 20 and 100MHz, respectively, are presented. Experimental results of a test chip are presented that verify the proposed circuits. A full wave precision rectifier based on the proposed rectifier cells is discussed.

Introduction: Precision rectification is one of the fundamental operations in nonlinear systems. New generations of VLSI systems for wireless applications operate from a single supply voltage of 1.5V or below with the need for low static power consumption and high frequency operation. Low-voltage CMOS and BICMOS rectifiers with 3.3V supply requirements and very good high frequency performance have been reported [1, 2]. In this Letter we report a very simple class AB precision rectifier cell that operates with a supply of 1.2V, fabricated in CMOS technology (for 0.85V transistor threshold voltages), and 0.8V using bipolar transistors. It has excellent high frequency performance and very low static power consumption. Utilisation of these circuits in combination with low-voltage mirrors [3] allows the implementation of very low-voltage piecewise linear approximation circuits according to the approaches reported in [4]. This is illustrated with the example of a full wave rectifier.

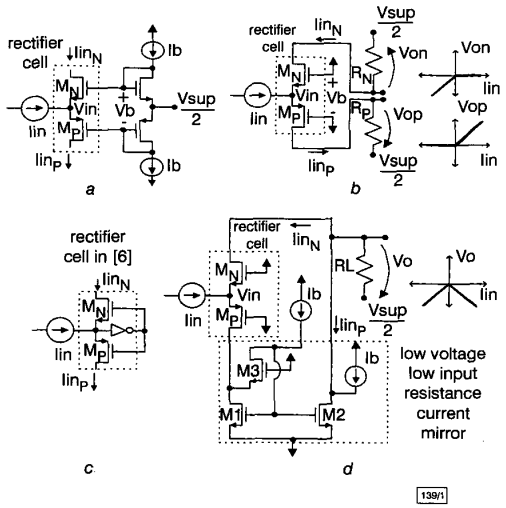

Fig. 1 *Low-voltage class AB CMOS precision rectifier*
a Circuit in [1]
b Proposed circuit
c Low-voltage rectifier in [5]
d Full-wave rectifier

Circuit operation: In the following we assume a single voltage supply V_{sup}. We also assume that $|V_{thP}| + V_{thN} > V_{sup} > \{|V_{thP}|, V_{thN}\}$ where V_{thP} and V_{thN} denote the threshold voltages of the P and N transistors, respectively. Fig. 1*b* shows the CMOS version of the proposed rectifier cell. It consists simply of two transistors (M_N and M_P). The gates of M_N and M_P are connected to V_{sup} and ground, respectively; therefore $V_{sup} = V_{GSN} + V_{GSP}$. Given that there is not enough voltage to turn on both transistors simultaneously ($V_{sup} < |V_{thP}| + V_{thN}$), under quiescent conditions, a very small (subthreshold level) current flows through M_N and M_P and $V_{on} = V_{op} \simeq 0$. For positive input currents, M_P turns on, and the input current *Iin* flows through M_P to R_P. The input voltage takes a value $V_{in} = V_{SGP} > |V_{thP}|$ that is closer to V_{sup} than to ground due to low-voltage supply operation ($V_{sup} < |V_{thP}| + V_{thN}$). Given that the voltage between the gates of M_N and M_P is constant ($V_{sup} = V_{SGP} + V_{GSN}$), when V_{SGP} increases, V_{GSN} decreases and M_N is turned off ($Iin_N = 0$). For negative input currents M_N turns on and the input current flows through M_N to R_N. In this case the input voltage decreases to a value V_{in} that satisfies the condition $V_{in} = V_{sup} - V_{GSN} > V_{sup} - V_{thN}$ which is closer to ground than to V_{sup}. Similar to the previous case, M_P is turned off ($Iin_P = 0$) when M_N is turned on.

Assuming that V_{sup} = 1.2V, and typical values for 1.2μm CMOS technology $V_{thN} = |V_{thP}|$ = 0.85V and $V_{GSN} = V_{SGP}$ = 0.95 V for both transistors, then the input voltage swings approximately from 0.95V (M_P ON) to 0.25V (M_N ON). This relatively limited swing provides the circuit with excellent high frequency performance. Another advantage for high frequency operation is the fact that the gates of M_P and M_N are not subject to swings in this circuit. Larger supply voltages (say V_{sup} = 1.5V) result in a reduced input voltage swing (0.95V to 0.55V) and improved high frequency performance. This is the only precision rectifier approach that uses a bias voltage between the gates of the two transistors (V_b in Figs. 1*a* and *b*) that satisfies the condition $\{V_{thN}, |V_{thP}|\} < V_b < V_{thN} + |V_{thP}|$. Another approach reported in [1] (Fig. 1*a*) uses a bias voltage $V_b > V_{thN} + |V_{thP}|$ and cannot be used with as low V_{sup} as that proposed here. A rectifier cell is presented in [5] that can operate also with very low voltage supply (Fig. 1*c*).