A 1-V, 10-MHz Clock-Rate, 13-Bit CMOS $\Delta\Sigma$ Modulator Using Unity-Gain-Reset Opamps

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Abstract

A low-voltage $\Delta\Sigma$ modulator, incorporating unity-gain-reset opamps, is described. Due to the feedback structure, the opamps do not need to be switched off during operation, and hence can be clocked at a very high rate. A test chip, realized in a 0.35-μm CMOS process and clocked at 10.24 MHz, provided a dynamic range (DR) of 80 dB and a signal-to-noise+distortion-ratio (SNDR) of 78 dB for a 20-kHz signal bandwidth, and DR = 74 dB and SNDR = 70 dB for a 50-kHz BW.

1. Introduction

Fine-linewidth low-voltage CMOS technologies make possible fast and low-power operation for digital circuitry; however, they introduce problems for the designers of analog circuits [1]. One difficulty involves the operation of floating switches required in switched-capacitor (SC) circuits. If the dc supply range $V_{dd} + |V_{ss}|$ becomes comparable to (or is less than) the sum of the magnitudes of the threshold voltages $V_{tn} + |V_{tp}|$, these floating switches can no longer be turned on for midrange signals [2]. Boosted or bootstrapped clock signals can overcome this problem [3], but they may stress and damage the gate oxide [4]. Low-threshold switches can also be used [5], but they require special fabrication technology which may be expensive, and tend to lead to increased leakage currents.

The commonly used technique for realizing low-voltage (LV) SC circuits in standard CMOS technology uses *switched opamps* (SOs) [6], [7]. An SC integrator using a SO is shown in Fig. 1. It does not have any floating switches, and hence can use low (e.g., 1 V) supply voltage. However, since the opamp needs to be turned off and then on again in every clock cycle, the settling time of the resulting transients limits the speed of the operation.

An alternative to the SO technique was proposed by us earlier [8]. It utilizes opamps whose output is reset to their input during one of the clock phases, and hence will be called *reset opamps* (ROs). The opamps remain in their active voltage regions at all times, and hence the turn-on and turn-off transients are avoided, making fast operation possible. Details of the various circuit techniques which can be used to implement RO stages were described in [8].

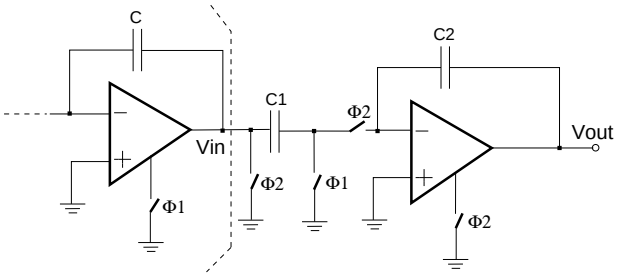

Figure 1. Switched-opamp integrator.

This paper describes a LV (1.05-1.2 V) high-speed $\Delta\Sigma$ modulator using RO stages. It was fabricated in a standard 0.35-μm CMOS process, could be clocked over 10 MHz, and achieved 13-bit performance over the audio frequency range. Over a 50-kHz signal band, it gave a 12.5-bit conversion accuracy.

2. Modulator architecture

Fig. 2 illustrates the block diagram of the modulator. Since the RO integrators used introduce half clock period delays, matching delays were introduced into the feedback paths. These were realized in the digital domain, using half-delay RS flip-flops.

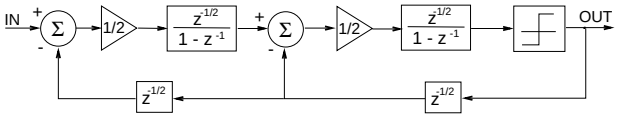

Figure 2. Low-voltage $\Delta\Sigma$ modulator.

3. The RO integrator and the input buffer

Fig. 3 shows the basic RO integrator. While $\Phi 1$ is high, the input capacitor $C1$ is charged to the input voltage v_{in}, and the opamp output is reset to V_{dd} (more precisely, to $V_{dd} - V_{dsat}$, to keep the output devices in saturation). When the next $\Phi 2$ rises, the output voltage of the preceding RO is reset, causing the charge in $C1$ to enter $C2$. Hence, v_{out} changes by an increment which is a linear function of v_{in}. All switches in the stage operate at

$V_{ss} = 0\ V$, and hence they all can be realized by single NMOS transistors.

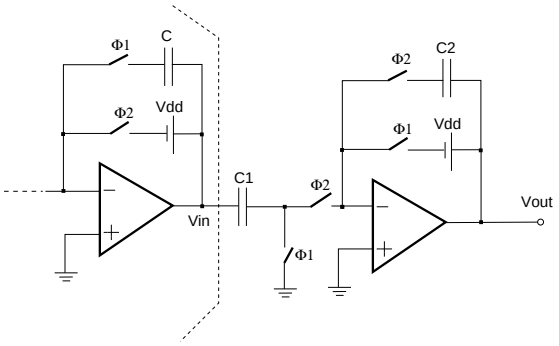

Figure 3. The unity-gain-reset integrator

Note that (as mentioned above) the integrator introduces a half-period ($T/2$) delay between its input and output signals, and hence adjacent stages must be operated with complementary clock phases.

The input integrator is a special case, since its input capacitor is not connected to the output of a RO. Ref. [10] describes an input stage which can be used to feed the first integrator of the filter. The circuit used by us is shown in Fig. 4. It is similar to the buffers described in Refs. [10], [11]. It is basically a track-and-reset (T/R) circuit used as an input-sampling switch. During Φ_2, it samples the input signal and provides the inverted input signal to the input capacitor of the first stage. During Φ_1, the opamp is in unity-gain-reset configuration, providing V_{dd} to the first stage.

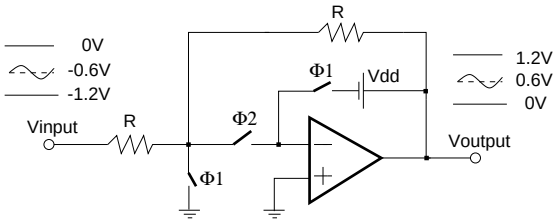

Figure 4. The LV input sampling circuit.

4. Low-voltage opamp

The opamp used is shown in Fig. 5 [12]. It has a pseudo-differential structure, chosen to ease the implementation of the common-mode feedback (CMFB) circuit. Each half contains a PMOS differential pair and an NMOS inverter output stage, with an RC compensating branch between them. The input stage uses a LV current mirror [7].

The minimum supply voltage needed for linear operation is given by

$$V_{ddmin} = max\ [\ 3V_{ov}, V_{th} + 2V_{ov}\ ] \qquad (1)$$

The main performance parameters of the opamp with a load of 3.5 pF are summarized in Table 1.

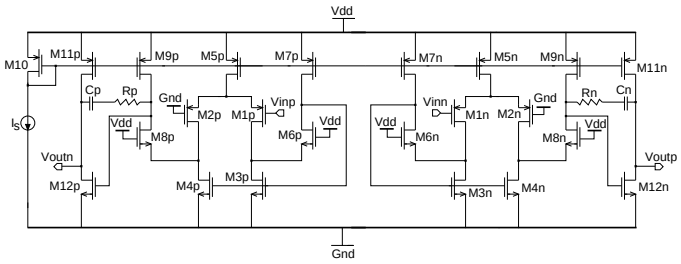

Figure 5. The LV pseudo-differential opamp.

Table 1. The simulated performance of the LV opamp.

Adc	fu	PM	Tsettling	Slew Rate
68 dB	170 MHz	70°	20 ns	100 V/μs

5. Level shifting and CMFB circuits.

A charge-domain dc level shifter is required to maintain the appropriate input and output common-mode voltages for the opamps. With a CM level of $V_{dd}/2$ at the opamp output, the CM at the next opamp input must be set to ground.

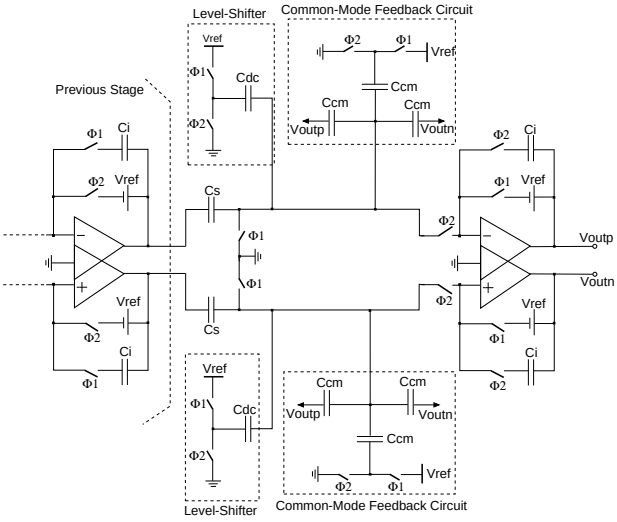

Figure 6. The pseudo-differential integrator with CMFB.

The SC dc level shifter and CMFB circuit [9] used are shown in Fig. 6. The output voltages V_{outp} and V_{outn} are averaged and used to inject a correction charge into the virtual grounds, so as to obtain an output CM voltage equal to $V_{dd}/2$.

6. The comparator and the DAC feedback branch

The low-voltage comparator used is shown in Fig. 7. It requires dc level shifters at the inputs to set the input CM to ground. The reset switches ground both latch outputs, since floating reset switches cannot be used. The simulated transition speed of the comparator was 12 ns.

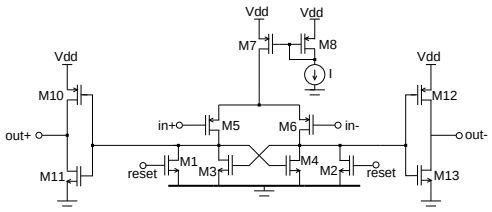

Figure 7. The LV comparator.

Fig. 8 shows the circuit diagram of the DAC feedback branches. Its switches operate at ground or V_{dd}. The CM of the DAC signal is cancelled by the level shifter circuits at the opamp inputs.

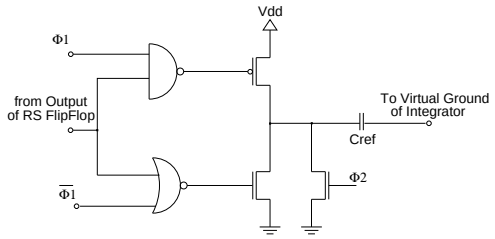

Figure 8. The low-voltage DAC feedback branch.

7. The overall circuit diagram

The circuit of the modulator (with the CMFB circuits and input buffers omitted for clarity) is shown in Fig. 9. The element values (scaled for optimum dynamic range) are given in Table 2.

Table 2. The capacitance values.

Cs1	2 pF	Cs2	0.8 pF	Csc	0.4 pF
Cdac	2 pF	Cdac2	0.4 pF	Cdcc	0.4 pF
Cdc1	1 pF	Cdc2	0.12 pf		
Ci1	8 pF	Ci2	1.6 pF		

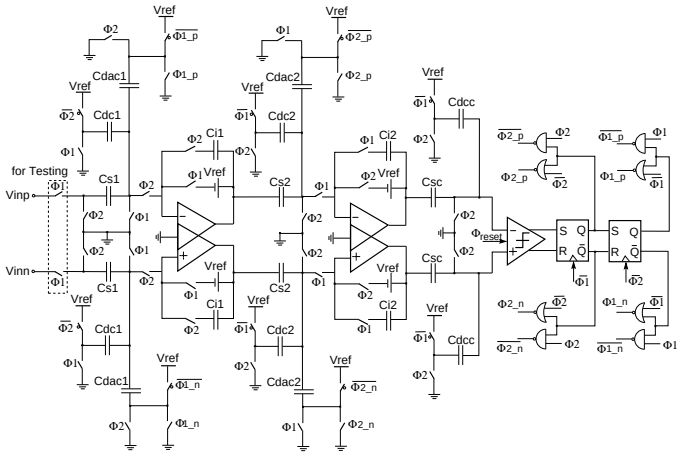

Figure 9. The LV second-order $\Delta\Sigma$ modulator.

8. Layout and floor plan

Fig. 10 shows the die photo of the prototype IC, realized in a 0.35 μm double-poly triple-metal CMOS technology. The digital and analog circuitries are separated, with the opamps located at maximum distance from the digital stages. Well and substrate guard strips and rings were also used to shield the sensitive analog elements from substrate noise. By using static switches, it was possible to allow operation using either the input stage of Fig. 4 or a floating input transmission gate at the front-end. This allowed operation even if the actual threshold voltages of the fabricated chip were different from the simulated values. The total chip area (excluding the input buffer) was 0.41 mm^2.

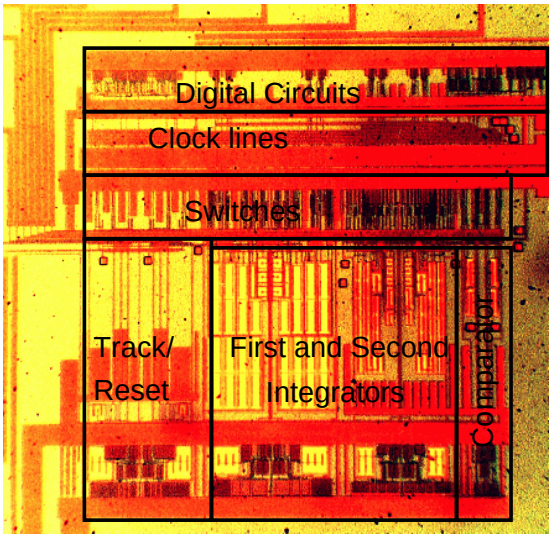

Figure 10. The die photograph of LV second-order $\Delta\Sigma$ modulator.

9. Test results

The fabricated chip was tested with a 10.24 MHz clock signal and with varying (1.05 to 1.2 V) supply voltages. Table 3 gives a summary of the measured results. For audio band (0 to 20 kHz) operation, a true 13-bit accuracy resulted; extending the input frequency range to 0-50 kHz, ENOB = 12.5 bits was obtained. The chip remained operational, but at ENOB = 10.5 bits, down to 0.95 V supply voltage. The SDNR and SNR curves for a 2.5 kHz input sine wave are shown in Fig. 11.

The typical measured spectrum of the digital output stream is illustrated in Fig. 12. No harmonics were detected.

There was a variation of the threshold voltages from the simulation models to the actual chips. While the models assumed $V_{thn} \cong 0.55$ V and $|V_{thp}| \cong 0.55$ V, in the chips V_{thn} ranged from 0.486 V to 0.563 V, and $|V_{thp}|$ from 0.422 V to 0.486 V. In the low-threshold chips, the floating input switch could be turned on; in the others, the

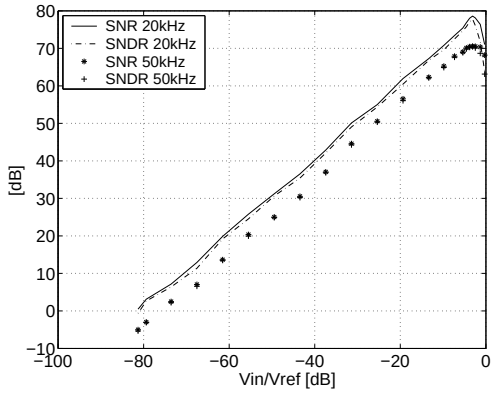

Figure 11. The SNR and SNDR for 20 kHz and 50 kHz signal bands

Table 3. The measured performance of the second-order $\Delta\Sigma$ ADC.

Signal Bandwidth	20 kHz	50 kHz
Sampling Frequency	10.24 MHz	10.24 MHz
Max. Diff. Input	1.2 Vpp	1.2 Vpp
Dynamic Range	80 dB	74 dB
Peak SNR	78.6 dB	70.6 dB
Peak SNDR	77.8 dB	70.4 dB
Power Consumption	5.6 mW	5.6 mW
Supply Voltage	1.05 V	1.05 V
Chip Core Area	0.41 mm^2	0.41 mm^2
Technology	0.35 μm	0.41 mm^2

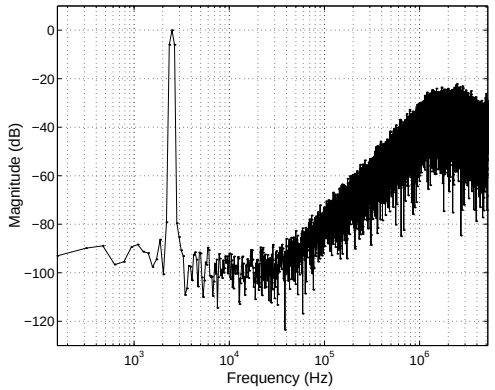

Figure 12. The spectrum of the digital output bit stream.

input buffer had to be used. The performance did not vary significantly between the two modes of operation.

10. Conclusions

A low-voltage and fast delta-sigma ADC was designed and fabricated. It uses unity-gain-reset opamps, which do not require the turning on and off associated with switched opamps. The test results indicate that this circuit technique is suitable for high-speed high-accuracy operation with 1 V or lower supply voltages.

11. Acknowledgments

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12. References

[1] Edgar Sánchez-Sinencio and Andreas G. Andreou, *Low-Voltage/Low-Power Integrated Circuits and Systems*, IEEE Press, NJ 1999

[2] M. Steyaert, V. Peluso, J. Bastos, W. Sansen, "Custom analog low power design: The problem of low voltage and mismatch," *IEEE Custom Integrated Circuits Conference,* 1997, pp. 285-292.

[3] J. Grilo, E. MacRobbie, R. Halim, Gabor C. Temes, "1.8 V, 94 dB dynamic range $\Delta\Sigma$ modulator for voice applications," *Proc. ISSCC*, Feb. 1996, pp. 230-231.

[4] "The national technology roadmap for semiconductors," Semiconductor Industry Assoc., Tech. Rep., 1997

[5] T. Atachi, A. Ishinawa, A. Barlow, and K. Taksuka, "A 1.4 V switched capacitor filter," *Proc. CICC*, May 1990, pp.8.2.1-8.2.4

[6] V. Peluso, M. Steyaert, and W. Sansen, "A 1.5 V 100 μW $\Delta\Sigma$ modulator with 12-bit dynamic range using the switched-opamp technique," *IEEE J. Solid-State Circuits,* vol. 32, pp. 943-952, July 1997.

[7] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900 mW low-power A/D with 77 dB dynamic range," *IEEE J. Solid-State Circuits,* vol. 33, pp. 1887-1896, Dec. 1998.

[8] E. Bidari, M. Keskin, F. Maloberti, U. Moon, J. Steensgard, and G. C. Temes, "Low-voltage switched-capacitor circuits," *Proc. IEEE Int. Symp. Circuits Syst.*, Florida, May 1999, vol. II, pp. 49-52.

[9] L. Wu, M. Keskin, U. Moon, and G. C. Temes, "Efficient common-mode feedback circuits for pseudo-differential switched-capacitor stages," *Proc. IEEE Int. Symp. Circuits Syst.*, Geneva, May 2000, vol. V, pp. 445-448.

[10] A. Baschirotto, R. Castello and G. P. Montagna, "Active series switch for switch-opamp circuits," *Electron. Lett.*, vol. 34, pp. 1365-1366, July 1998.

[11] M. Ishikawa and T. Tsukahara, "An 8-bit 50-MHz CMOS subranging A/D converter with pipelined wide-band S/H," *IEEE J. of Solid-State Circuits*, vol. 23, pp. 1309-1315, Dec. 1988.

[12] A. Baschirotto, "A 40 MHz CMOS sample & hold operating at 1.2 V," *ESSCIRC*, 1998