SWITCHED-CAPACITOR CIRCUIT TECHNIQUES IN SUBMICRON LOW-VOLTAGE CMOS

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Biography

Un-Ku Moon (S'92–M'94) received the B.S. degree from University of Washington, Seattle, the M.Eng. degree from Cornell University, Ithaca, New York, and the Ph.D. from University of Illinois, Urbana-Champaign, all in electrical engineering, in 1987, 1989, and 1994, respectively. From February 1988 to August 1989, he was a Member of Technical Staff at AT&T Bell Laboratories in Reading, Pennsylvania, and during his stay at the University of Illinois, Urbana-Champaign, he taught a microelectronics course from August 1992 to December 1993. From February 1994 to January 1998, he was a Member of Technical Staff at Bell Laboratories, Lucent Technologies in Allentown, Pennsylvania. Since January 1998, he has been with Oregon State University. His interest has been in the area of analog and mixed analog-digital integrated circuits. His past works include highly linear and tunable continuous-time filters, telecommunication circuits including timing recovery and analog-to-digital converters, frequency synthesizers, and switched-capacitor circuits.

Abstract

The continued down scaling of submicron CMOS technology forces innovation of practical and economical circuits that will tolerate reduced headroom (reduced power supply voltage) due to lowering of the technology's maximum allowable voltage. Given the relatively large threshold voltages with respect to the shrinking headroom, a group of widely used analog signal processing building blocks that are made of switched-capacitor (SC) stages will encounter severe overdrive problems when operating at these low-voltage conditions. This tutorial will summarize some of the well-known solutions currently in use, problems associated with these solutions, and propose novel circuit techniques that we have recently developed for truly low-voltage switched-capacitor applications.

This work was supported by Lucent Technologies and CDADIC (NSF Center for Design of Analog-Digital Integrated Circuits).

I. Introduction

As we move towards the nanotechnology era, technological advancements in fine-linewidth submicron CMOS process has allowed tremendous improvements in the area of digital VLSI. The continually increasing level of integration with steadily rising clock rates is paving a path in the direction of more sophisticated and powerful digital systems. While this positive trend of technological achievement promises small, fast and complex digital signal processing available today and increasingly so into the very near future, one of the key *analog* limitations of state-of-the-art submicron CMOS technologies remains the restricted power-supply voltage, limited by the low junction breakdown voltage of the high density process and by the thin gate oxide, prone to voltage stress and breakdown. Even beyond this fundamental limitation for analog circuit design, in growing number of portable applications, the available external power source may also limit the supply voltage. For example, the external power source may be a 1.2 V battery, with an end-of-life voltage of only 0.9 V.

In much of analog and mixed analog-digital circuits, the circuit technique that is most commonly used for analog signal processing is based on switched-capacitor (SC) stages. They are used in many practical necessary applications, such as data conversion (both in Nyquist-rate and over-

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sampled $\Delta\Sigma$ ADCs), analog filters, sensor interfaces, etc. However, there are fundamental limitations on the operation of switches when the supply voltage becomes less than the sum of the absolute values of the PMOS and NMOS threshold voltages. This is specifically illustrated in Fig. 1. With

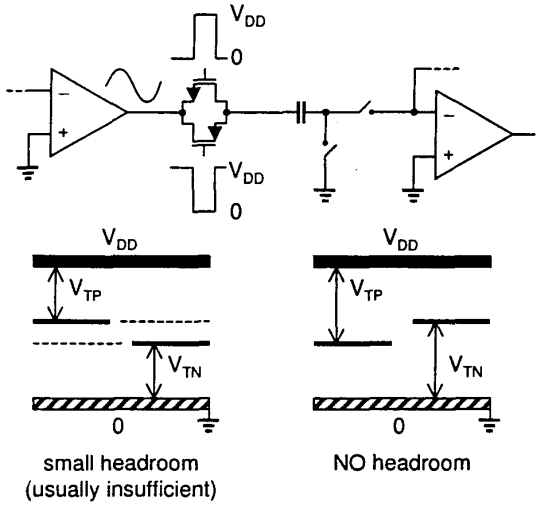

Figure 1: Fundamental problem of a CMOS switch

a switch connected to a signal voltage (commonly referred to as the *floating switch*) that is about half-way between the rail voltages (0 V and V_{DD}), and $V_{tn} + |V_{tp}| > V_{DD}$, it would not be possible to turn the switch *on*, even if a CMOS transmission gate is used to realize it.

There are two well-known approaches that are commonly used to bypass this problem. One uses internal voltage boosting to obtain high-swing clock signals [1]. This is typically done by doubling the swing of clock signals from $0 - V_{DD}$ to $0 - 2V_{DD}$. This approach is useful if the supply voltage is restricted by the external source, as in the case of battery-operated devices, or if only the junction breakdown was of concern (i.e. gate oxide can tolerate $2V_{DD}$). This technique, however, cannot be used if the thin gate oxide limits the permissible clock voltage, which is the case in the submicron low-voltage CMOS process. This current and future trend is outlined in the Technology Roadmap for Semiconductors [2]-[3]. The second alternative suggests the use of switched op-amps [4]. This approach also suffers from some shortcomings. Specifically, the transients introduced by the required power-up/power-down of the op-amp output stage slow down the operation—increased settling time leading to reduced operating speed (clock rate) of the circuit.

A third possibility for bypassing the problem associated with floating switches is the use of multi-threshold process. With the availability of well controlled low-threshold devices in future low voltage processes, the headroom problem for floating switches can be relaxed by a significant amount. This direction, thus far, was also difficult to achieve. This is due to lack of tight control of threshold voltages over process and temperature variations, and increasing switch leakage during the floating switch's *off* state.

Finally, recent bootstrapping techniques have demonstrated effectiveness for use in low-voltage floating switches [5]-[6]. However, these methods impose an instantaneous higher voltage glitch across the thin gate oxide before the inversion takes place under the gate and a channel forms in the MOSFET switch. Authors of these circuits hope that these brief higher voltage glitches exceeding the technology's maximum will not have a negative effect on the long-term integrity of the gate oxide. The second possible drawback is the circuit complexity involved in the implementation of a good bootstrapped switch. This would most likely limit the maximum clocking speed at which it can operate.

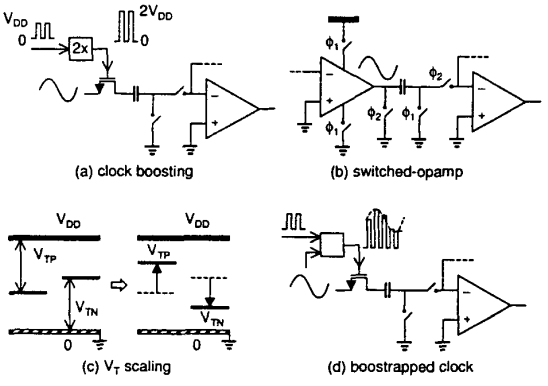

Figure 2: Existing low-voltage switch solutions

These various methods to ease the problem of low-voltage switches described in the above are summarized in Fig. 2.

In the following section (section II), we will expand the dicussion of prior techniques used to ease the low-voltage switch problem. And in section III, we will present a newly proposed method of realizing low-voltage SC circuits. It is based on the use of a novel integrator architecture, and a novel SC gain amplifier. A number of low-voltage SC circuit architectures (in the form of an integrator) that may allow operation down to 1-V level or even lower power supply will be presented. The proposed techniques avoid the use of clock-voltage boosters, switched-opamp, or non-standard low-threshold transistors. Circuit design examples including various low-voltage integrators, biquad, bilinear filter, $\Delta\Sigma$ modulator, and pipelined A/D converter have been successfully demonstrated. Initial simulation results of the 10-bit 20 MS/s pipelined A/D converter example confirm the speed advantage of the new scheme over the existing switched-opamp technique.

II. Prior Art

As we have discussed in the previous section, the existing techniques for low-voltage switches may be classified into four categories. Since one of the options was directed to technology control, i.e. well-controlled low-threshold voltage transistors, we will discuss in this section the other three options that use circuit techniques. The discussions herein are intended to be brief, but substantial enough to provide systematic circuit-level understanding of each method to the reader.

A. Clock-voltage boosting—This method has been particularly useful in the past when an application calls for low-voltage external power source (e.g. 2.4 V battery) but the IC is fabricated via a high-voltage process (e.g. 5-V 2-μm CMOS process). Typically all circuit components, excluding the switches and clocks voltages driving them, are designed for operation in low voltage. A variety of low-voltage op-amps is available for use with low power supply voltages, often at around 1 V or even lower. Given these options, SC circuits are operated with boosted clock voltages, most commonly twice the V_{DD}. This insures that the "on" voltage of the N-channel MOSFET is well above the minimum "V_{th} + required clock overdrive".

A good conceptual example of a clock booster, published by Nakagome et al. [7], is shown in Fig. 3. The input to the clock booster is a s-

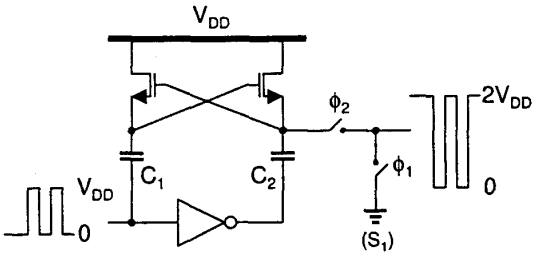

Figure 3: Nakagome clock booster

tandard swing (0 – V_{DD}) clock. Once the circuit settles, during phase-1 (ϕ_1), the booster output is reset to 0 V while the capacitor C_2 is precharged to $\approx V_{DD}$, and during phase-2 (ϕ_2), C_2 is connected to the output with a boosted voltage of $\approx 2V_{DD}$.

An alternative to boosting each clock voltage (as shown above) is to create a $2V_{DD}$ power supply using the same booster (or a similar booster) without the switch S_1, and using this doubled power supply voltage in the output of the clock generator.

One highly successful reference point for the implementation of a switched-capacitor circuit using low external voltage IC is described in [1].

B. Switched-opamp technique—This is a fairly recent method that suggests a way to allow a true low-voltage operation, without the use of clock-voltage boosters. The switched-opamp technique would not violate the maximum voltage restrictions of a low-voltage CMOS process. The basic concept behind this method is illustrated in Fig. 4. In comparison with the standard SC integrator in Fig. 4(a), the switched-opamp integrator shown in Fig. 4(b) operates *without* the floating switch S_1, thus during sampling phase ϕ_1 all switches operate with standard low voltage clocks and NMOS switches. This will operate down to 1-V level with typical threshold voltage (V_{tn}) of 0.7 V, when the opamp virtual ground is set at 0 V. During the opposite phase (ϕ_2), however, the node Ⓐ is reset to ground as in an ordinary integrator. In order to avoid conflict with the opamp output, the output stage of the opamp is tri-stated (i.e. the opamp is *switched off*). And, naturally, the opamp is

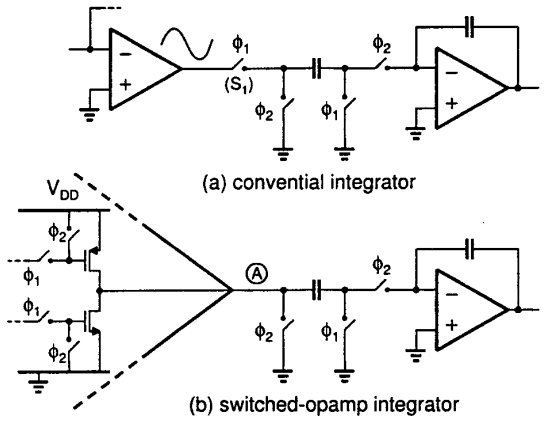

Figure 4: Conventional and switched-opamp

switched back *on* in the next sampling phase ϕ_1. One successful example with good performance is found in [8].

C. Bootstrapped clocking—The idea of boostrapping the clock voltages was used before in the context of accurate and linear sampling of continuous-time input signal [9]-[10]. This has now been extended to allow a nearly-perfect low-voltage operation [5]-[6].

The fundamental operating concept behind the boostrapped low-voltage switches is that the floating MOSFET switch (NMOS for example) would always experience a fixed gate-to-source *overdrive*. Typically V_{gs} sees the technology's maximum voltage V_{DD} during the *on* phase. The circuit details maybe found in [5]-[6].

To illustrate a drawback of the boostrapped switch, a simplified conceptual description is shown in Fig. 5. The NMOS switch (in this example) is *off* when

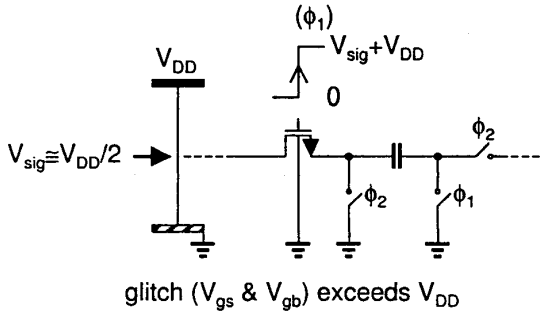

Figure 5: Bootstrapped floating switch

the gate voltage is 0 V. And during the *on* phase, the gate voltage is set to $V_{sig} + V_{DD}$, where the input signal voltage being sampled V_{sig} is somewhere between 0 V and V_{DD}. When the clock transition occurs in the NMOS switch, from *off* state to *on* state, the gate oxide will temporarily see a peak voltage glitch exceeding technology's maximum voltage V_{DD} (V_{gs} and V_{gb} see $V_{DD} + V_{sig} > V_{DD}$), which can be as high as $2V_{DD}$. As soon as the channel is formed under the NMOS gate, the voltage drop across the gate oxide settles to V_{DD}. The authors of these circuits anticipate no reliability issues associated with these temporary glitches.

The other drawback of the low-voltage boostrapped switches is the increased complexity. Abo and Gray [5] demonstrated 14-MHz clocking at $V_{DD} = 1.5V$, while this low-voltage switch has a problem and would experience difficulty with a lower power supply voltage. Steensgaard [6] introduced a version that overcomes this problem, but with additional complexity which would further limit the maximum clock frequency—as his intent was to implement high-*accuracy* low-voltage switch and was not aiming for speed.

III. New Low-Voltage Integrators

The topology of the new integrator is illustrated in Fig. 6 [11]. The critical changes are that the floating switch S_1 of Fig. 4(a) is eliminated and the operation of the grounding/resetting switch is replaced by connecting the sourcing opamp in unity-gain feedback (by switch S_A in Fig. 6). The switch S_B is used to preserve the integrated charge on capacitor C_2. The phases Φ_1 and Φ_2 are non-overlapping clock pulses. For a very low voltage application (1-V for example), a low virtual ground voltage V_A

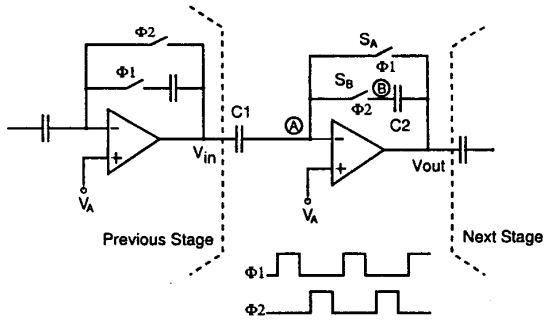

Figure 6: New low-voltage integrator topology

is used ($V_A = 0$ for example). This allows the use of NMOS switches; however, the switch S_B may suffer from forward biasing of the N-diffusion to P-well (substrate) junction during the $\Phi_1 = 1$ period. This happens at node B if the output voltage V_{out} was high during the integrating phase Φ_2. Specifically, if $V_{out} \geq V_{ON} \approx 0.7$ during Φ_2. Several solutions to this problem have been found, and they are discussed in the following.

A. Integrator Using Voltage-Shifted Clock—One solution to this forward-biasing problem is shown in Figs. 7 and 8. This simple solution involves the use of a PMOS switch for S_B and the generation of a voltage-shifted clock signal which swings from ground to $-V_{DD}$ (instead of $+V_{DD}$ to gnd). The clock level-shift generator shown in Fig. 8 is similar in appearance to the commonly used clock booster (e.g. Nakagome booster), but one important distinction is that this circuit *shifts* the clock voltage while *never* exceeding the technology's maximum voltage V_{DD} across any p-n junction or gate oxide. Note that the assumed N-well process allows the biasing of N-type wells to gnd (0 V) instead of V_{DD}.

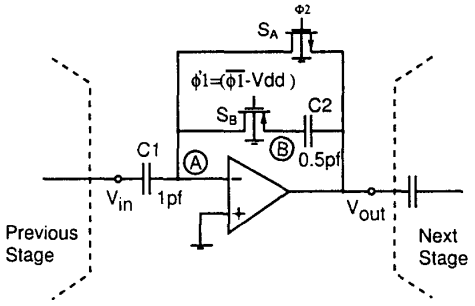

Figure 7: Integrator with PMOS switch

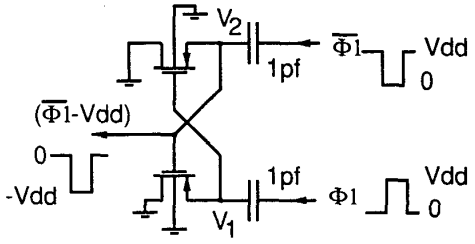

Figure 8: Voltage-shifted clock generator

The transient simulation of this integrator using voltage-shifted clock is shown in Fig. 9. A

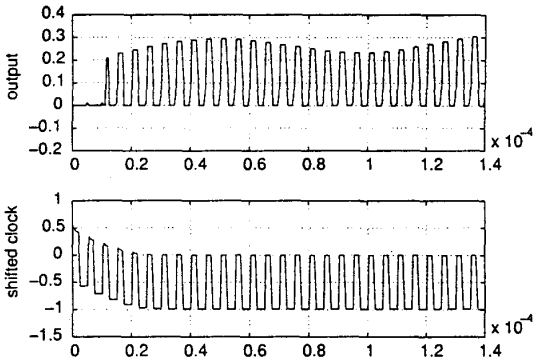

Figure 9: Simulation of integrator in Fig. 7

sinewave input and 200 kHz clock is used. Also, a simplified finite-gain and bandwidth opamp macromodel was used in this simulation. Note that the voltage-shifted clock quickly settles to the shifted voltage swing, and the output voltage resets to 0 V instead of somewhere near $V_{DD}/2$. This resetting of the output voltage is necessary for very low-voltage operation, and a compensating circuit is needed to remedy the resulting dc offset. This will be discussed in the following sub-section.

B. Integrator Using Floating Reference—The conceptual schematic of an alternate implementation is shown in Fig. 10. Here, the forward-biasing of

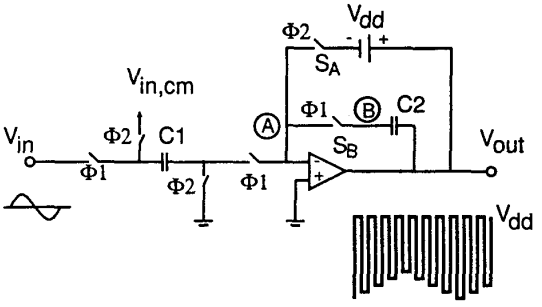

Figure 10: Integrator using floating reference

the substrate-to-diffusion P-N junction at node B is avoided by placing a floating voltage reference in the unity-gain feedback path during $\Phi_2 = 1$. The net result is that the output voltage resets to V_{DD} instead of gnd. Another attractive feature of this topology is that the voltage-shifted clocking is no longer necessary. This may prove to be an important advantage when high-speed operation is considered.

One realization of the integrator using floating voltage reference is shown in Fig. 11. In this implementation, the capacitor C_3 is precharged to V_{DD} during integration phase Φ_1, and used as a floating voltage reference during reset phase Φ_2. In this figure, the input dc shift circuit (containing C_4) is also shown. Because the input capacitor C_1 is reset to V_{DD}, the compensating capacitor C_4 ($= C_1/2$) is used to cancel the inherent input dc offset and allows the effective input virtual ground to be at $V_{DD}/2$. In these very low voltage SC circuits where the opamp virtual ground is forced to an extreme bias voltage, either gnd or V_{DD}, such dc shift compensation is necessary at the input of the integrator.

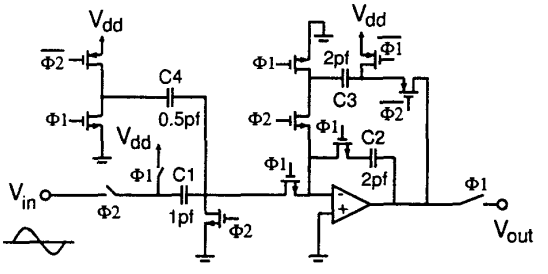

Figure 11: Floating reference implementation

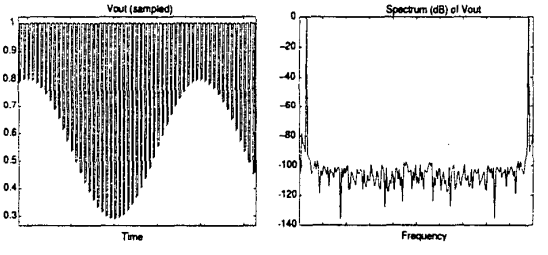

Figure 12: Simulated output (time and frequency)

A transient simulation with a sinewave input signal for this integrator using floating voltage reference is shown in Fig. 12. The input is a 5-kHz 0.2-V peak-to-peak sinewave operating with $V_{DD} =$ 1 V.

C. Integrator Using Master/Slave Stages—Yet another technique for avoiding charge leakage in the low-voltage integrator is to use an extra op-amp stage (slave integrator) for storing the charge during the reset phase when the integrating capacitor is floating. Fig. 13 shows the schematic diagram and required clock phases of such circuit in a pseudo-differential configuration. At the rising edge of Φ_2 (and Φ_{2a}), the signal charge stored in the master storage element C_{int} is transferred into the slave storage capacitor C_{intB}; at the rising edge of Φ_1 (and Φ_{1a}), the charge is returned into C_{int}. The sensitive nodes A and B (Fig. 6) are kept at or near the analog ground, and charge leakage is thereby prevented. This stage can use NMOS switches everywhere, since all switches operate at analog virtual ground. A drawback of the master-slave structure is the need for the second integrator stage (slave). However, it is possible to operate

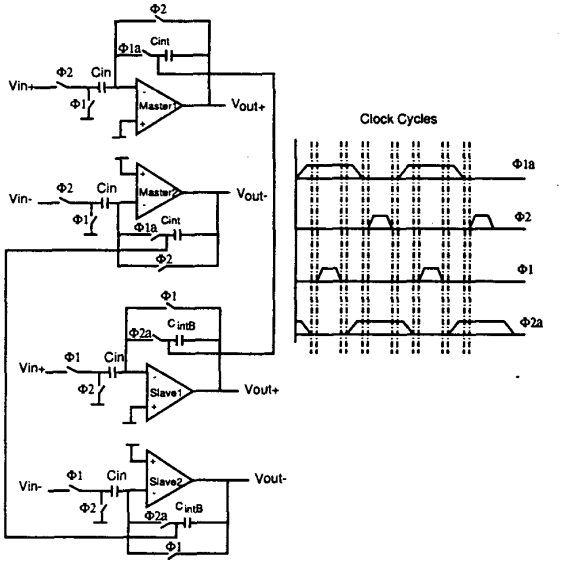

Figure 13: Master/slave integrator

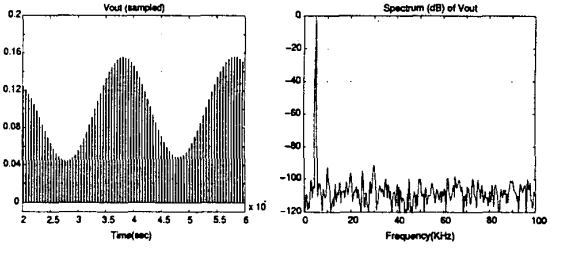

Figure 14: Simulated output (time and frequency)

the structure in a double-sampling mode, in which both integrators receive input charges in alternating clock phases. For such double-sampling circuit, the sampling rate can be doubled without increasing the op-amp bandwidth. The performance of this integrator was simulated in HSPICE. A macro

model, corresponding to a dc gain of 80 dB and a unity-gain frequency of 100 MHz was used for the opamp, and the switches were transistor-level models. The value of all capacitors were 2 pF, and the sampling frequency was 200 kHz. A 20-mV p-p 5-kHz sine wave was used as the input signal. Fig. 14 shows the output voltage in the time-domain for two periods and its spectrum of a larger data set. The low harmonic distortion verifies the absence of charge leakage.

IV. Low-Voltage SC Circuit Examples

In order to verify the proper operation of these low-voltage integrators, several of circuit designs are in progress. The design and simulation results of two benchmark switched-capacitor circuits are presented in the following. The circuit examples include $\Delta\Sigma$ modulator, and 1.5-bit per stage pipeline A/D converter.

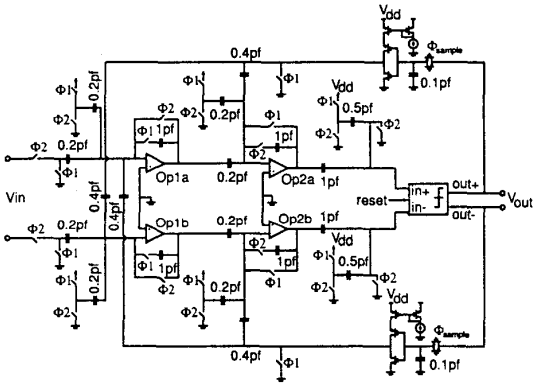

Figure 15: Low-voltage $\Delta\Sigma$ modulator

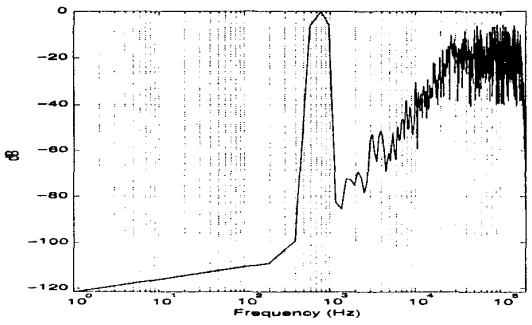

Figure 16: MATLAB results match HSPICE

A. 1.2-V $\Delta\Sigma$ Modulator—A second-order $\Delta\Sigma$ modulator operating with a 1.2-V supply was designed and simulated at transistor level using a 0.25μm CMOS models where V_{tn} = 0.7V and $|V_{tp}|$ = 0.9. The second-order modulator core is shown in Fig. 15. The example shown uses integrators with voltage-shifted clocking (refer to Fig. 7). A modulator using integrators with floating voltage reference (refer to Fig. 11) would look very similar with appropriate modifications. Note that the implementation is pseudo-differential. Given the limited power supply voltage, it is likely that this class of very-low-voltage SC circuits will have to use a pseudo-differential configuration due to high threshold voltages (unless, of course, the threshold voltages also scale down and are small relative to the supply voltage).

Also, for the sampling of the input signal, shown in the figure is a conventional floating input sampling switch. In a true low-voltage implementation, the input would be driven either by a similar low-voltage circuit (from another block on the IC) or by a low-voltage input sampling circuit that samples the signal coming from an external source to the IC. Such sampling circuit will be described later. The existing low-voltage IC implementations in switched-opamp technique use a passive resistor tied directly from the input to the virtual ground of the first opamp. This resistor-input circuit approximation is satisfactory only for an oversampling circuit.

Without the common-mode feedback (acceptable for simulation purposes), the first two hundred data samples of the $\Delta\Sigma$ modulator were simulated at the transistor-level. The first two hundred data samples match the spectrum (from MATLAB) shown in Fig. 16. The transistor-level simulations were done incorporating a low-voltage opamp.

B. Commonmode Error Accumulation—Due to the pseudo-differential structure which inherently lacks any common-mode feedback, each integrator used in the $\Delta\Sigma$ modulator is prone to common-mode error accumulation. This is because the integrator capacitor is never reset. From one cycle to the next any small amount of common-mode error (such as non-zero charge injection) is accumulated and stored on the integrating capacitor. Without common-mode compensation, given that

the source of common-mode error is fixed (dc), the opamp output will eventually saturate. In order to overcome this problem, a small amount of common-mode feedback is implemented. This is as shown in Fig. 17. The capacitors C_6 and C_7

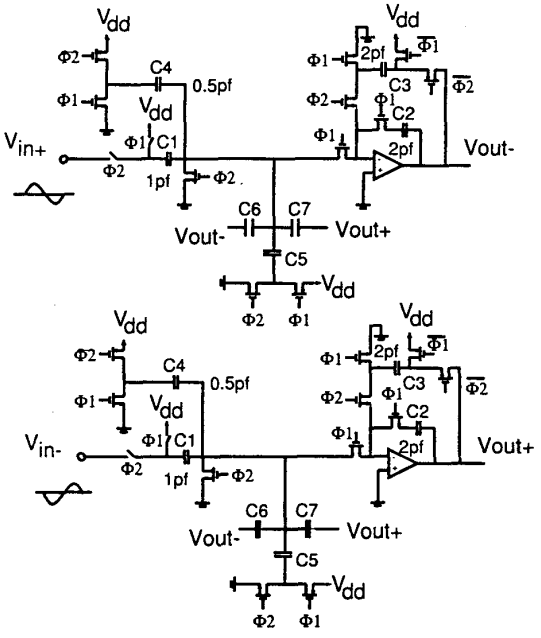

Figure 17: Pseudo-differential integrator with CMFB

sense/sample the output (pseudo-differential) common-mode voltage and C_5 does the dc shift compensation similar to input dc shift circuit discussed earlier. The capacitances of C_5 to C_7 are same and do not have to be very large. The common-mode feedback needs only to be enough to compensate for the common-mode error.

C. Nyquist Input Sampling Circuit—Thus far, we have excluded from the discussion a critical need for low-voltage input sampling circuitry. If the input signal to these low-voltage blocks are originating from another block within the IC, the same low-voltage SC techniques apply, but sampling a continuous-time input signal originating from external to the IC poses a critical problem. A resistor is often used to transfer the input signal to a very low-voltage switched-capacitor circuit in order to avoid having to implement a low-voltage sampling circuit [4] [8]. This is acceptable since it is not critical for an oversampled converter to utilize Nyquist input sampling, but the issue becomes more critical as oversampling ratio is reduced and when the need extends to Nyquist A/D converters.

A simple implementation of Nyquist input sampling for low-voltage is shown in Fig. 18. It is

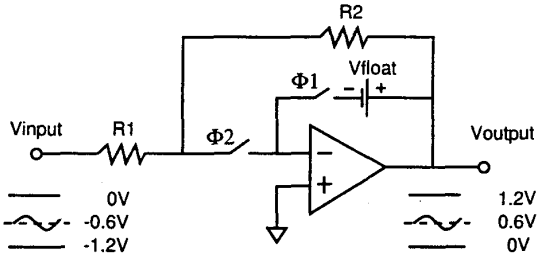

Figure 18: Nyquist input-sampling circuit

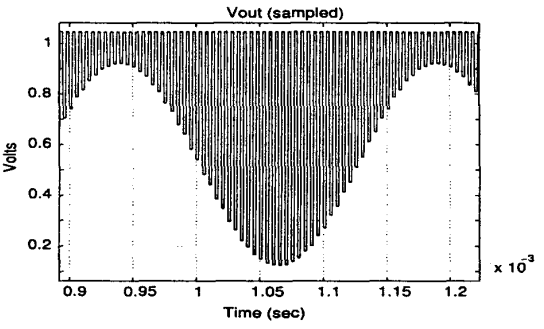

Figure 19: Input-sampling circuit output

simply an inverting gain stage (with a fixed gain of -1) when the signal is being sampled by the following low-voltage switched-capacitor stage, but in the opposite phase the opamp resumes unity-gain configuration for reset. Fig. 18 also utilizes a floating voltage reference so that it is consistent with the rest of the switched-capacitor circuit (refer to Fig. 11). The HSPICE simulation results shown in Fig. 19 verify its proper operation. One drawback of this Nyquist sampling circuit is that the input range is shifted to 0 to $-V_{DD}$ range. The signal source external to IC will have to be able to provide such shift, and the bonding pad cannot allow the forward-bias ESD diode from ground. Due to the input series resistor (e.g. poly) we would anticipate a reasonable ESD protection if used with a reverse breakdown diode for negatively-charged ESD protection. It is possible to have the input range between ground and V_{DD}

with additional circuitry [12], but with an added possibility for sampling error.

D. Pipeline A/D Converter—In addition to circuits using integrators, a fast low-voltage pipeline A/D converter has also been designed and simulated. A 20-Ms/s 10-bit 1.5-bit/stage pipeline ADC (with digital redundancy) was chosen for speed benchmark. Many of the the low-voltage switch issues are identical to those of low-voltage switched-capacitor integrators, while some are simplified. One fundamental difference between the low-voltage integrators and the gain stage used in the pipelined A/D converter is illustrated in Fig. 20. Notice the

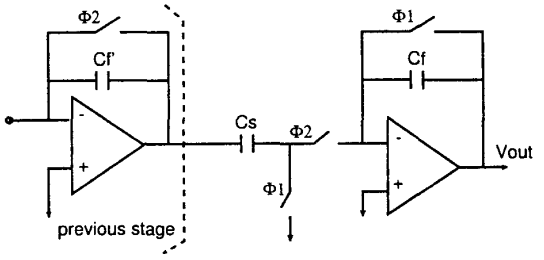

Figure 20: Low-voltage SC gain stage

simplification for the reset phase. Because a fixed gain stage does not require maintaining an integrated charge, a series switch (Fig. 6) for the integrating capacitor is no longer needed and the forward biasing problem of p-n junction (diffusion to well) is eliminated.

The key repetitive block in the 1.5-bit/stage pipelined A/D converter, the residue-multiply-by-two circuit, has been designed for low-voltage operation and its overall structure simulated. For this key structure, shown in Fig. 21, in single-ended configuration for illustration purposes, 0 or $\pm V_{ref}$ injection is implemented by a separate set of capacitors. This was done to avoid the use of floating switches as in a conventional residue amplification block. Also shown in the figure is the dc offset compensation block (capacitor C_{com}) which sets the effective input common-mode at $V_{DD}/2$.

As discussed in the context of pseudo-differential integrators, the pipelined ADC structure also faces the common-mode accumulation problem. This is due to the cascade of fixed 2x gain in each of the residue amplification. In pseudo-differential structure without common-mode feedback, the common-

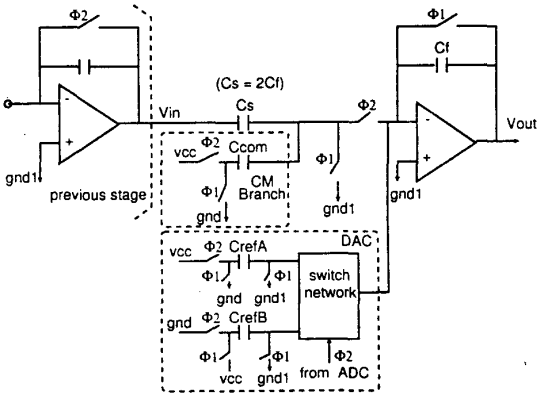

Figure 21: Residue-multiply-by-two circuit

mode gain is same as the differential gain. For a 10-bit converter example, where there are nine residue amplification stages, the initial common-mode error will see a total gain of $2^9 = 512$. It is impossible to insure that the common-mode error be small enough for such common-mode gain. This common-mode accumulation problem is resolved by cross-coupling the feedback capacitors, as shown in Fig. 22. The cross-coupling capacitors

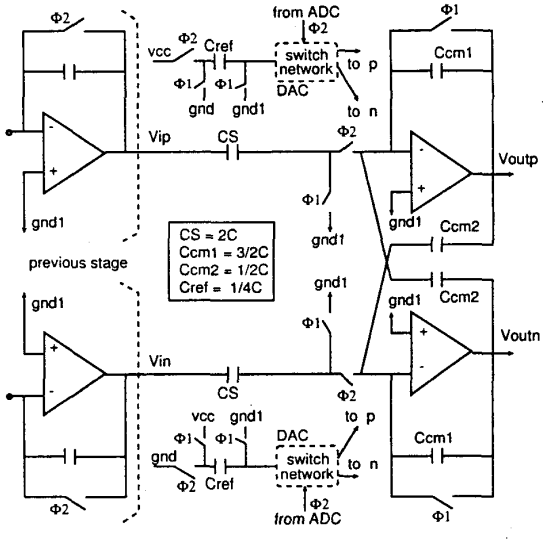

Figure 22: Residue-x2 circuit with CM compensation

establish a mild positive feedback in parallel with the standard negative feedback. The net differential gain is maintained (x2), but the net common-mode gain has now been reduced to one. This guarantees that the common-mode error injected at any point in the converter is no longer ampli-

fied. The capacitor values may be manipulated to reduce the common-mode gain to less than one (achieving common-mode attenuation), but with increased capacitive loading. A common-mode gain of one has been found sufficiently small for a reasonable amount of anticipated common-mode errors.

Finally, shown in Fig. 23 is the transistor-level HSPICE simulation result for a 10-bit pipelined ADC implemented with a cascade of nine 1.5-bit/stage stages. Multiple simulation results indicate an SNDR of 65-70 dB. The input signal is full-scale and the sampling rate is 20 MS/s for $V_{DD} = 1.5$V. The low-voltage architecture will allow the operation down to 1-V level, but current opamp design limits the operational bandwidth for a very low-voltage power supply.

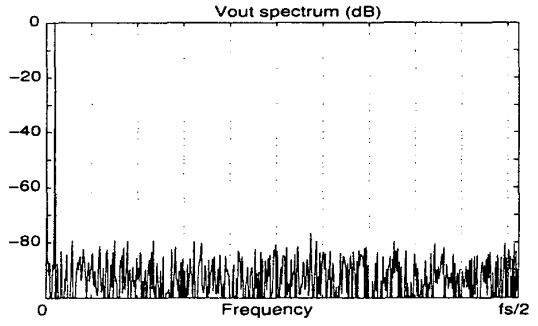

Figure 23: Simulated spectrum of 10-bit ADC

V. Conclusions

A brief overview of existing low-voltage switched-capacitor circuit techniques were presented. In the context of today's aggressive down scaling of CMOS processes, new low-voltage switched-capacitor circuit techniques were proposed. The newly proposed methods allow larger signal swing without the significant reduction of the operating speed, and hence are appropriate for future submicron low-cost low-voltage CMOS technologies. Design examples of a second-order $\Delta\Sigma$ modulator and a 20 MS/s 10-bit 1.5-bit/stage pipelined A/D converter demonstrate the practical capability of the new low-voltage SC circuit techniques.

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