A Two-Chip Interface for a MEMS Accelerometer

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***Abstract*—A proposed third-order noise-shaping accelerometer interface circuit enhances the signal-to-noise ratio, compared with previously presented interface circuits. The solution for the two-chip implementation is described and a novel cross-coupled correlated double sampling integrator is proposed. This scheme functions even with large parasitic capacitances between the sensor and the interface circuit. The op-amp noise is first-order shaped. Dithering circuit is also implemented on the chip, fabricated in an 1.6-μm CMOS process.**

***Index Terms*—Accelerometer, correlated double sampling (CDS), delta–sigma modulator, dither, sensor interface.**

I. Introduction

MODERN micromachining technology allows the fabrication of mechanical sensors on a chip. A successful application is the accelerometer, widely used in automobile air-bag systems. This is basically a capacitive sensor, but its capacitance is quite small. There are several ways to sense the capacitance accurately. Our previous result [1] shows that one can use the sensor as the input capacitor in the delta–sigma loop. The other solution using the delta–sigma loop is based on force feedback [2], [3]. For the accelerometer, force feedback is attractive, since it offers the potential of wide dynamic range [4]. Recently, we introduced a two-chip implementation of a capacitive sensor interface circuit, intended especially for the accelerometer [5]. However, practical circuit implementation incorporating $1/f$ noise and offset voltage reduction was not shown yet.

In Section II, we review a new noise-shaping structure with higher loop gain and three-level force feedback. In Section III, we show how to obtain a two-chip implementation. In Section IV, a novel fully differential cross-coupled integrator is described. It allows a large parasitic capacitance at the input of the op-amp and includes correlated double sampling (CDS) to reduce $1/f$ noise and cancel offset voltages. A practical way to apply dithering is described in Section V. Our conclusions are given in Section VI.

II. Third-Order Structure

Fig. 1 shows the proposed structure for the sensor interface circuits [5]. The main departure from earlier structures [2], [3] is the additional integrator in the loop. The dynamics of the sensor gives no noise-shaping at low frequencies. That means that the signal-to-noise ratio (SNR) is determined by the sensor gain and resonance frequency. The integrator is added for additional noise shaping to get a higher SNR at low frequencies, and the op-amp noise, amplified due to the large parasitic capacitance between the chips, is also first-order shaped. A novel three-level force feedback with mismatch shaping enables the use of a simple digital compensator for this high-order noise-shaping structure [5].

To implement the interface circuit separately, we have to solve the problems arising from stray capacitance due to the wiring between sensors and circuits. These are discussed in the next Section. A fully-differential cross-coupled integrator with CDS is proposed in Section IV to solve these problems.

III. Two-Chip Implementation

Even for an on-chip sensor or a surface MEMS sensor, for low-noise op-amps, the parasitic input capacitance can be several pF large [3]. For two-chip implementation, it can be as large as 10–30 pF. To minimize the problems due to the large parasitic capacitance, the following basic rules must be satisfied.

- The floating terminal of the parasitic capacitor must not be reset to a dc potential in any clock phase.
- No series switch must be placed between the parasitic capacitor and the input terminal of the op-amp.
- The front-end circuit block should not be an amplifier, but an integrator.

Next, the reasons for these rules will be discussed.

A. Rule 1: Offset Sampling

The first rule holds because switching or resetting the large parasitic capacitor creates a large error charge flow since the input potential of the op-amp is not exactly at ground. In Fig. 2(a), the voltage V_A at Ⓐ contains an offset voltage, kT/C and $1/f$ noise, and also some signal due to the finite op-amp gain. After resetting C_p with S_1 and opening S_1 again, the error charge C_pV_A will flow into the feedback capacitor C_f.

B. Rule 2; kTC Charge Noise

The second rule must be satisfied in order to minimize the effect of the kTC charge noise caused by the resistance of the switch. In Fig. 2(b), the switch S_2 between the parasitic capacitor C_p and the input terminal creates a noise voltage with a mean-square value kT/C_p, which leads to an rms noise charge $\sqrt{kTC_p}$. This is large if C_p is large. For example, an input capacitor $C_{\rm in} = 1$ pF causes 64 $\mu V_{\rm rms}$ of kT/C noise, but the charge noise from a parasitic capacitor $C_p = 20$ pF, referred back to the input, is as large as 287 $\mu V_{\rm rms}$, more than four times

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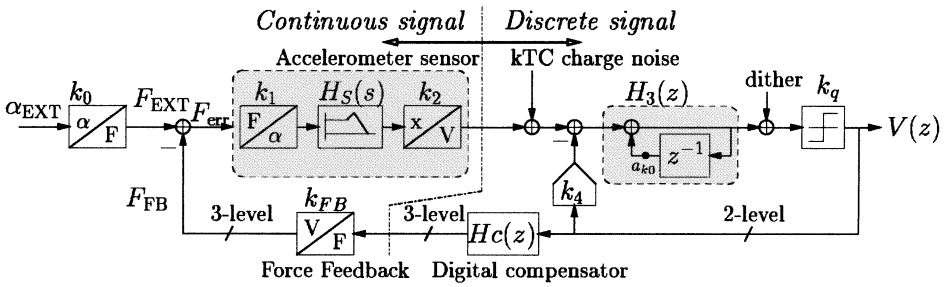

Fig. 1. Third-order sensor circuit block.

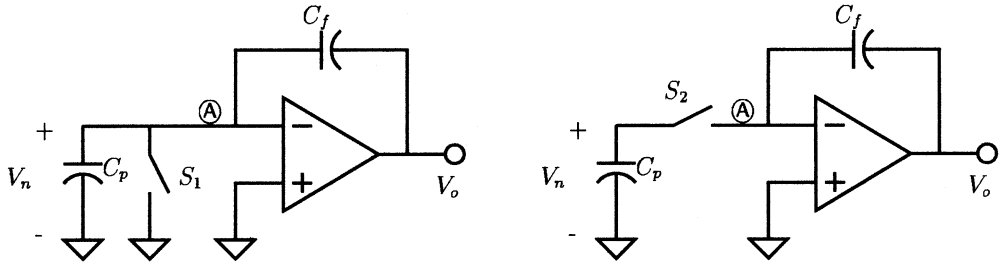

Fig. 2. Problems occurring for SC stages with a parasitic capacitor.

larger than the kT/C noise of the input capacitor. Even for only $C_p = 2$ pF, the input-referred noise due to C_p is 91 $\mu V_{\rm rms}$, 50% larger than that due to $C_{\rm in}$.

The noise is sampled by S_2, and will appear at the output of the op-amp. The bandwidth of this kTC_p charge noise is determined by the op-amp. The power spectral density is given by

$$S^{S/H}(\omega) \propto [kT(R_{\rm on} + R_{\rm eq})\omega_0 {f_s}^2] \left(\frac{1}{\omega_2}\right)\left(\frac{C_p}{C_f}\right), C_p/C_f \gg 1 \quad (1)$$

where $\alpha = C_p/C_f$, $R_{\rm on}$ is the on-resistance of the switch S_2, $R_{\rm eq}$ is the equivalent resistance for the input-referred op-amp noise, ω_0 is a unity gain frequency of the op-amp, and f_s is a sampling frequency [6]. Equation (1) indicates that the noise from the parasitic capacitance is large at low frequencies, and it increases with C_p/C_f if the switch S_2 is present.

C. Rule 3: Op-Amp Noise

To understand the third rule proposed above, consider a standard SC integrator and an amplifier, with the large parasitic capacitance at input node of the op-amps. Their noise performance was simulated in HSPICE. The generation of the noise voltage for the op-amp and the post-processing were performed using MATLAB, and the noise source was imported as a piece-wise linear voltage source into HSPICE. The noise changed at least 10 times in each clock period so that it behaved as a continuous-time signal. The op-amp's dc gain was assumed to be 60 dB, and its bandwidth 5 MHz. The clock rate was 1 MHz.

The output noise spectrum and the input-referred noise spectrum for each case are shown in Fig. 3. The parasitic capacitor C_p amplified the op-amp noise in both cases, but, due to integrating action, the input-referred noise of the integrator is much smaller than that of the amplifier. Hence, for measurements of low-frequency signal, it is better to use the integrator for the front-end circuit block in the sensor interface circuits.

IV. Fully Differential CDS Integrator

A novel CDS circuit is shown in Fig. 4. C_{S1} and C_{S2} are on the sensor chip, which contains several switches. The rest of the components are on the interface chip, except for the large parasitic capacitors C_{p1} and C_{p2}. The cross-coupled input branches modulate the common-mode signal injected from the common-plate node. When the common terminal of the sensor is switched, a large common-mode signal along with the small sensor signal is injected into the feedback capacitors C_{f1} and C_{f2}. That large common-mode signal is subtracted during $\Phi 2$ and $\Phi 4$ due to the cross-coupling. At the same time, the differential signal (sensor signal) is doubled.

The basic principle of operation [7] is that if the input and feedback capacitors $C_{S1,S2}$ and $C_{f1,f2}$ are connected to the virtual ground while switches at the input-side terminal of $C_{S1,S2}$ are toggled between $V_{\rm in}$ and ground, then the magnitude of the charge entering the feedback capacitors $C_{f1,f2}$ will be (to a very good approximation) $C_{S1,S2} \cdot V_{\rm REF}$, independent of the slowly varying components (offset, $1/f$ noise, and signal) of the op-amp input error voltage. If, afterwards, the feedback capacitors are disconnected, then their charge injection is independent of the input signal and causes only a small constant offset at the output. Thus, the charge integration is nearly ideal.

Detailed circuit operation is as follows. Before the input switches are toggled between the ground and $V_{\rm REF}$ (from $\Phi 1$ to $\Phi 2$ and from $\Phi 3$ to $\Phi 4$), the input capacitors $C_{S1,S2}$ are reset by

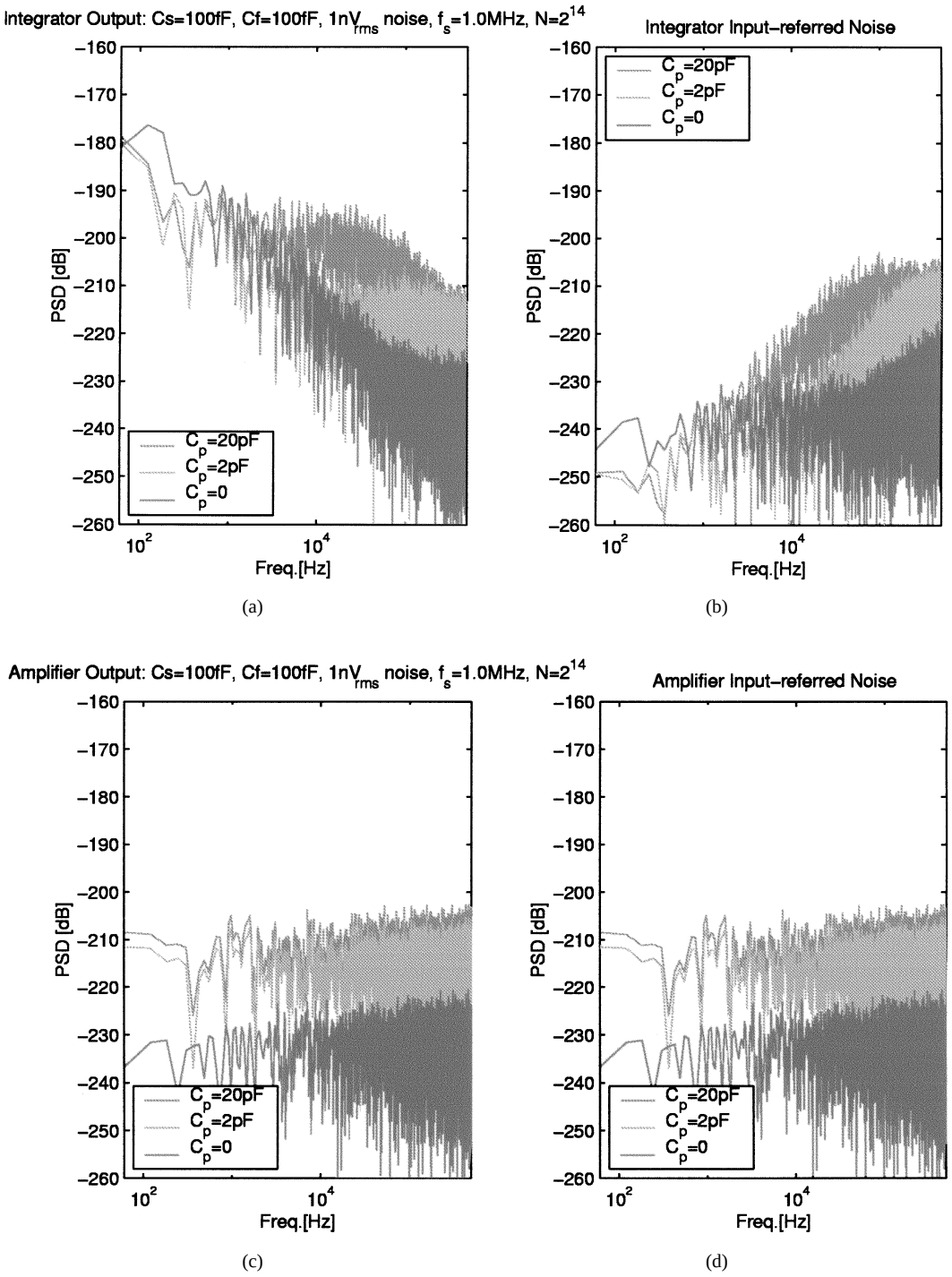

Fig. 3. (a) Output noise of an integrator. (b) Input noise of an integrator. (c) Output noise of an amplifier. (d) Input noise of an amplifier.

the right-hand side switches during $\Phi 1$ and $\Phi 3$. The integrating capacitors $C_{f1,f2}$ are disconnected during $\Phi 1$ and $\Phi 3$, but the holding capacitors $C_{h1,h2}$ hold the previous outputs. When the switches next to $C_{f1,f2,h1,h2}$ are toggled, the right-hand-side switches of the input capacitors remain closed. During this period, the op-amp's input node voltage (due to offset voltage, noise, and finite op-amp gain) is stored in $C_{S1,S2}$. Hence, the sampled charge delivered by $C_{S1,S2}$ to $C_{f1,f2}$ at $\Phi 2$ and/or $\Phi 4$ is not affected by the voltage at the input node.

As described in the previous section Section III, the parasitic capacitance is not reset in the circuit of Fig. 4, and there is no series switch between the parasitic capacitors and the input terminal of the op-amp. The integrator is used to shape the op-amp noise as well.

V. Dithering

Since the input signal of the accelerometer is usually at very low frequencies, tone generation may occur in the loop.

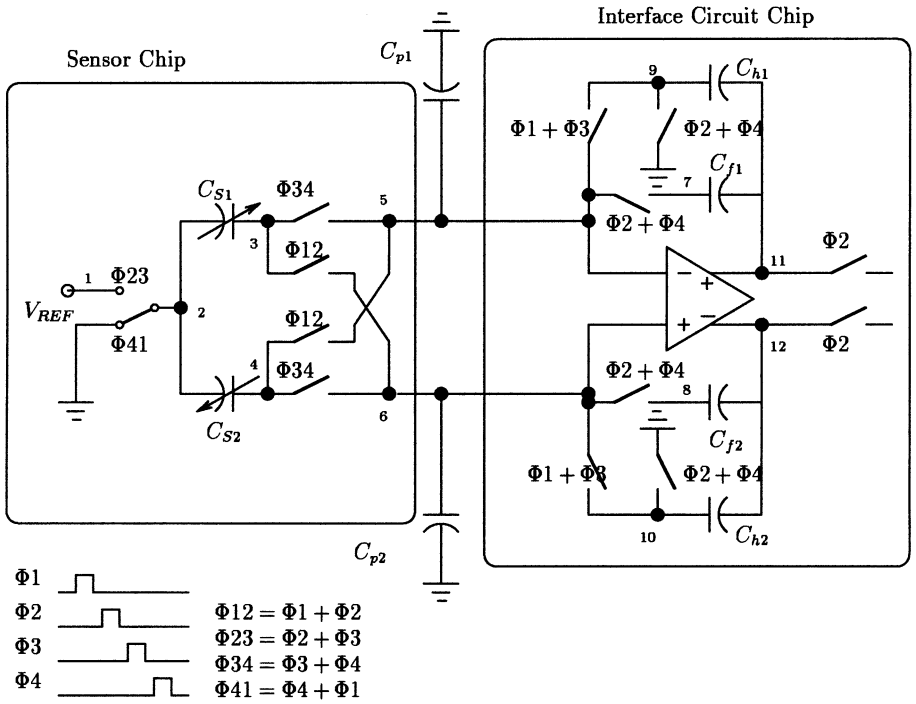

Fig. 4. New CDS fully differential circuit.

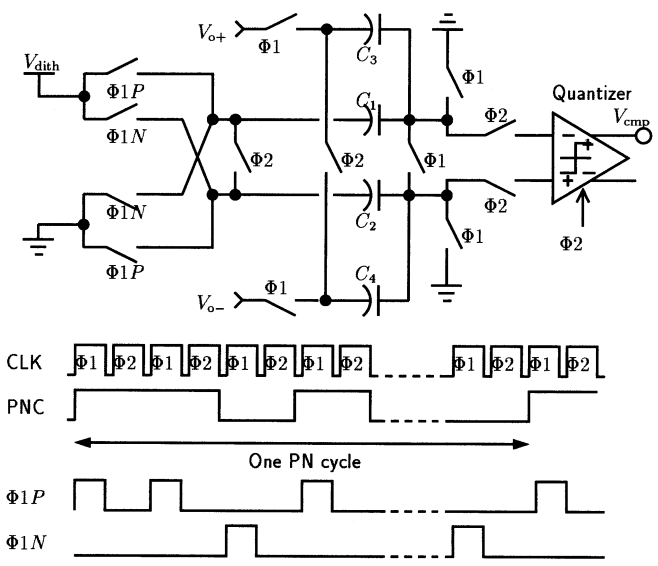

Fig. 5. Dithering circuit.

Dithering signal helps to reduce such tones in the band of the interest.

There are several ways to implement dithering. Thermal noise of the pn junction can be used for generating the dither signal [8]. However, it is better to use a pseudo-random sequence in a digital circuit for testability and repeatability. This was done here.

Fig. 5 shows the circuit used in the actual interface chip. $C_{1,2,3,4}$ are used to sample the output of the op-amp and the dither signal. Those two signals are added at the input of the quantizer. The random sequence is controlled by a digital pseudo random noise code (PNC). It is easily obtained using shift registers. The dither voltage level is determined by the constant voltage $V_{\rm dith}$. $V_{\rm dith}$ can be supplied by a simple single-ended voltage source. It is modulated by the PNC and added to the signal from the integrator at the quantizer input. The left-hand terminals of the sampling capacitors are tied together to cancel the common-mode voltage.

Fig. 6 shows the simulation result using MATLAB. It shows that the SNR is much improved with dithering, especially at small accelerations. It reduces the SNR slightly for large inputs.

The interface chip was designed for the AMI 1.6-μm CMOS process. It is now under test.

VI. Conclusion

A new interface circuit containing a novel fully differential CDS integrator was proposed. It allows large parasitic capacitors, and is effective in the presence of large common-mode charge as well as common-mode noise.

A practical dither circuit was also shown. Even though the third-order delta–sigma structure helps the noise-shaping, only first-order behavior can be expected in the band of interest. Since the sensor signal is very close to dc, tones will affect the SNR ratio. Hence, dithering helps to improve the SNR.

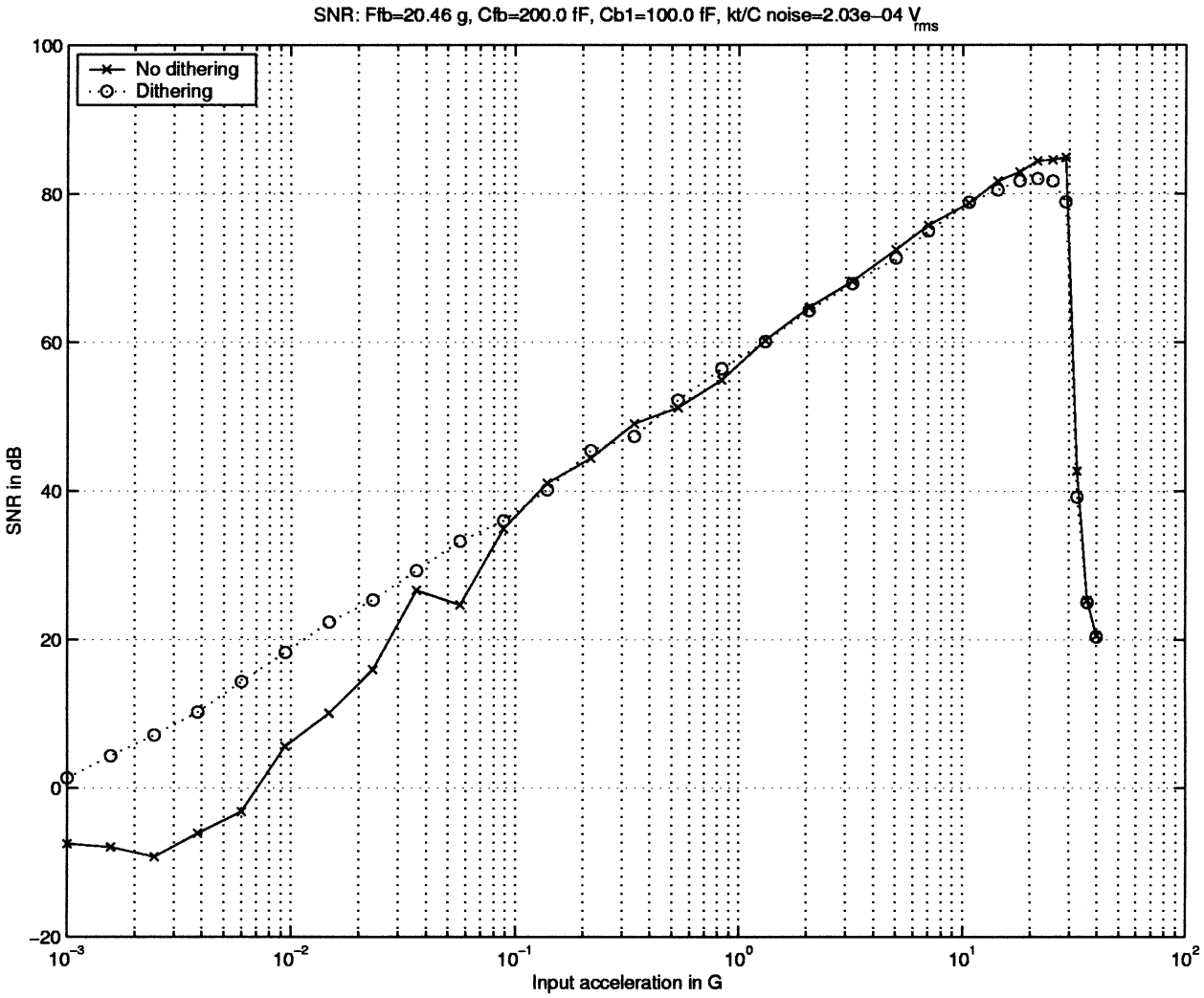

Fig. 6. SNR versus input acceleration with and without dithering.

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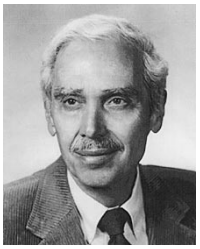

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