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EFFICIENT COMMON-MODE FEEDBACK CIRCUITS FOR PSEUDO-DIFFERENTIAL SWITCHED-CAPACITOR STAGES

L. Wu, M. Keskin, U. Moon and G. Temes

Electrical and Computer Engineering, Oregon State University
OSU, ECE-220, Corvallis, OR 97331-3211

ABSTRACT

Novel common-mode feedback circuits are proposed for use in pseudo-differential switched-capacitor circuits. They can be implemented by incorporating just four additional capacitors (and switches) for an integrator, and only two additional capacitors for a residue gain amplifier. The circuits are applicable to very low-voltage switched-capacitor stages realized in submicron low-voltage CMOS processes.

1. INTRODUCTION

Fast-moving technological advancements in fine-linewidth submicron CMOS process have benefitted digital VLSI. The continually increasing level of integration with steadily rising clock rates allows the implementation of more sophisticated and powerful digital systems on a single IC. While this positive trend of technological achievement promises great things in the digital arena, one of the key *analog* limitations of state-of-the-art submicron CMOS technologies remains the restricted power-supply voltage, limited by the low junction breakdown voltage of the high density CMOS process and by the thin gate oxide, prone to voltage stress and breakdown. Even beyond this fundamental limitation for analog circuit design, in a growing number of portable applications, the available external power source may also limit the supply voltage (e.g. external power source may be a 1.2 V battery with an end-of-life voltage of only 0.9 V).

In many analog and mixed analog-digital circuits, the circuit technique that is most commonly used for analog signal processing is based on switched-capacitor (SC) stages. They are used in many practical applications, such as data conversion (in both Nyquist-rate and oversampled $\Delta\Sigma$), analog filters, sensor interfaces, etc. However, there are fundamental limitations on the operation of switches when the supply voltage becomes less than the sum of the absolute values of the PMOS and NMOS threshold voltages. This is illustrated in Fig. 1. With a switch connected to a signal voltage (*floating switch*) that is about half-way between the rail voltages (0 V and V_{DD}), and $V_{tn} + |V_{tp}| > V_{DD}$, it is not possible to turn the switch *on*, even if a CMOS transmission gate is used to realize it.

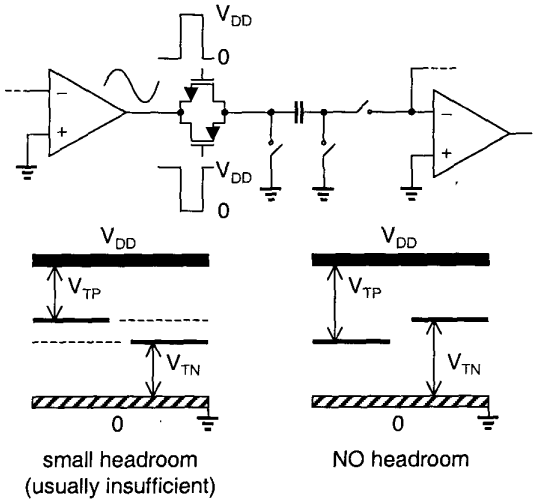

Figure 1: Fundamental problem of a CMOS switch

There are currently only a few solutions that are free of any high-voltage reliability issues. They are the switched-opamp technique [2] and the *unity-gain-reset* (UGR) technique described in [6]. While the switched-opamp approach suffers from speed limitation due to the transients introduced by the required power-up/power-down of the opamp output stage, the new unity-gain-reset technique may operate at much higher speeds by keeping the opamp in its active operating region at all times.

In both of these true low-voltage switched-capacitor circuit techniques, due the low headroom (power supply) in comparison to the transistor threshold voltages, the circuits are forced to operate with a very low (or high) virtual ground potential so that only the NMOS (or PMOS) transistors could be used as switches. Even though a fully-differential structure is implementable, as demonstrated in [5], due to the resetting mechanism during one of the two alternating clock phases, the *continuous-time* common-mode feedback circuit must power-up and settle within one phase (1/2 of clock

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period). This naturally leads to using pseudo-differential structures for IC implementation. In the following sections, we will summarize both switched-opamp and UGR techniques, and in the context of the unity-gain-reset technique (but applicable to both techniques), a simple but effective common-mode feedback compensation scheme is described.

2. LOW-VOLTAGE INTEGRATOR

The topology of the low-voltage UGR integrator [6] is illustrated in Fig. 2. Note that the floating switch of the conventional integrator is eliminated (just as in switched-opamp circuit) and the operation of the grounding/resetting switch used both in conventional and switched-opamp circuits is replaced by connecting the sourcing opamp in unity-gain configuration. The key concept in this new topology is the simple idea to keep the opamp fully operating at all phases, thereby avoiding *switching* the opamp *off* as in the switched-opamp technique. Several circuit realizations of this basic new integrator topology have been found, and they are discussed in references [6]-[7].

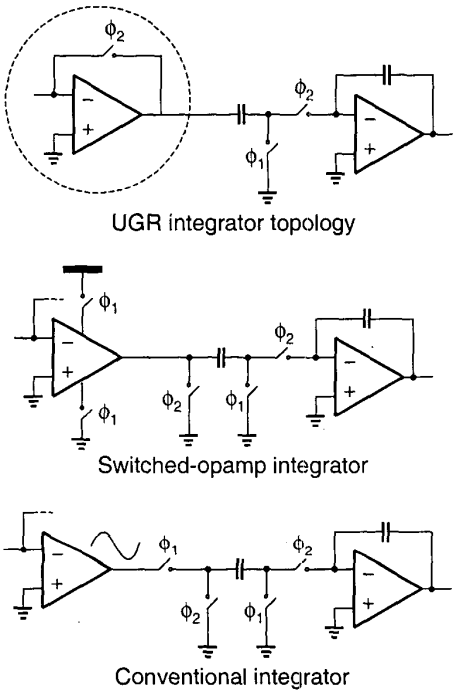

Figure 2: Low-voltage integrator topology

In the new integrator (and also the switched-opamp integrator), a common issue is that because the signal virtual ground is near the lowest potential ($\approx 0\ V$), there is a constant amount of dc offset charge injected in every clock cycle. For example, if the opamp operates with an output bias $V_{DD}/2$, in every phase ϕ_1 the dc offset voltage $V_{DD}/2$ is sampled into the input capacitor, and the charge is transferred to the integrating capacitor during phase ϕ_2. Typically this dc offset injection problem is overcome by a separate dc offset injection circuit providing charge of opposite polarity. As circuit components are never perfectly matched, due to the inaccurate cancellation of the input dc offset and to uncancelled charge injection from switches, there will be uncancelled dc offset charge (common-mode signal in a pseudo-differential configuration) injected into the integrating capacitor in every clock cycle. As this common-mode error is a dc value, over time the opamp will eventually saturate either to the negative or to the positive supply rail. This necessitates a common-mode feedback even for the pseudo-differential integrator.

The pseudo-differential integrator complete with common-mode feedback is shown in Fig. 3. Without the capacitors

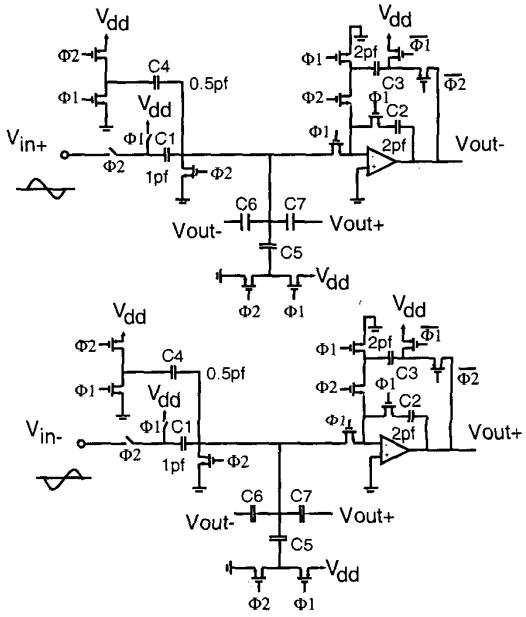

Figure 3: Pseudo-differential integrator with CMFB

C_5, C_6, and C_7, the integrator is made up of two single-ended integrators operating in parallel without common-mode feedback. In this pseudo-differential configuration, capacitor C_4 functions as the dc offset correction circuit, and capacitor C_3 functions as a floating voltage reference such that the opamp output is reset to V_{DD} instead of ground. Once again, reader is referred to [6] for the details of this this implementation.

Our main point of interest here is the common-mode feedback circuit, which contains capacitors C_5, C_6, and C_7. Note that during phase ϕ_2 the common node of these three capacitors is pulled to ground, while both opamp outputs (tied to capacitors C_6 and C_7) are set to V_{DD}. At phase ϕ_1, when the opamps are operating at the integrating mode, the

average of the opamp outputs is set to $V_{DD}/2$ if there were no common-mode offset error. Due to this shift, the capacitor C_6 and C_7 injects a negative charge $-(C_6 + C_7)V_{DD}/2$ into the virtual grounds of each opamps. The capacitor C_5 neutralizes this charge by discharging (precharging) to ground during phase ϕ_2 and charging to V_{DD} during phase ϕ_1, thus delivering a positive charge equivalent of $C_5 V_{DD}$. The nominal capacitance of all three capacitors is the same. Now, if there is any common-mode error accumulation at the outputs of the opamps, the net value of the charges injected into the virtual grounds of the opamps will act to correct for the error. The capacitors C_5, C_6, and C_7 only need to be large enough to compensate for the small amount of common-mode error that is injected in every clock cycle, and the bandwidth of this common-mode feedback loop does not need to be wide.

An HSPICE simulation of the proposed common-mode feedback implementation is shown in Fig. 4. A small amount

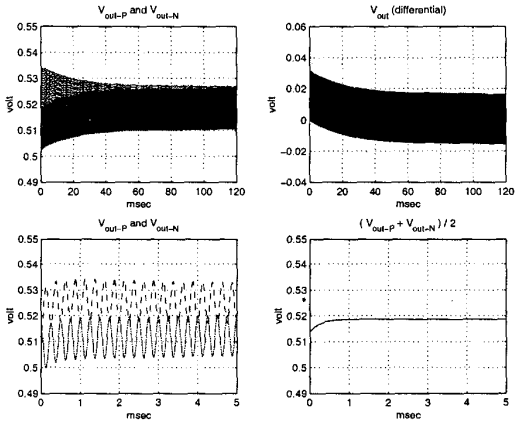

Figure 4: Pseudo-differential integrator CMFB settling

of common-mode error at the beginning of the transient simulation is shown to be corrected over multiple clock cycles. This simulation was performed in the context of a $\Delta\Sigma$ modulator where a small amount of differential offset initial condition is also shown to settle to zero.

The common-mode feedback described above is also directly applicable to pseudo-differential switched-opamp circuits, as the resetting operation (typically to a low potential such as ground or to high potential such as V_{DD}) of the opamp output is common to both the switched-opamp and UGR techniques.

3. LOW-VOLTAGE RESIDUE AMPLIFIER

In other circuits and applications there is also a need to correct for common-mode error accumulation. One such example is the pipelined A/D converter structure. In the pipelined architectures, the signal path includes a cascade of residue amplification stages. Thus, when a small amount of common-mode error is injected at some point, that error will propagate throughout the pipeline and will experience a significant amount of gain by the time it reaches the end of pipeline. Specifically, for a single-bit per stage architecture where the residue amplification is by *two*, by the time the common-mode error has propagated over ten gain stages (as it would for an 11-bit converter), the total gain would be $2^{10} \approx 1000$! While this does not happen in a cascade of fully-differential amplification stages, in the pseudo-differential configuration the differential gain of two parallel paths (positive and negative signal paths) is the same as the common-mode gain, i.e. the single-ended gain.

A low-voltage pseudo-differential 2X residue amplifier suitable for use in a pipelined analog-to-digital converter (ADC) is shown in Fig. 5 [8]. The necessary compensation

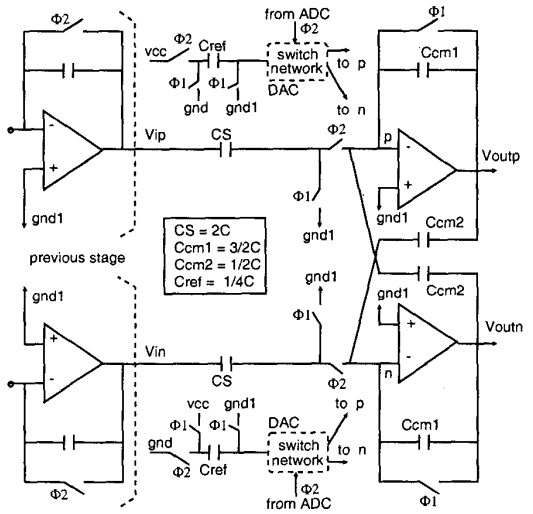

Figure 5: Residue-x2 circuit with CM compensation

for the common-mode offset accumulation is incorporated in the schematic. The cross-coupling of the opamp feedback capacitors performs the task of controlling the common-mode error accumulation. The branches shown separately at the top and bottom of the figure are the $\pm V_{ref}$ injection circuits. Due to a very low-voltage operation, they could not be incorporated into the signal path, as is commonly done in the conventional multiplying digital-to-analog converter (MDAC) implementation. The details of this circuit and the application in a A/D conversion system are described in [8]-[9].

The key aspect of the residue amplifier shown in Fig. 5 is how the cross-coupling of capacitor controls the differential and the common-mode gains in different ways. The cross-coupling allows a small amount of differential positive feedback which makes the differential gain of this circuit $C_S/(C_{cm1} - C_{cm2})$. (Note the subtraction!) Since the

positive feedback is only applied differentially, the common-mode gain of this circuit is $C_S/(C_{cm1} + C_{cm2})$. Using the capacitance values shown in Fig. 5, the net differential gain is $2C/(1.5C - 0.5C) = 2$ and the common-mode gain is $2C/(1.5C + 0.5C) = 1$. Also note that the dc offset injection circuit, discussed earlier, is not used in this structure as the combination of C_{cm1} and C_{cm2} achieves the same net effect. Given the reduced common-mode gain equal to 1 in this example, all common-mode errors injected at any point in the pipeline propagate to the next stage *without* any magnification. We found that the cumulative effect of nine gain stages without multiplicative effect was satisfactory for a 10-bit ADC.

The proper operation of the common-mode error suppressing method was verified in a transistor-level HSPICE simulation, using the cascade of residue amplifier stages in a 10-bit pipelined ADC. Shown in Fig. 6 is the FFT plot of a transient simulation with a full-scale sinusoidal input signal. The simulation result indicates a better than 70 dB

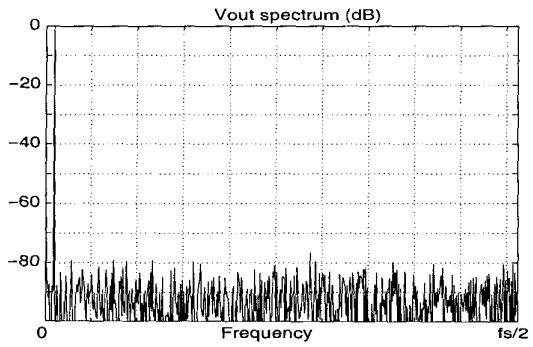

Figure 6: Simulated spectrum of 10-bit ADC

SNDR performance for a 20 MS/s conversion speed and a 1.5-V power supply. Incorporating capacitor mismatches and other nonideal effects, we anticipate the overall SNDR performance at a 60 dB level.

Final points to note is that is it possible to make the common-mode gain less than 1 (any gain value less than the differential gain is possible). For example, setting $C_{cm1} = 2.5$ and $C_{cm2} = 1.5$ reduces the common-mode gain to 0.5, while maintaining a differential gain of 2. Also, these techniques are directly applicable to pseudo-differential switched-opamp configurations.

4. CONCLUSIONS

Two methods were presented for suppressing and controlling the effects of common-mode error accumulation in low-voltage pseudo-differential switched-capacitor configurations. Both implementations are of cost effective as they only require a few added switched capacitors. For integrators that may be used in systems such as the $\Delta\Sigma$ modulator, the common-mode error is cancelled by a local CMFB circuit made up of four capacitors. In the common-mode compensation of a residue amplifier block, such as the one used in a pipelined ADC, a cross-coupled pair of feedback capacitors allows controlled common-mode gain of any value smaller than the gain of the differential residue amplification.

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