EFFICIENT ERROR-CANCELLING ALGORITHMIC ADC

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ABSTRACT

An algorithmic ADC that is insensitive to capacitor mismatch and finite opamp gain and offset is described. Using the *differential sampling scheme* with the correlated double sampling (CDS) technique together, the virtually error-free and fast multiply-by-two operation is obtained for the proposed ADC. For an N-bit converter, a new output word is obtained every $4N$ clock periods, and this represents a significant improvement in conversion speed (or efficiency) in comparison to the latest work to achieve the same error compensation. Thus it can be used in the applications which require low-cost medium-speed and high-resolution A/D conversion.

1. INTRODUCTION

Driven by the need for low-power and high-resolution data converters, a number of error-compensating techniques have been developed [1]-[4]. The key concept behind all these techniques is to manipulate the switching of capacitors ,which contain the signal charges (or other unit elements) in ways such that the randomly mismatched values will not affect the accuracy of the data conversion. Most of these techniques also account for the input-referred offset voltages of the opamps used in the signal processing. And in the most recent work reported [4], the finite gain of the opamp is also compensated (effectively squaring the opamp gain) at the cost of many additional clock phases.

This algorithmic ADC combines toghter the CDS technique [7] and capacitor-ratio-independent technique to obtain high resolution A/D conversion. The proposed *differential sampling scheme*, which performs virtually error-free multiply-by-two operation, is to sample $2V(i)$ into the same capacitor by recharging it from $V(i)$ to $-V(i)$, which is sourced from the inverting output terminal of the fully differential structure. Using this technique for a N-bit conversion, a new output word is obtained every $4N$ clock periods. Prior efforts in this area have needed 6 and 3 clock periods per bit to achieve capacitor mismatch error cancellation [1][3], which are requiring high-gain opamps to obtain high-resolution conversion. The most recent work also incorporating finite opamp gain compensation needs 7 clock periods per bit [4]. Thus, this new scheme is a significant improvement over existing implementations.

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2. CONVERTER STRUCTURE

A standard 1-bit/cycle algorithmic ADC structure is shown in Fig. 1. In the first cycle, $V(1) = V_{in}$, and thereafter the S/H output voltage is doubled in amplitude and added to a reference, resulting in $V(k+1) = 2V(k) + b(k)V_{ref}$. Depending upon the polarity of the bit $b(k)$, either $+1$ or -1, determined by the output of the zero-threshold comparator, an appropriate signal residue is propagated to the next cycle. Primary nonideal effects in this structure include (1) capacitor mismatch, (2) opamp finite gain and offset, (3) parasitic capacitances, (4) clock feedthrough and charge injection, and (5) comparator offset. Well-known techniques can be used to overcome (3) and (4). Problems associated with (5) can be easily cancelled by using auto-zeroing, CDS, or digital redundancy (often referred to as digital correction) [5]-[6]. In the following circuit description of the new algorithmic converter, the focus will be on the correction of problems associated with (1) and (2).

3. ACCURATE RESIDUE AMPLIFICATION

We first describe the topology of the error-free residue amplification in a single-ended configuration. The steps involved in the correction of capacitor mismatch error are illustrated in Fig. 2. We start from the end of the *previous* bit conversion, when the residue was stored on capacitor C_1 and also on C_3 as voltage $V(i)$.

In the *first* phase, the signal charge from C_1 is transferred to capacitor C_2. At the same time, the bottom plate of C_1 is connected to voltage $-V(i)$. Even though the schematic shows a unity-gain inverting buffer, in the actual fully differential circuit this operation is simply a cross coupling of the differential signal paths. Note that in this very first step, exactly twice the charge that was stored on C_1 is now transferred to capacitor C_2.

In the *second* phase, the capacitor C_1 is discharged in preparation for the next phase.

In the *third* and the last phase, the charge from C_2 is transferred back to its "original owner" C_1. The charge on C_1 is now twice what it was before these three cycles took place, and the voltage $V(i+1)$ is also twice $V(i)$. A parallel injection of $\pm V_{ref}$ during either first or second phase would establish a perfectly linear residue amplification resulting in an error-free $2V_{in} \pm V_{ref}$ operation.

The fully differential structure for the same set of operations is shown in Fig. 3. In the *first* phase, it shows that the cross-coupling of the differential signal output paths implement the unity-gain inverting buffer. This configuration also includes the injection of the reference $\pm V_{ref}$. It is important to note that the charge-injecting capacitors C_{41} and C_{42} are different from signal-carrying capacitors C_{11} and C_{12} due to capacitor mismatch. This will result in an overall gain error for the A/D converter, but does not affect the converter linearity. However, if the original input signal to the A/D is sampled by the same set of capacitors C_{41} and C_{42}, even this gain error would be eliminated.

Finally, as illustrated in Fig. 4, opamp gain and offset compensation is also applied. The compensation scheme uses predictive correlated double sampling [7]. Capacitors that are active for the *predictive* function are denoted by the suffix *_pre*, and those that are used to hold the input-referred opamp offset and finite gain effect are denoted by the suffix *err*. In step 4 of Fig. 4, both C_{m_pre} and C_{h_sig} are charged into $V(k+1)$. In step 1, the main-amp performs the $2V(k+1) \pm V_{ref}$, and simultaneously, the errors are charged into the C_{merr}. In step 2, the main-amp performs the virtually error-free multiply-by-two operation by subtracting those errors. Similarly, the prediction of the hold-amp is obtained at step 3. For the whole CDS process, only one more clock phase is added to achieve opamp gain and offset compensation—for a total of *four* clock periods per bit.

4. SIMULATION RESULTS

All of the features discussed above are incorporated into the ADC schematic shown in Fig. 5. Only one side of capacitors and switches networks is shown for simplicity. In the SWITCAP simulation, we have incorporated $60 - 70$ dB gain and $20 - 50$ mV offset opamps, and a capacitor mismatch of σ=1-3%, which results in 3-9% mismatch between the maximum and minimum capacitor values. In addition, approximately 20% bottom-plate and 5% top-plate parasitic capacitors (also randomly 3% mismatched) were included. For high-speed comparison, we designed a latched comparator containing a 40 dB gain 50 mV pre-amp with auto-zero compensation capacitors (also 3% mismatched) and a 30 dB gain and 100 mV track-and-latch stage. A 16-bit ADC structure was used in the simulation.

Under these assumptions, the SWITCAP simulations results are shown in Fig. 6, before and after the new compensation scheme was applied. The simulation results indicate that the SNDR can be improved from 57 dB (before compensation) to 90 dB, and the 3rd harmonic is about -110 dB.

5. CONCLUSIONS

An efficient algorithmic A/D converter was described. The new switching scheme is able to achieve capacitor mismatch error compensation as well as finite gain and offset compensation of opamps. In comparison to most recent technique that uses a minimum of 7 clock periods per bit conversion, all tasks in the new technique is accomplished in 4 clock periods per bit. By avoiding multiple sampling over multiple clock periods for accurate signal amplification, a differential charge-mode sampling scheme has allowed the accurate and efficient two-times amplification of signal charge without the use of additional clock periods. The proposed ADC is being designed and fabricated to achieve 1.8 V, 100 ksample/s and 16 bit resolution with 0.18 μm double-poly CMOS process. The expected active area is about 600 μm x 700 μm, and the expected power consumption is about 4 mW.

6. REFERENCES

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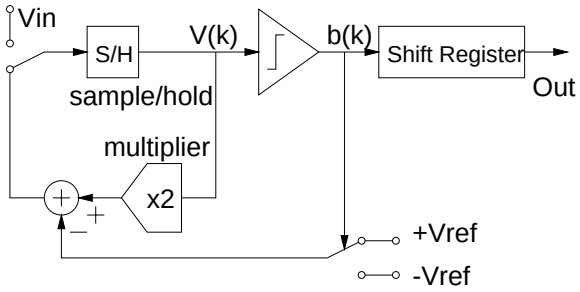


Figure 1: Algorithmic ADC structure

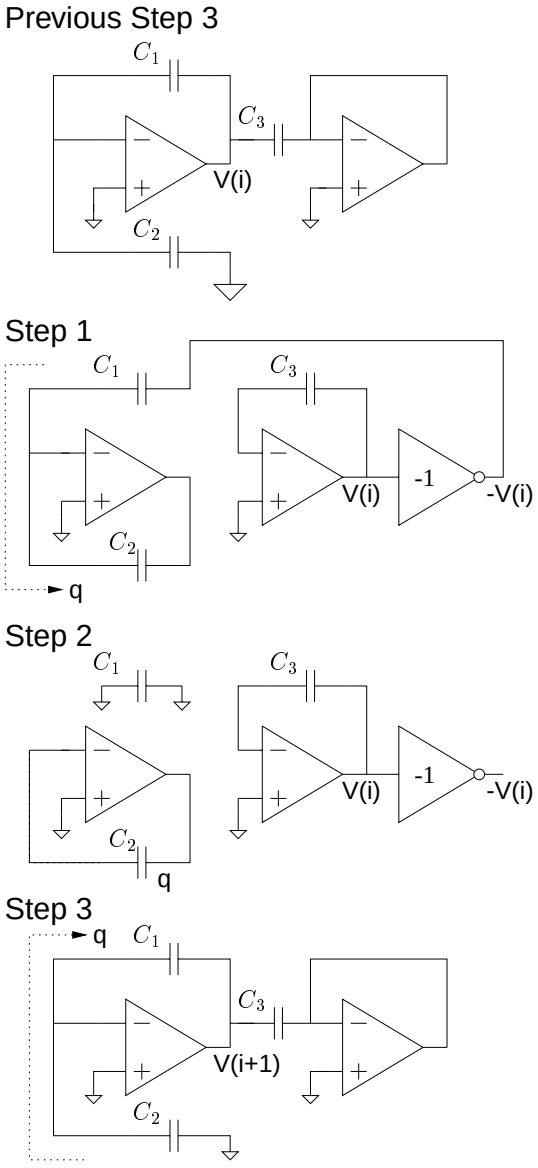


Figure 2: New capacitor ratio independent switching scheme

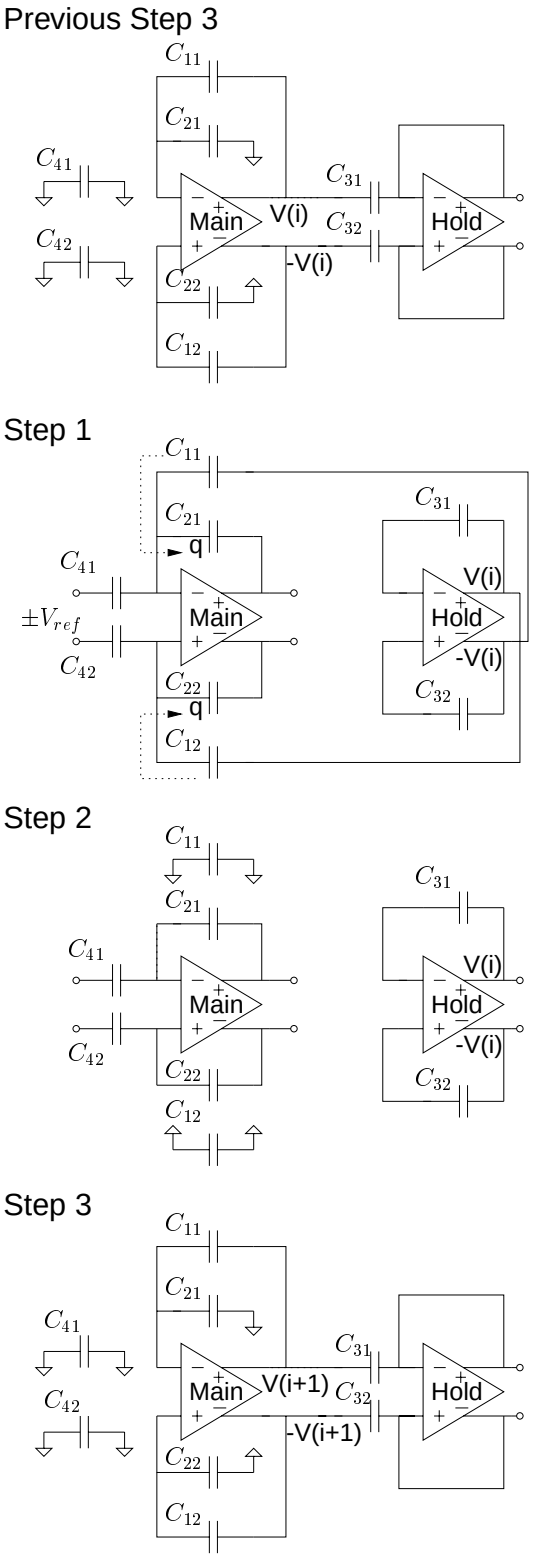
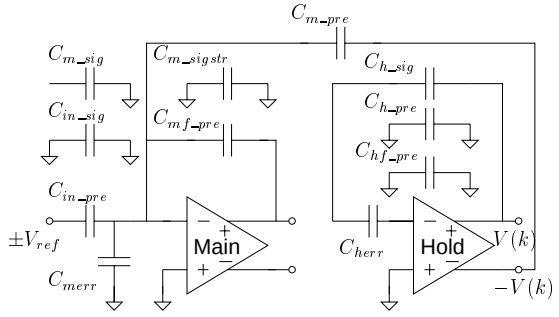
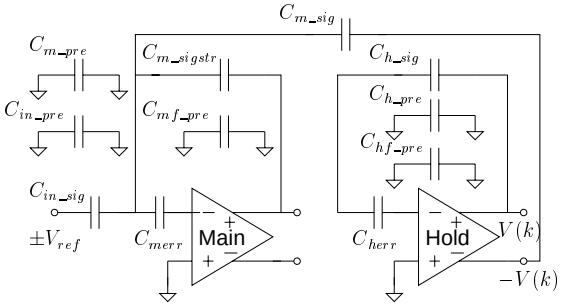


Figure 3: Accurate residue amplifier ($2V(i) \pm V_{ref}$)

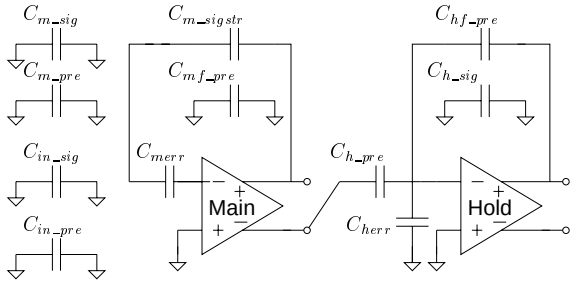
Step 1: Predict 2v(k)+/-Vref



Step 2: Store 2v(k)+/-Vref



Step 3: Hold 2v(k)+/-Vref



Step 4: Get v(k+1) = 2v(k)+/-Vref

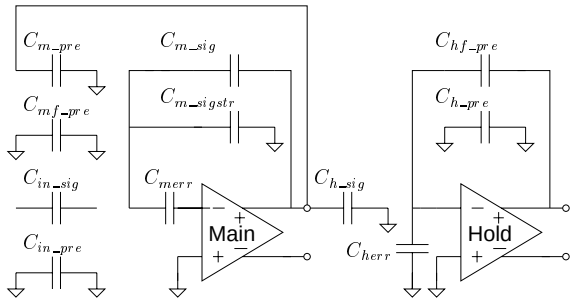


Figure 4: Accurate residue amplifier with GOC

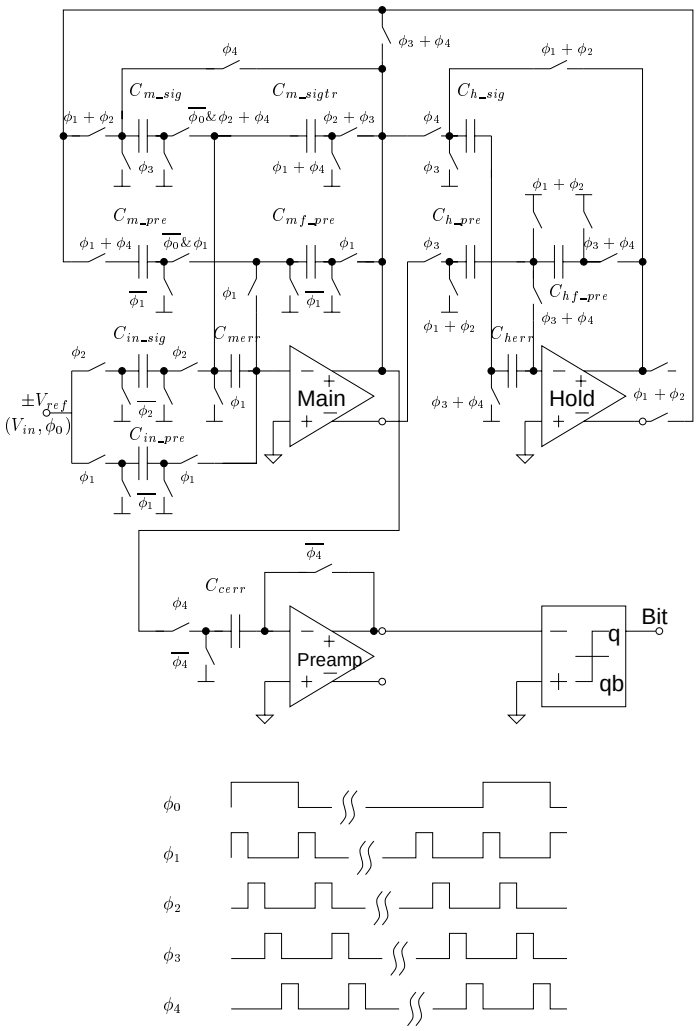


Figure 5: Complete new algorithmic ADC

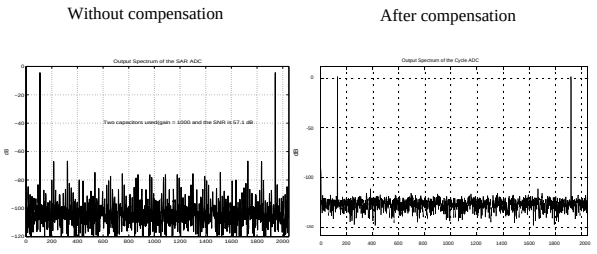


Figure 6: SWITCAP simulation results (before and after)