AN ADAPTIVE OFFSET CANCELLATION MIXER FOR DIRECT CONVERSION RECEIVERS IN 2.4GHZ CMOS

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ABSTRACT

In this paper we present a new circuit design for a 2.4GHz CMOS direct conversion mixer incorporating adaptive offset cancellation. The basic circuit structure is that of a Gilbert cell mixer. Offsets are cancelled by dynamically varying the bias on the loads, which are designed to provide constant impedance independent of the load cancellation current. The bias control is regulated via an adaptive dual-loop (gear-shifting) algorithm. Performance is good when canceling offsets of any realistic magnitude. The mixer has a gain of 6.4dB, IIP3 of 17dBm and noise figure of 17dB.

1. INTRODUCTION

In the continuing effort to minimize wireless transceiver size and power consumption great hopes exist for the eventual shift of receiver architectures from heterodyne to direct conversion. The primary advantage of direct conversion over heterodyne is the improved amenability to monolithic integration of the entire receiver system. There are two fundamental problems with full integration of heterodyne receivers. First, heterodyne receivers require a discrete component RF image-reject filter. Second, it is difficult to realize IF channel select filters with the low-Q available on chip [1,2]. Both problems are circumvented by the direct conversion implementation, as shown in Fig. 1. Direct conversion is highly touted to be the low power receiver solution [1,3,7]. Channel select filtering is performed in the base-band with high-Q switched-capacitor low-pass filters. The entire CMOS direct conversion transceiver can be implemented alongside the base-band DSP in a single inexpensive microchip. However, direct conversion introduces its own set of problems.

The major impediment in using direct conversion is the DC offset problem [3]. Insufficient on-chip isolation allows strong LO signals to couple through the substrate to the antenna, low noise amplifier, and the RF port of the mixer. The coupled LO signals are amplified as they follow the signal path to the mixer where they 'self mix,' causing energy to be superimposed onto the down-converted signal in the form of a DC offset. Coupling of the LO to the LNA and RF port of the mixer cause static or fixed offsets. However, when the LO couples to the antenna, radiates and then reflects off moving objects back to the antenna a time varying or dynamic offset is created [1] as can be seen in figure 2. The DC offsets created at the output port of the mixer, are often 20 to 30 dB larger than the desired signal levels. If not removed these offsets will saturate downstream gain stages desensitizing the receiver and destroying performance.

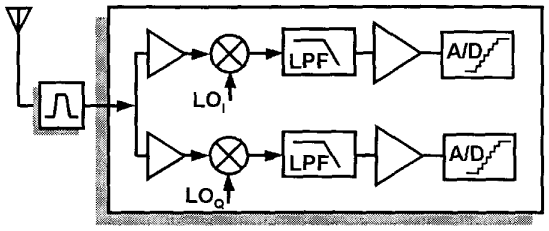

Fig. 1 Direct conversion receiver architecture.

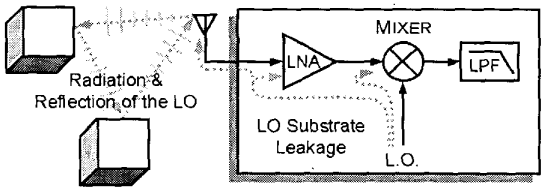

Fig. 2 Dynamic and static sources of DC offset.

In the balance of this paper we present a new circuit design to allow for the cancellation of these offsets. In section II we discuss typical offset levels found in a Gilbert cell mixer. In section III we discuss the detection of offsets. In section IV, we present our new design and discuss the tradeoffs of mixer offset cancellation. Finally, in Section V, we present HSPICE simulation to demonstrate the effectiveness of our new approach.

2. OFFSET IN THE GILBERT CELL

Our design is based on a Gilbert cell mixer for several reasons. The conversion gain requirement necessitates the use of an active mixer. Double balanced structures provide high port to port isolation and reject common mode digital clock noise. Excellent rejection of LO AM noise and rejection of spurious LO signals keep adjacent channel interferes from leaking to the LO port and self mixing. Finally, CMOS Gilbert cell mixers have wider dynamic range than other active doubly balanced mixers [4].

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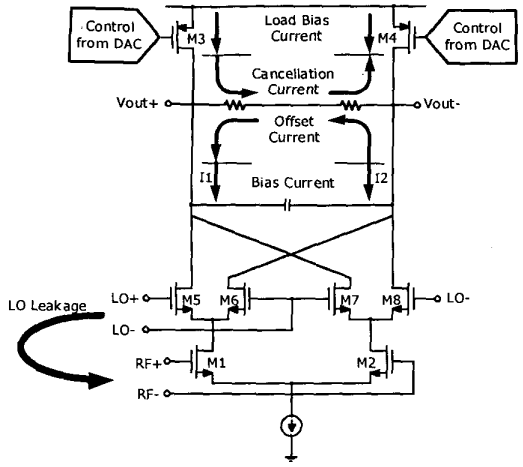

Fig. 3 Differential current offsets in the Gilbert cell are be cancelled by M3 and M4.

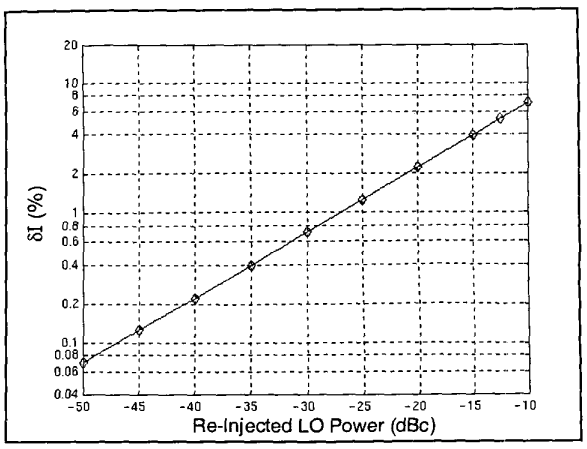

Fig. 4 Percent ratio of offset current to bias current caused by Re-Injected LO Power.

However, all mixers are subject to the generation of offset signals in their loads. In Fig. 3, we show how the operation of a Gilbert cell is affected. For the reasons stated earlier, a fraction of the LO gets coupled to the RF input (added to the desired signal) and the transconductors M1-M2 convert it into a current signal. The combined RF current signal (leaked LO plus desired) is down-converted to baseband by the switches M5-M8. The LO portion self-mixes causing an *offset current* to appear in the legs above the switches. This undesired offset current is then converted to an undesired offset voltage in the loads. However, if we can control the biases of M3-M4 to produce cancellation currents equal to the offset current, no voltage offset will appear at the differential output. To demonstrate the magnitude of the offset currents that we will have to cancel we define a new quantity,

$$\delta I = \frac{\text{offset current}}{\text{bias current } I} \times 100\%$$

which is the ratio of the offset current to the handling current through one leg. In Fig. 4, we present HSPICE simulation results of δI for typical levels of LO coupling. The x-axis maximum of -10dBc (worst case we are considering) could occur when there is 30dB of isolation between the LO and input of an LNA which has a gain of 20dB. We have designed our mixer to operate with good performance up to the expected maximum δI of 17%.

3. DETECTION OF OFFSETS

Previous attempts to track offsets in direct conversion receivers used large off-chip capacitors to perform low pass filtering and feed back a cancellation signal to a baseband amplifier. This method is reported to have worked well for removing static offsets, but was reported to have difficulty handling dynamic offsets [5].

In our work, we detect dynamic offsets, while maintaining good steady state performance, by employing an adaptive digital "gear shifting" approach. While we do not have time to go into detail in this paper, the basic idea is to utilize two IIR filters (one slow, one fast) implemented as dedicated digital logic circuits. When the offset is stationary, the slow filter (and of course the fast filter to a noisier degree) detect and track the offset. However, when there is a jump change in value of the offset, the slow loop is no longer a good estimator for the offset. This situation is detected when the outputs of the fast and slow filters differ by more than a pre-designated threshold. When this occurs, two things happen. First, the fast mode IIR filter's output is used. Second, its data history replaces the data history in the slow mode IIR filter, fooling it into "thinking" it has been tracking the new offset all along. This method has been simulated and been shown to perform well at tracking dynamic offsets[8].

4. CIRCUIT DESIGN

Our complete mixer design, including Gilbert cell, differential offset cancellation circuitry and common-mode feedback (CMFB), is shown in Fig. 5. The differential cancellation circuitry is controlled by a 6-bit DAC to cancel differential offset voltages. The CMFB fixes the output voltage and reduces even order distortions caused by the offset cancellation. Together, good mixer performance is achieved.

Since the mixer is the primary source of distortion in the front-end, careful gain budgeting must be applied to determine target noise figure, gain, and IIP3. For direct conversion, gain is required between the mixer and channel select filter to overcome the large noise figure of the latter. Performance goals have been set for a theoretical 3-volt receiver with an LNA gain 20dB, noise figure of 3dB and a channel select filter with noise figure of 40dB. The target mixer gain is 6dB, noise figure less than 20dB and the largest IIP3 possible. However, we must also be aware that the offset cancellation creates some imbalance, which makes IIP2 a critical design parameter. To improve mixer IIP2

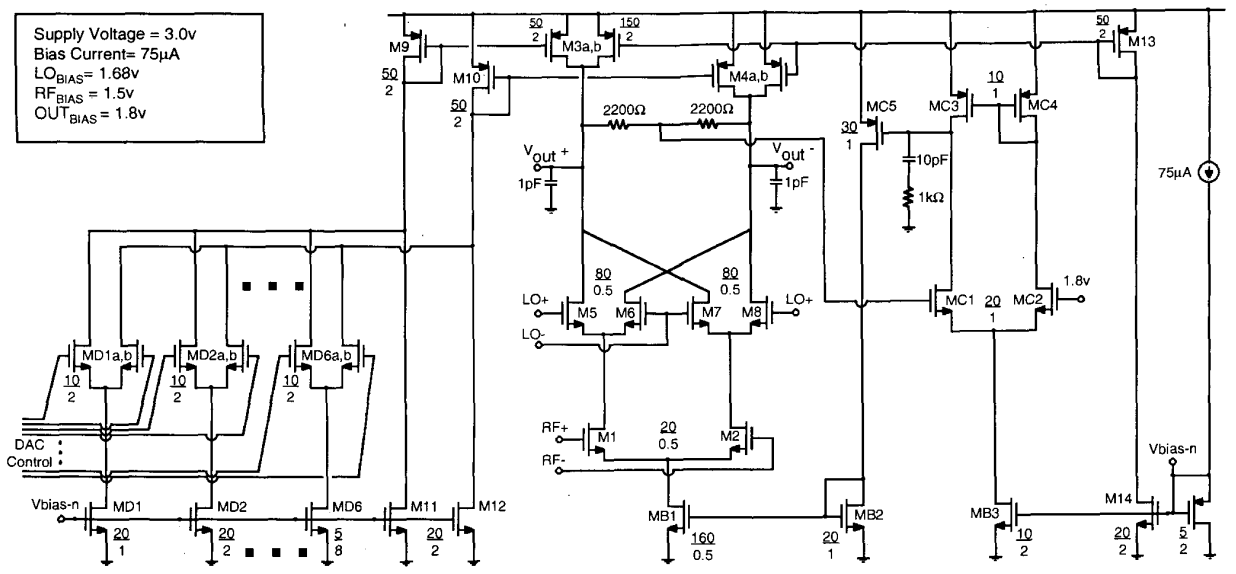

Fig. 5- Circuit diagram of adaptive cancellation mixer.

and IIP3, mixer gain is distributed less to the transconductors and more to the load.

The transconductors M1-M2 set the IIP3 for the mixer. They are biased high with v_{eff} = .72volts to allow for large input signals. To reduce gain contribution from the large v_{eff} a narrow channel width of 20μm is used. This increases mixer bandwidth and reduces the load for the LNA, at the cost of noise figure.

Sizing of switches M5-M8 is critical since they must be fast enough to fully commutate the LO but must be large enough to not contribute excessive flicker noise [6]. We bias these at 1.68volts and employ a 0dBm square LO wave to reduce the transition time when all four switches conduct. Frequency simulations show 80μm to be the largest width to meet the 2.4GHz switching speed.

The load consists of two poly-silicon resistors connected differentially and the PMOS transistors M3-M4. Since M3-M4 are only required to handle base-band signals we can safely use long channel (2μm) transistors which are operated in saturation to have large channel resistance $r_{ds3,4}$. Their large capacitance is actually beneficial in filtering unwanted RF signals and the double frequency terms created during mixing. The poly-silicon load resistors are small compared to $r_{ds3,4}$ and act as the primary source of impedance seen by differential current signals. Two advantages of this are: First, they can be scaled to adjust gain since they have little affect on limiting the mixer performance. Second, because the large impedance of M3-M4 creates a voltage divider with the poly-silicon loads, the perceived impedance mismatch in the 2200Ω poly-silicon resistors is only 27Ω at the maximum current imbalance of 88μA. Thus, the mixer gain, IIP3, and output signal swing remain quite constant, regardless of the cancellation current.

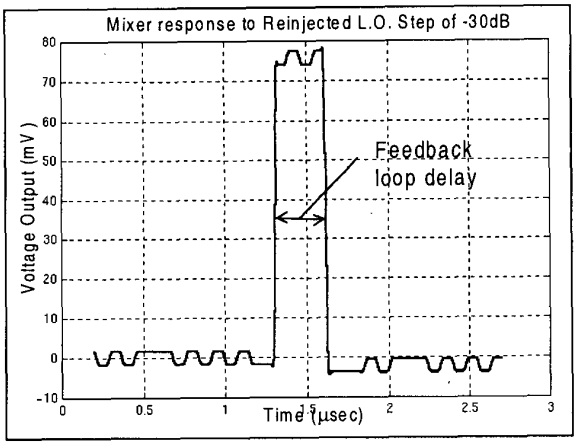

Fig. 6 HSPICE of mixer when LO is re-injected

The simplest means of reducing δI is to increase operating current. Unfortunately, an increased current density in M1-M2, raises the noise coefficient γ degrading the noise figure [6]. A tail current of 2.5mA is used to balance these tradeoffs.

To minimize noise contribution from both the differential and common mode circuits a large common mode loop gain of 60dB is used. To compensate this large gain a 10pF capacitor in series with a 1kΩ resistor is used to yield a 70° common mode phase margin.

To reduce power consumption and noise contribution from the DAC, M3-M4 are split. This split reduces the noise contribution from the differential cancellation circuitry by a factor of four.

The cost is a slight reduction the mixer's IIP3 when the DAC is fully deflected however, simulations show this amount to be negligible.

The initial prototype is expected to be digitally controlled off-chip where DSP algorithms can be easily manipulated to perfect the gear shifting algorithm. The DAC inputs are controlled by an on-chip binary decoder to reduce the number of lines coming off-chip. Besides the digital pin connections, the Output, RF, and LO ports are differentially brought off-chip to external baluns. A test board operating the mixer at 2.4GHz in the presence of on-chip digital switching will demonstrate the effectiveness of this solution.

5. SIMULATION RESULTS

The circuit in figure 5 has been simulated in HSPICE using both level 49 models 'tuned' for RF and level 49 models available from MOSIS for a .5μm HP process. Gain, bandwidth and distortion performances were also checked in SpectreRF and found to be comparable. Two sinusoidal tones spaced 1MHz apart near 2.4GHz were used in transient simulations to measure the gain, IIP2 and IIP3 values presented in this section.

Figure 7, shows offset cancellation performance against various levels of Re-Injected LO power. Gain and IIP3 are satisfactorily independent of LO coupling. IIP2 varies directly with LO coupling. An upper limit of 50dBm is expected when matching limitations are taken into account. Table I details mixer performance for the same mixer with and without the offset cancellation circuitry. For this mixer the cost of offset cancellation is an additional 0.9dB of noise figure and 1.8mW of power over the mixer without offset cancellation circuitry

Table I Mxer Characteristics

	Mixer w/o cancellation	Mixer w/ cancellation
Gain	6.4dB	6.4dB
IIP3	17dB	17dB
noise figure	16.1dB	17.0dB
linear output range	$2.4V_{pk\text{-}pk}$	$2.4V_{pk\text{-}pk}$
LO Power	0dBm	0dBm
CMRR	34dB	34dB
Current Consumption	3.4mA	4.0mA
Power Consumption	10.2mW	12.0mW

To demonstrate cancellation performance a bit stream was down converted by the mixer in an HSPICE simulation. A step offset of -30dBc is added and after a contrived delay the DAC is driven to cancel the offset. The results shown in Fig. 6 clearly illustrate mixer functionality.

6. CONCLUSIONS

In this paper an offset cancellation mixer has been presented. Relevant mixer design issues have been discussed in the light of heightened distortion performance requirements caused by mixer operation under imbalance. Simulation results show good mixer performance during the cancellation of a full range of offsets. We hope that this work helps to facilitate low power receiver designs as transceiver integration becomes prevalent.

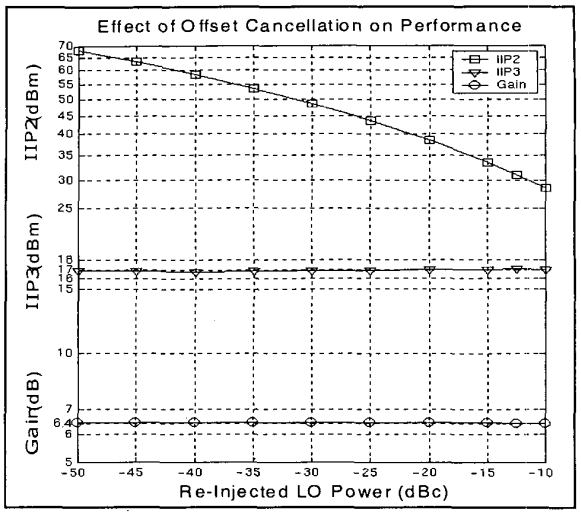

Fig 7- Mixer Performance during Offset Cancellation

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