AREA EFFICIENT CMOS CHARGE PUMP CIRCUITS

Ryan Perigny *

Conexant Systems, Inc.
3536 JFK Parkway
Fort Collins, CO 80525, USA

Un-Ku Moon and Gabor Temes

Department of Electrical and Computer Engineering
Oregon State University
Corvallis, OR 97331, USA

ABSTRACT

This paper describes the operation of three types of charge pump circuits. Power efficiency theory of charge pumps is discussed. A method of estimating the output ripple of a charge pump from the size of the capacitors used is described. A new charge pump circuit that uses two cascoded buffer transistors to improve the area efficiency is proposed.

1. INTRODUCTION

The charge pump [1] is a dc-dc converting circuit used to obtain a dc voltage higher or lower than the supply voltage, and/or opposite in polarity to the supply voltage. Charge pumps are widely used in low-voltage circuits [2], dynamic random access memory circuits [2], switched-capacitor circuits [3] and EEPROM's [4].

Three important issues of on-chip charge pump circuits are output voltage ripple, power efficiency and area efficiency. For most applications, a low output ripple is desired. Large output ripple degrades the performance of the circuit that the charge pump is powering. Charge pumps with very low power efficiency cancel the benefit of scaling the supply voltage down and are not desirable for portable applications. Area efficiency is desirable for many applications as smaller chip areas are less expensive to fabricate.

For low-noise applications, a very low output ripple is desirable to achieve good performance. This paper introduces a new charge pump circuit that provides very low output ripple with a smaller amount of capacitance than existing charge pumps, at the cost of a reduced output voltage and reduced power efficiency.

In this paper, the operation of three types of charge pumps will be described. Comparisons between the three charge pumps with regard to area efficiency, power efficiency and output voltage ripple will be discussed.

In Section 2, the conventional 2-capacitor charge pump will be described and analyzed. In Section 3, a charge pump that uses a buffer transistor to improve the area efficiency will be discussed. In Section 4, a newly proposed charge pump that uses two cascoded buffer transistors to further improve the area efficiency will be described.

2. CONVENTIONAL CHARGE PUMP

A conventional 2-capacitor charge pump that uses cross-coupled NMOS transistors [2] is shown in Figure 1. For simplicity, the body/bulk connections are not shown in the figure. The body/bulk connections of the n-channel switches are grounded. The p-channel switches are in an n-well, which is connected to the V_{well} node.

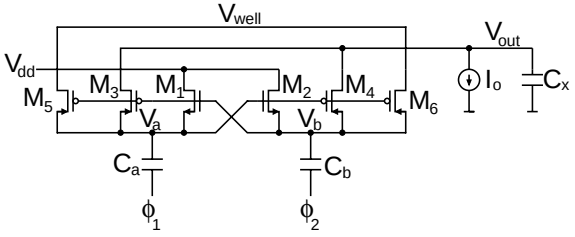

Figure 1: Conventional 2-capacitor charge pump.

This circuit uses two clock phases and operates as follows: during ϕ_2, switches M_1 and M_4 are turned on and capacitor C_a is charged to V_{dd}. During ϕ_1, switches M_2 and M_3 are turned on and capacitor C_b is charged to V_{dd}. Capacitor C_a, which was charged to V_{dd} during the previous clock phase, is now connected between V_{dd} and the load, lifting the voltage at the load to $2V_{dd}$. During every clock cycle, one capacitor is being charged to V_{dd} and the other capacitor is providing the load current.

Switches M_5 and M_6 are used to bias V_{well} to $2V_{dd}$, preventing latchup from occurring during startup. This method is discussed in [5].

2.1. Non-Filtering Case

If there is no load current, the output voltage will remain at $2V_{dd}$. If there is a significant load current and no added output capacitor ($C_x \cong 0$), the voltage at the output will ramp down with a slope of $\frac{I_o}{C_a}$ for half of a clock period before it is boosted to $2V_{dd}$ again.

The peak-to-peak voltage ripple at the output, ΔV_{out}, can be calculated as

$$\Delta V_{out} = \frac{I_o}{2 f_{clk}\, C_a}\ , \tag{1}$$

where f_{clk} is the clock frequency.

If there is an output capacitor, which is the usual case when a significant current must be provided, the slope of the output is reduced to $\frac{I_o}{C_a + C_x}$ due to the added capacitance at the output node. This reduces the ripple. The ripple is now

$$\Delta V_{out} = \frac{I_o}{2 f_{clk} (C_a + C_x)}\ . \tag{2}$$

A drawback of this circuit is that in order to achieve a very small output ripple, a large amount of capacitance is required. For

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example, in order to drive a load current of 50 μA with a clock frequency of 10 MHz and a desired output ripple of 5 mV, more than 500 pF of capacitance is required. For low-current pumps, most of the chip area of a charge pump is due to the capacitor area, so the area efficiency of a charge pump can be significantly improved by reducing the total capacitance needed to achieve a desired output ripple.

Power efficiency is an important consideration in charge pump design. An important cause of power loss in a charge pump is the charging and discharging of the bottom-plate parasitics of the pump capacitors (C_a and C_b in the previous example). These parasitics are charged to V_{dd} every clock cycle. For the conventional 2-capacitor charge pump shown in Figure 1, neglecting the resistance of the switches, and assuming that $\Delta V_{out} << V_{out}$, and $V_{out} \approx V_{low}$, the efficiency can be derived as

$$\eta = \frac{I_o\, V_{low}}{2I_o\, V_{dd} + 2f_{clk}\, p\, C_a\, V_{dd}^2}\ . \tag{3}$$

Here, p is the ratio of stray capacitance to desired capacitance ($C_p = p\ C_a$). This value is determined by the type of capacitors used and is usually between 5 and 20%. A good derivation of an equivalent expression for the power efficiency can be found in [5].

2.2. Filtering Case

One way to reduce the capacitance needed to achieve a given output voltage ripple is to use the on-resistance of transistor M_3 and capacitor C_x as a lowpass filter. This can be achieved by making transistors M_3 and M_4 narrow enough to provide enough resistance to bring the corner frequency of the RC branch below twice the clock frequency. Unfortunately, this also lowers the average output voltage due to the voltage drop across the switch, but for low current and high clock frequency applications the drop in output voltage may be small.

The corner frequency of the filter is equal to $\frac{1}{2\pi\ r_{on(M_3)}\ C_x}$. If this corner frequency is less than twice the clock frequency, then an approximation for the ripple at the output, ΔV_{out} can be found by assuming, for simplicity, that the ripple at nodes V_a and V_b in Figure 1 is a sinusoid of frequency $2f_{clk}$ and amplitude $\frac{I_o}{2f_{clk}\ C_a}$. If this were the case, the output ripple would be calculated as

$$\Delta V_{out} = \frac{I_o}{8\pi\ f_{clk}^2\ r_{on(M_3)}\ C_a\ C_x}\ . \tag{4}$$

Because the waveform is a ramp (not a sinusoid), the resulting ripple amplitude is smaller than the approximation given by (4).

3. SINGLE CASCODE CHARGE PUMP

A charge pump circuit that greatly reduces the total capacitance needed to achieve a given output voltage ripple is reported by Duisters and Dijkmans in [6]. A similar circuit is shown in Figure 2 as a simplified schematic. The capacitors shown with boxes around them symbolize conventional 2-capacitor charge pumps of the type described in the previous section. This circuit uses a buffer transistor and the on resistance of the switch connecting Charge Pump 2 to the drain of M_{buf} to provide additional filtering of the ripple.

Charge pump 1 provides the gate voltage for the buffer transistor M_{buf}. Because there is no dc current through the gate of M_{buf}, the charge pump capacitors need only be large enough to overcome the leakage from the parasitic gate capacitance of the switches and

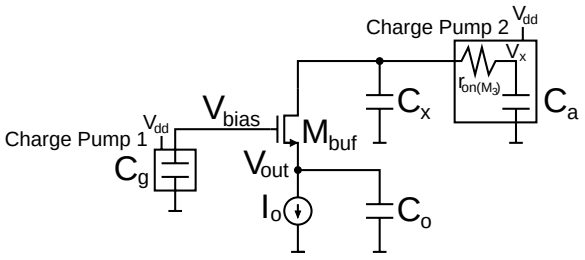

Figure 2: Single cascode charge pump.

provide around $2V_{dd}$ at the gate of M_{buf}. Charge pump 1 also provides the n-well bias voltage for all of the p-channel switches. Charge pump 2 provides the load current.

3.1. Non-Filtering Case

If C_x and C_o are small enough that both of the corner frequencies are greater than twice the clock frequency, then filtering is negligible, and the ripple at the drain of M_{buf} will be $\frac{I_o}{2f_{clk}\ (C_a+C_x)}$ as given by (2). The ripple at the output, ΔV_{out}, is reduced by the intrinsic gain of the buffer transistor ($g_m\ r_o$) and can be shown to be

$$\Delta V_{out} = \frac{I_o}{2f_{clk}\ g_{m(M_{buf})}\ r_{o(M_{buf})}(C_a + C_x)}\ . \tag{5}$$

It is important that the voltage at the drain of M_{buf} not drop more than V_T below the voltage at the gate in order to keep M_{buf} in saturation. This means that $\frac{I_o}{2f_{clk}\ C_a} + I_o\ r_{on(M_3)} < V_T$. Thus,

$$C_a > C_{a_{min}} = \frac{I_o}{2f_{clk}(V_T - I_o\, r_{on(M_3)})}\ . \tag{6}$$

If this condition is violated, M_{buf} becomes biased in the triode region and the output resistance of M_{buf} falls off sharply, causing the circuit to be much less effective.

3.2. Filtering Case

If enough capacitance is added at the drain of M_{buf} or at the output, the ripple is further reduced due to additional lowpass filtering.

Assuming the on-resistance of M_3 is large, the ripple at node V_x in Figure 2, ΔV_x, can be found using (1) to be

$$\Delta V_x = \frac{I_o}{2f_{clk}\ C_a}\ . \tag{7}$$

If the corner frequencies of the RC branches of this filter are all less than twice the clock frequency, additional filtering occurs, futher reducing the ripple amplitude.

The charge pump used to bias the gate of M_{buf} introduces more bottom-plate losses, which lowers the efficiency. The efficiency for a single cascode charge pump can be expressed as

$$\eta = \frac{I_o\, V_{out}}{2I_o\, V_{dd} + 2p\ f_{clk}(C_a + C_g)V_{dd}^2}\ , \tag{8}$$

where V_{out} is now equal to $2V_{dd} - V_T - V_{eff(M_{buf})}$, $V_T = V_{T0} + \gamma\left(\sqrt{2\phi_f + V_{out}} - \sqrt{2\phi_f}\right)$, and $V_{eff} = V_{GS} - V_T$.

3.3. Gate Biasing Circuit

Because M_{buf} acts as a source follower to the output of the single cascode charge pump, it is important that the gate bias voltage be as stable as possible in order to achieve very low ripple. Although charge pump 1 does not provide any current, there may be a significant ripple at the gate of M_{buf} caused by clocking glitches.

From a power standpoint, the best clocking scheme is to have the two clock signals ϕ_1 and ϕ_2 cross somewhere in the middle of the voltage range. This minimizes the wasted power due to leakage currents during the transition period, but also results in large glitches at the gate of M_{buf}. The ripple at this node occurs because when M_3 connects C_a to the gate of M_{buf}, the voltage at V_a has not yet reached $2V_{dd}$. The ripple at this node can be as much as a few millivolts, which can still increase the ripple at the output node if very low ripple is desired.

We propose a new circuit which provides a much smaller bias voltage ripple with clock signals that overlap in the middle of the voltage range is shown in Figure 3. The circuit is similar to the conventional charge pump circuit, with the addition of two switches and two capacitors. During ϕ_2, switches M_1, M_4 and M_7 are turned on and capacitor C_g is charged to V_{dd}. During ϕ_1, switches M_2, M_3 and M_8 are turned on and capacitor C_h is charged to V_{dd}. Capacitor C_g, which was charged to V_{dd} during the previous clock phase, is now connected between V_{dd} and V_{gx}, lifting the voltage at V_{gx} to $2V_{dd}$. During the next clock phase (ϕ_2), V_{gx} is connected to the gate of M_{buf}, providing a bias voltage of $2V_{dd}$.

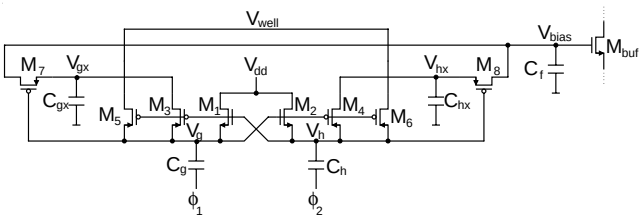

Figure 3: Modified conventional charge pump to provide the gate voltage for M_{buf}.

The ripple at nodes V_{gx} and V_{hx} is not easily determined, but depends on the rise and fall times of the clocks, the on-resistance of switches M_3 and M_4, and the size of C_{gx} and C_{hx}. If C_{gx} and C_{hx} are very small (less than 0.5 pF), the ripple at V_{gx} and V_{hx} is on the order of tens of millivolts. This is fairly large, but when these nodes are switched/relayed to the gate of M_{buf} through M_7 and M_8, the ripple at the output is very small (less than 0.1 mV). A small capacitor, C_f, also helps to reduce the bias voltage ripple.

4. DOUBLE CASCODE CHARGE PUMP

A proposed new charge pump circuit that further improves the area efficiency of a charge pump is shown in Figure 4. This circuit includes two cascoded buffer transistors, a third charge pump and an additional output capacitor. Charge pump 1 provides a bias voltage of $2V_{dd}$ to M_{buf1}. Charge pump 2 provides a lower gate voltage for transistor M_{buf2} in order to bias it in the saturation region. Charge pump 3 provides the load current.

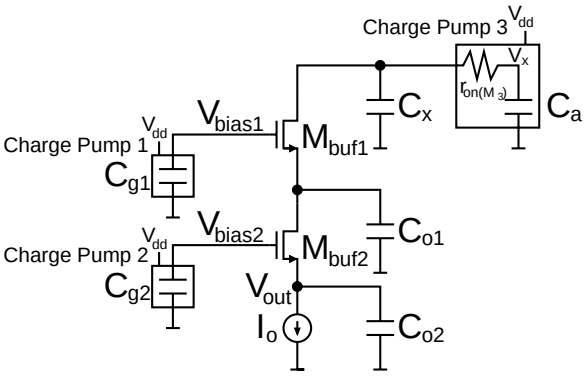

Figure 4: Double cascode charge pump.

4.1. Second Gate Biasing Circuit

The circuit used for biasing the gate of M_{buf2} is shown in Figure 5. This circuit is similar to the modified conventional 2-capacitor charge pump shown in Figure 3, with the addition of two capacitors, C_y and C_z from nodes V_{g2} and V_{h2} to ground. This circuit works as follows: when capacitor C_{g2} is charged to V_{dd}, C_y is also charged to V_{dd}. When the clock ϕ_1 rises to V_{dd}, some of the charge in C_{g2} is shared with C_y, causing the output voltage to be less than $2V_{dd}$. When ϕ_1 drops to zero, the additional charge stored in C_y goes back into C_{g2}. This is important because it allows a voltage lower than $2V_{dd}$ to be provided without any additional power loss due to the extra capacitors. The bias voltage V_{bias2} should be no higher than $2V_{dd} - V_{eff(M_{buf1})}$ in order to bias M_{buf2} in the saturation region.

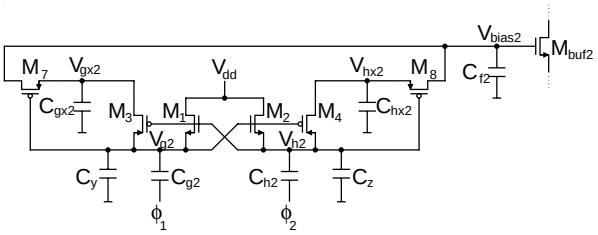

Figure 5: Conventional charge pump with added capacitors to obtain the second bias voltage.

The output voltage of this biasing charge pump is controlled by the size of C_y (and C_z) and is given by

$$V_{bias2} = V_{dd}\left(1 + \frac{C_{g2}}{C_{g2} + C_y}\right) . \quad (9)$$

4.2. Non-Filtering Case

The operation of this circuit is similar to the single cascode equivalent circuit, but the ripple is attenuated by the intrinsic gain of M_{buf2} and another filter branch.

In order for the third branch to filter effectively, the corner frequency, $\frac{g_{m(M_{buf2})}}{2\pi\ C_{o2}}$, must be less than twice the clock frequency.

If the on-resistance of the p-channel switches in charge pump 3 is small, the ripple at the drain of M_{buf1} will be $\frac{I_o}{2f_{clk}(C_a+C_x)}$

$$\Delta V_{out} = \frac{I_o}{2f_{clk}\ g_{m(M_{buf1})}\ r_{o(M_{buf1})}\ g_{m(M_{buf2})}\ r_{o(M_{buf2})}(C_a + C_x)}\ . \tag{10}$$

as given by (2). If a small amount of capacitance is used, so that no filtering occurs, the ripple at the output is reduced by the product of the intrinsic gains of M_{buf1} and M_{buf2}. The ripple at the output, ΔV_{out}, for a double cascode charge pump with no filtering is easily determined and is shown in (10) at the top of the page.

4.3. Filtering Case

If the on-resistance of the p-channel switches in charge pump 3 is relatively large (to provide filtering), the ripple at node V_x, ΔV_x, will be $\frac{I_o}{2f_{clk}\ C_a}$ as given by (1).

Treating the three filter branches as separate single-pole filters and assuming that the corner frequencies of all of the branches are well below $2f_{clk}$, an approximation for the ripple at the output for the filtering case can be found. The net result is a dramatically attenuated ripple amplitude.

The charge pump used to bias the gate of the second buffer transistor introduces additional bottom-plate losses, but because the capacitors used in this charge pump are small compared to C_a and C_b, this power loss may be tolerable. The power efficiency of the double cascode charge pump is given by

$$\eta = \frac{I_o\ V_{out}}{2I_o\ V_{dd} + 2p\ f_{clk}(C_a + C_{g1} + C_{g2})V_{dd}^2}\ , \tag{11}$$

where $V_{out} = 2V_{dd} - V_T - V_{eff(M_{buf1})} - V_{eff(M_{buf2})}$, $V_T = V_{T0} + \gamma\left(\sqrt{2\phi_f + V_{out}} - \sqrt{2\phi_f}\right)$, and $V_{eff} = V_{GS} - V_T$.

5. CONCLUSIONS

Figure 6 shows a plot of output ripple vs. efficiency for all three charge pumps where no filter is used. This plot was generated from multiple transistor level simulations. This shows that as buffer transistors are added to the circuit, the maximum efficiency decreases, but the ripple gets much smaller due to the intrinsic transistor gain for each stage that is added, regardless of the total capacitance or clock frequency that is used.

The relationship between output ripple and efficiency for the case where filtering is used is shown in Figure 7. For the filtering case, the difference in minimum ripple between the three charge pumps is much larger, and is dependent on how much total capacitance is used. If more capacitance were used, the curves would be farther apart, and if less capacitance were used, the curves would be closer together.

This new charge pump circuit is more area-efficient than the single cascode charge pump, at a price of reduced headroom (thus lower power efficiency). The size of ripple that can be tolerated seems to be the most important factor in determining which charge pump to use for a given application. For example, if power efficiency is the biggest concern and a larger output ripple can be tolerated, either a single cascode or a conventional charge pump would be a good choice. The double cascode circuit would be especially useful for applications where power efficiency is less critical and a very low output ripple is desired.

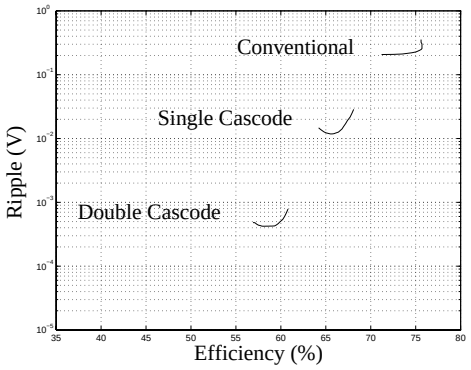

Figure 6: Efficiency vs. ripple for different charge pump circuits without filtering (I_o=100 μA, C_{total}=30 pF, p=5%, f_{clk}=10 MHz, V_{dd}=1.65 V, $|V_{T0}|$=0.55 V, $V_{T(M_{buf})} \approx$ 0.7 V, V_{eff}=0.2 V).

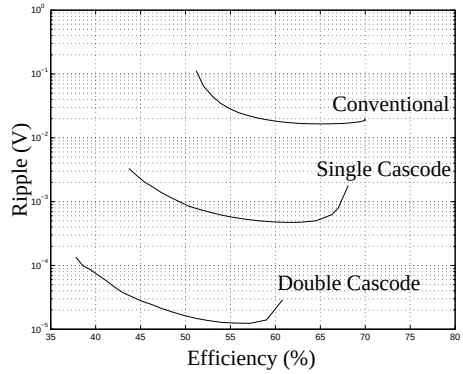

Figure 7: Efficiency vs. ripple for different charge pump circuits with filtering (I_o=100 μA, C_{total}=30 pF, p=5%, f_{clk}=10 MHz, V_{dd}=1.65 V, $|V_{T0}|$=0.55 V, $V_{T(M_{buf})} \approx$ 0.7 V, V_{eff}=0.2 V).

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