MULTIBIT ΔΣ ADC WITH MIXED-MODE DAC ERROR CORRECTION

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ABSTRACT

A mixed-mode error correction scheme is described for multibit ΔΣ ADCs with resistor-string and switched-capacitor DACs. The correction circuit uses a simple calibration ADC and digital filtering. It operates in the background and remains effective even for very low oversampling ratios.

1. INTRODUCTION

The use of multibit quantizers in delta-sigma (ΔΣ) analog-to-digital converters (ADCs) has great advantages over single-bit ones, such as increased signal-to-noise ratio (SNR), relaxed opamp specifications and improved stability [1]. However, the performance bottleneck is usually the linearity of the internal multibit digital-to-analog converter (DAC), which needs to be at least as good as that of the overall ADC. Off-line [1, 2] as well as on-line [3] digital calibration, and mismatch shaping [4–7] have been used to solve this problem for operation with a *large* oversampling ratio (OSR). An analog correction technique was also recently proposed [8].

In this paper, a mixed-mode on-line correction method is described. Unlike earlier techniques [1, 3–7], it remains effective even for very low oversampling ratios. It is also able to follow drift caused, e.g., by temperature variations during operation.

2. THE CORRECTION SYSTEM

A second-order ΔΣ ADC (DS_1) will be used to illustrate the proposed correction technique (Fig. 1). The digital output d_1 of DS_1 is given by

$$\begin{aligned} D_1(z) &= STF_1(z)\,U_1(z) + NTF_1(z)\,E_A(z) \\ &\quad + NLF(z)\,E_D(D_1(z)), \end{aligned} \tag{1}$$

where $STF_1(z)$ is the signal transfer function of DS_1, $NTF_1(z)$ is the quantization noise (e_A) transfer function of DS_1, and $NLF(z)$ is the DAC nonlinearity error (e_D) transfer function (i.e., from e_D to d_1). For the coefficient values used [1], $STF_1(z) = z^{-2}$, $NTF_1(z) = (1 - z^{-1})^2$ and $NLF(z) = -2z^{-1} + z^{-2}$.

As shown in Fig. 1, the internal DAC has two analog outputs: v_1 is input to the loop filter, and v_T is input to the calibration ADC (DS_2). The calibration ADC is used to derive a digital estimate $\hat{e}_D$ of the DAC errors e_D for all output levels, and stores these in a RAM. During conversion, internal DAC errors are corrected by filtering the RAM outputs via the FIR filter $NLF_d(z)$ and subtracting the result from the digital output d_1 of DS_1:

$$D_{corr}(z) = D_1(z) - NLF_d(z)\,\hat{E}_D(D_1(z)) \tag{2}$$

$$\begin{aligned} &= STF_1(z)\,U_1(z) + NTF_1(z)\,E_A(z) \\ &\quad + NLF(z)\,E_D(D_1(z)) - NLF_d(z)\,\hat{E}_D(D_1(z)). \end{aligned} \tag{3}$$

Assuming that the measurement of e_D was performed at the required accuracy, $\hat{e}_D \cong e_D$, the linearity of d_{corr} will be limited *only* by the mismatch between $NLF(z)$ and $NLF_d(z)$, which should not be critical. The details of the acquisition process for $\hat{e}_D$, and the analysis of the system, are given in the next Section.

The system shown in Fig. 1 assumes that a single DAC provides feedback signals to both integrators. Mismatch of coefficients b_1 and b_2 does not affect the system's linearity.

It should be noted that the nonlinearity errors of the internal ADC are not corrected by the system. However, these are suppressed by the same noise transfer function as the quantization noise (typically, $(1 - z^{-1})^2$ for a second-order ΔΣ ADC), and hence rarely present a problem. This may be insufficient when very low OSR is used, and high linearity is required. In this case, a second stage (as in the MASH configuration) may be added, or ADC element mismatch shaping [9] may be used.

3. THE CORRECTION PROCESS

The on-line acquisition of the actual DAC output level errors can be tailored to the DAC structure. If the DAC can provide multiple inputs and outputs, such as the *resistor-string* DAC described in [1] (Fig. 2(a)), then the off-line calibration proposed in [1] can be transformed into a background process. In that case, a digital calibration signal d_T

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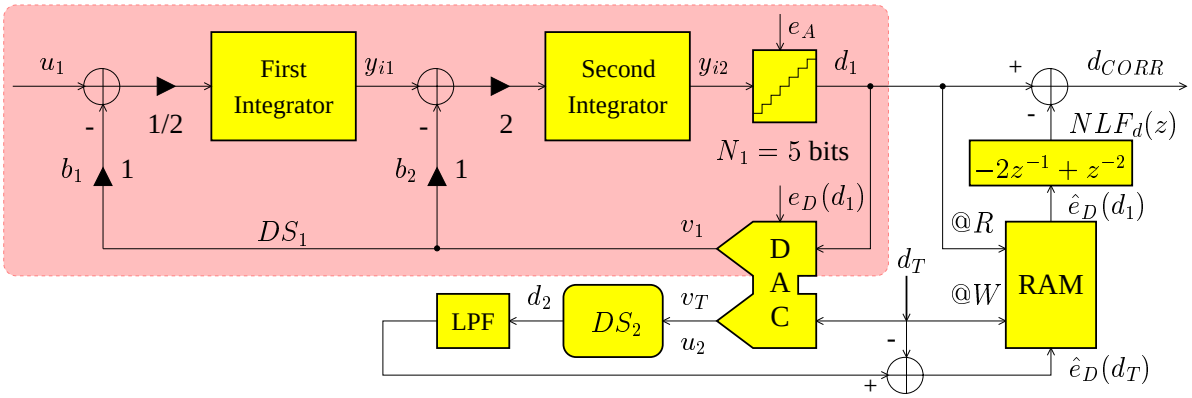

Figure 1: Multibit $\Delta\Sigma$ ADC with mixed-mode error correction.

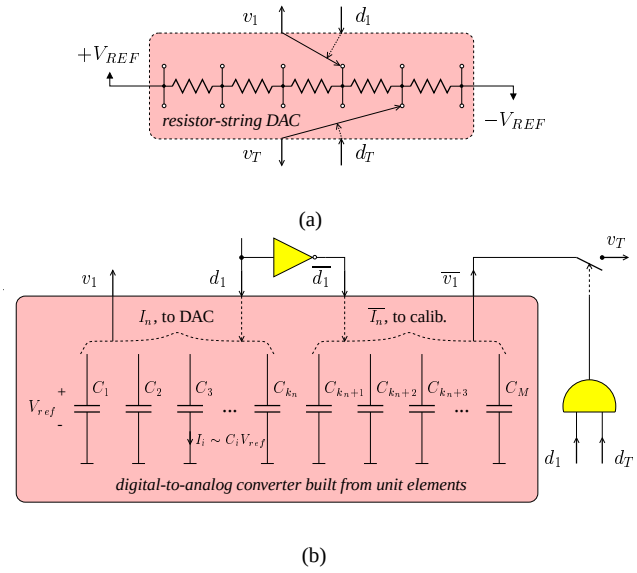

Figure 2: DAC structures which may be used in DS_1: (a) resistor-string DAC; (b) unit-element DAC.

will provide a staircase waveform sequentially generating every possible input to the DAC (Fig. 1). Each DAC output level v_T is converted to digital form d_2 by the calibration $\Delta\Sigma$ A/D converter DS_2, and lowpass filtered by LPF (Fig. 1) to remove the quantization noise of DS_2. Then, d_T is subtracted to recover the level errors e_D in a digital representation. Therefore, estimates $\hat{e}_D(d_T)$ are obtained for each possible input code d_T. They are stored (@W) in the RAM at the location given by d_T. The estimate $\hat{e}_D(d_1[m])$ is recalled (@R) for each output $d_1[m]$ to correct it. During operation, the calibration can be periodically repeated to track any drift in the DAC output levels, e.g., due to temperature effects.

For low oversampling ratios and for low-order loop filters, the transfer function $NLF_d(z)$ cannot be approximated accurately by $NLF_d(z) = -1$, as was done in [1] and [3]. The RAM output needs to be filtered by the actual $NLF_d(z)$ (here, $-2z^{-1} + z^{-2}$) in order to achieve accurate error cancellation, as shown in Fig. 1. If one uses $NTF_d(z) = -1$ [1, 3], than the corrected output $D_{corr}(z)$ will contain an error-leakage term $(NLF(z) + 1) \cdot E_D(z)$, derived from eq. (3). This significantly deteriorates the corrected performance at low oversampling ratios as demonstrated in Section 4 (for details refer to [10]).

In some DAC implementations, M equal-valued *unit elements* (current sources, capacitors, resistors, etc.) are used. The algorithm described above may still be used, if $M + 1$ elements are implemented in the DAC [3], and their errors are measured sequentially one-by-one using DS_2.

Alternatively, the output signal d_1 may be used also as the calibration signal d_T (Fig. 2(b)). For a d_1 value calling for the use of $k_n(d_1)$ unit elements to produce $v_1(d_1)$, the remaining $M - k_n(d_1)$ unit elements are utilized to generate $v_T(\overline{d}_1)$. Therefore, $v_T(\overline{d}_1)$ is the DAC output level which corresponds to the binary input code $\overline{d}_1$ = (full scale code $- d_1$). If (as usual) fixed DAC gain and offset errors are acceptable, so that the sum of all unit-element errors can be regarded as zero, then the error present in v_T is the negative of that in v_1 (Fig. 2(b)):

$$v_1 \quad \propto \quad I_n = \sum_{i=1}^{k_n} I_i = k_n\, I_{ave} + \delta_n, \tag{4}$$

$$v_T \quad \propto \quad \overline{I_n} = \sum_{i=k_n+1}^{M} I_i = (M - k_n)\, I_{ave} - \delta_n, \tag{5}$$

where I_{ave} is the average current of the M unit elements. Based on the value of d_1 one can sort the analog samples in v_T into K channels[1], with one channel dedicated to each possible input code d_1 *and* its complement $\overline{d}_1$. Hence, DS_2 can be used to produce the digital form $d_2(d_T)$ of the individual DAC output levels. From $d_2(d_T) - d_T$ one can estimate the nonlinearity errors e_D and store them into the

[1]For M even: $K = M/2$; for M odd: $K = (M - 1)/2$.

RAM. The operation of DS_2 can easily be multiplexed among the channels, with only the memoried elements (feedback capacitors) replicated for each channel [11, page 585].

For linear operation, the calibration ADC (DS_2) must itself be highly linear. This may require the use of a single-bit internal quantizer in DS_2. However, linear effects (gain and offset errors) are acceptable in DS_2 because the DAC nonlinearity information is preserved. Also, the matching errors between the actual DAC nonlinearity error transfer function $NLF(z)$ and its digital replica $NLF_d(z)$ (Fig. 1) can be shown to have only a minor effect on the linearity of the overall conversion (see next Section).

4. SIMULATION RESULTS

The operation of the digitally corrected ADC shown in Fig. 1 was simulated under the following realistic conditions. 5-bit (32-level) internal ADC and DAC were assumed. The transfer function and the nonlinearity error of the DAC are shown in Fig. 3. A 0.1% linear gradient error [12, Section 4.3.1] was assumed in the DAC; the offset and gain errors were removed since they do not affect the performance. Finite (54 dB) dc gain for all opamps and randomly mismatched capacitors (with 0.1% standard deviation) were assumed in all circuits. A very low oversampling ratio ($OSR = 4$)

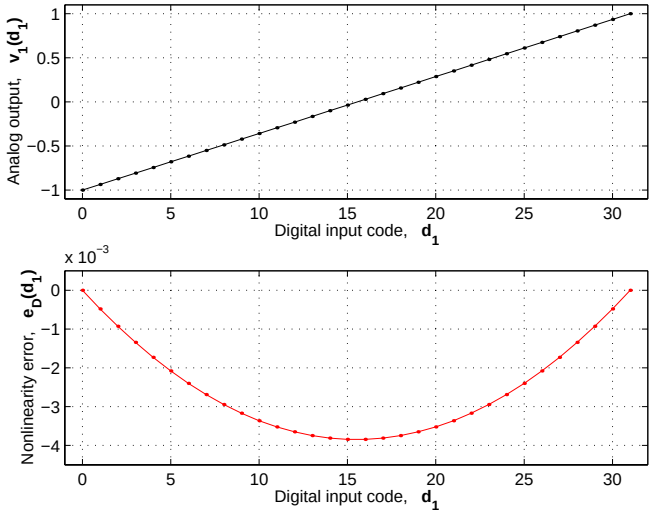

Figure 3: Static characteristics of the DAC used in DS_1.

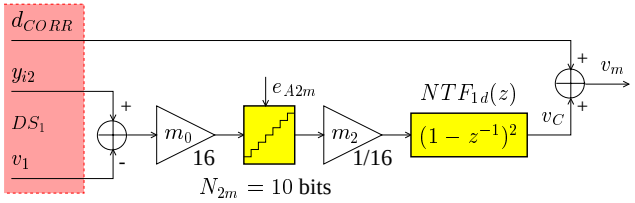

Figure 4: 2-0 MASH ADC with DS_1 as its first stage.

was used. A 0.45-V peak midband two-tone input signal u_1 was applied to DS_1, and a second-order single-bit $\Delta\Sigma$ ADC realized DS_2. In order to demonstrate the high linearity achievable with the proposed correction, DS_1 was embedded in a 2-0 MASH containing a 10-bit ADC as its second stage (Fig. 4). The mismatch between the MASH stages was not considered; it can also be corrected by digital methods [13].

The computed spectrum of the system operating with an ideal DAC but with nonideal opamps and capacitors (described above) is shown in Fig. 5(a). Fig. 5(b) shows the spectrum using the nonlinear DAC without error correction. Large harmonics are generated and the spur-free dynamic range ($SFDR$) is only 52 dB. Fig. 5(c) shows the result when using the digital correction described in this paper; a $SFDR > 100$ dB was achieved. In order to obtain sufficiently accurate estimates of e_D needed for such a high $SFDR$, DS_2 processed 2^{18} samples for each level of the DAC (a complete background calibration cycle then needs about 4 seconds if DS_2 is clocked with $f_S = 5$ MHz). Finally, Fig. 5(d) illustrates the detrimental effect of using $NLF_d(z) = -1$, as was done in earlier work [1, 3]: the $SFDR$ drops from 101 dB to 60 dB.

Note that the spurs in the corrected spectrum (Fig. 5(c)) compared to the ideal response (Fig. 5(a)) are due to the *finite* accuracy in the estimation process; it can be improved by increasing the number of samples (equivalently, increasing OSR) used in DS_2. However, the mismatch[2] between $NLF_d(z)$ and the actual $NLF_d(z)$ limits the achievable $SFDR$ to about 120 dB; this can be overcome by increasing OSR in DS_1. Finally, the correction method presented in this paper works equally well for other $\Delta\Sigma$ ADC topologies, and also for larger and different type (e.g., randomly distributed) DAC errors.

5. CONCLUSION

A mixed-mode on-line correction method was proposed for DAC nonlinearities in $\Delta\Sigma$ ADCs with multibit internal quantizers. It is applicable even for ADCs with very low oversampling ratios, where the commonly used mismatch-shaping techniques become less effective. Simulations indicate that excellent linearity can be obtained using the proposed process.

6. ACKNOWLEDGMENT

Useful discussions with Professor Gert Cauwenberghs of Johns Hopkins University, Baltimore, MD, are gratefully acknowledged. The valuable comments of the reviewers are also appreciated.

[2]The mismatch between $NLF_d(z)$ and $NLF(z)$ depends on the capacitor mismatch and the finite dc gain of the opamps used in DS_1.

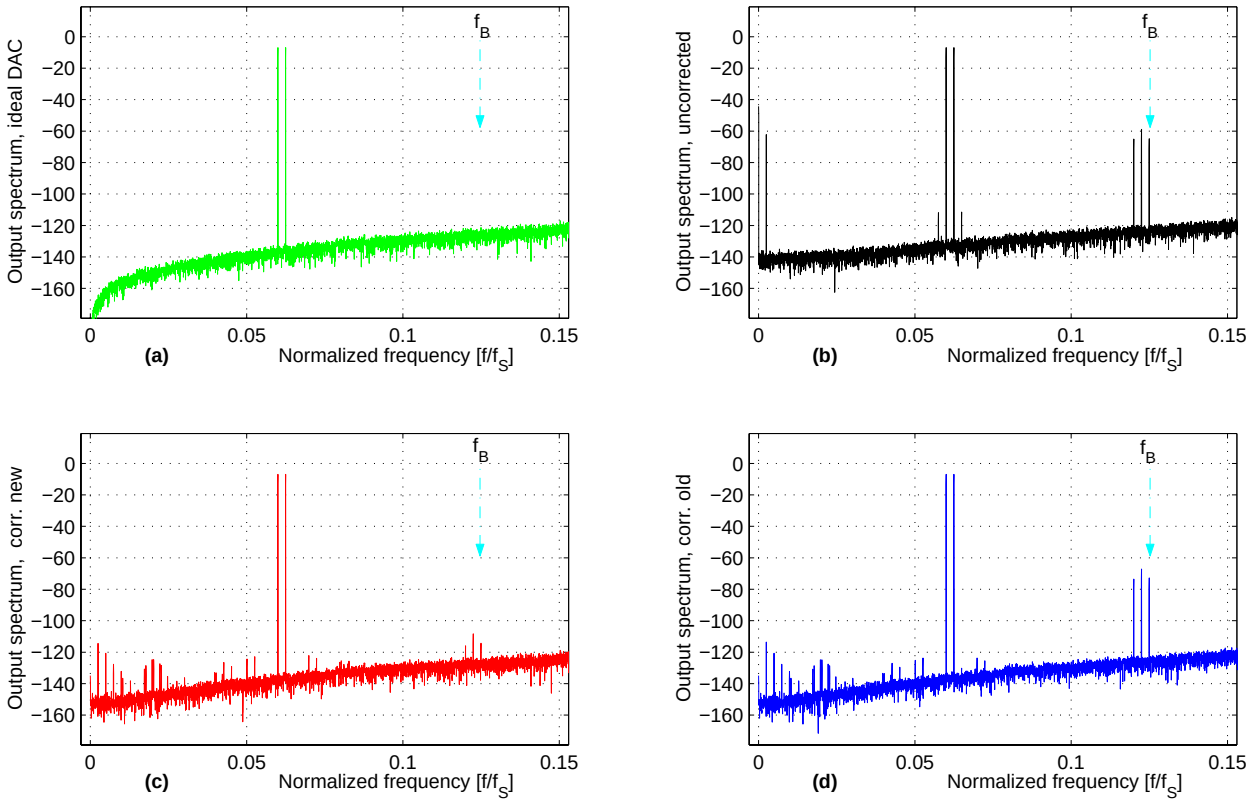

Figure 5: Output spectra of the MASH (computed using 64× averaged FFTs for 2^{15} samples, $f_B = \frac{f_S}{8}$: inband limit for $OSR = 4$): **(a)** for ideal DAC; **(b)** for nonlinear DAC without correction; **(c)** for nonlinear DAC with the proposed correction, and **(d)** with correction, but using $NLF_d(z) = -1$.

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