LOW-VOLTAGE LOW-SENSITIVITY SWITCHED-CAPACITOR BANDPASS $\Delta\Sigma$ MODULATOR

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1. ABSTRACT

A novel low-voltage (LV) switched-capacitor (SC) resonator circuit and its bandpass $\Delta\Sigma$ modulator implementation are presented. The proposed circuit not only uses lower supply voltage but also reduces the errors due to analog imperfections. Hence, these circuits may be suitable for submicron LV CMOS process in the next generation of AM and FM digital radio and GSM receivers.

2. INTRODUCTION

The recent explosion of interest in wireless personal communication systems motivates the development of fully integrated radio receivers. The parallel reduction of the dimension in CMOS technology, and hence higher levels of integration enables the combined integration of bandpass or baseband analog-to-digital converter along with the traditional front-end receiver building blocks. While this trend of technological achievements advances the digital technology, one of the key analog limitations of state-of-the-art submicron CMOS technologies remains the restricted power-supply voltage, limited by the low-junction breakdown voltage of high density CMOS process and by the thin gate oxide, prone to voltage stress.

There exist many resonator circuits to implement SC bandpass $\Delta\Sigma$ modulators and filters for high-frequency communication applications such as the "lossless-discrete integrator" (LDI) and "forward-Euler" (FE) types [1], two-delay loop (TDL) [2], [5], low-pass filter [3], high-pass filter based [4] and pseudo-two-path (P2P) type [6]. The most recent ones use P2P and TDL techniques, with double sampling to increase the sampling frequency. In these previous implementations, the minimum available power supply voltage was 3 V.

In our previous work, we have shown the LV implementations of SC ADCs and low-pass filters [7] based on the *unity-gain-reset* (UGR) technique. Compared to the switched-opamp technique [8], this technique is suitable for operating at higher speeds, by keeping the opamp in its active operating region at all times.

In this paper, we present a novel LV resonator circuit, which is functional down to 1 V. This resonator will be used as the main block of the LV SC bandpass $\Delta\Sigma$ modulator. Our aim is not only to design LV circuit but also to reduce the effects of analog circuit imperfections.

The following sections will discuss the analog imperfections in one of the common resonator types, based on an LDI integrator. After this, we focus on the proposed low-voltage resonator circuit and its bandpass $\Delta\Sigma$ implementation. The simulation results will be shown in the last section.

This work was supported by the NSF Center for Design of Analog-Digital Integrated Circuits (CDADIC).

3. ANALOG CIRCUIT IMPERFECTIONS IN RESONATORS

The typical resonator transfer function with unit delay from input to output is given by

$$H(z) = \frac{z^{-1}}{1+z^{-2}} \tag{1}$$

This leads to the time-domain relation

$$v_o(n) = v_{in}(n-1) - v_o(n-2) \tag{2}$$

which involves a delay by $2T$ and the inversion of $v_o(n)$. In the previous works [1-6], the main limitations or error sources in the implementation of (1) and (2) were the finite gain and bandwidth of the operational amplifier and the path mismatch. The first two were the main problems in all previous implementations, but path mismatch is the main limitation for designs which used two-path or double-sampling technique. We discuss finite gain and bandwidth effects in detail in the following subsections for the low-voltage implementation of the LDI resonator.

3.1. The Effect of the Finite Gain of the Operational Amplifier

Since the $H(z)$ of (1) can be obtained from two half-delay integrators, the effects of nonidealities on such integrator will be analyzed next. In the presence of finite operational amplifier gain (A_{dc}), the half-delay SC integrator will have the transfer function:

$$H_1(z) = m_1 \frac{z^{-1/2}}{1-p_1 z^{-1}} \tag{3}$$

where m_1 is the actual integrator gain and p_1 is the shifted pole. They are given by

$$m_1 = \frac{(\frac{C_s}{C_I})}{1+\frac{1}{A_{dc}}(1+(\frac{C_s}{C_I}))} \quad and \quad p_1 = \frac{1+\frac{1}{A_{dc}}}{1+\frac{1}{A_{dc}}(1+\frac{C_s}{C_I})} \tag{4}$$

where C_s and C_I are the sampling and integrating capacitors, respectively. A_{dc} is the DC gain of the opamp used.
The low-voltage LDI resonator which can be implemented with two cascaded half-delay integrator in a positive feedback loop is

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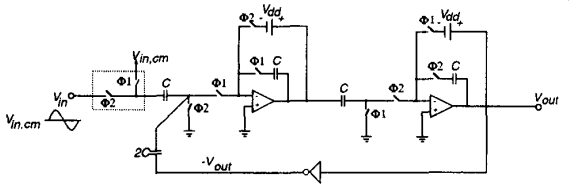

Figure 1: Single ended LDI type low-voltage resonator.

shown in Fig. 1. The circuit is shown in single-ended configuration for illustration purpose only; in fact, it is usually realized in a differential form.

The effect of the finite gain will be severe in this resonator circuit. This resonator (Fig. 1) will not only introduce gain error but also shift the center frequency as shown below:

$$H(z) = \frac{(m_1 m_2)z^{-1}}{1 + (2m_1 m_2 - p_1 - p_2)z^{-1} + (p_1 p_2)z^{-2}} \quad (5)$$

where m_1 and p_1 refer to the first integrator and m_2 and p_2 refer to the second integrator.

As shown by the denominator coefficient of z^{-1} (ideally zero),

$$\frac{\Delta f_o}{f_o} = \frac{2m_1 m_2 - p_1 - p_2}{\pi} \quad (6)$$

This shift may introduce large out-of-band noise into the signal band. At the same time, the coefficient of z^{-2} term is equal to $(p_1 p_2)$ instead of "1" as for the ideal case. Therefore, a gain drop will also be introduced.

3.2. The Effect of the Finite Bandwidth of the Operational Amplifier

The finite bandwidth of an operational amplifier introduces a gain error in an ordinary integrator:

$$H(z) = \frac{C_s}{C_I}(1 - g_1)\frac{z^{-1/2}}{1 - z^{-1}} \quad (7)$$

where the gain error term is $g_1 = e^{-T/\tau}$, and τ is the settling time constant.

Here, this gain error will be transferred to the denominator of the resonator transfer function because of the positive feedback from the output to the input:

$$H(z) = \frac{G(1 + g_1 g_2 - g_1 - g_2)z^{-1}}{1 - (2g_1 + 2g_2 - 2g_1 g_2)z^{-1} + z^{-2}} \quad (8)$$

and the shift in f_o is given by

$$\frac{\Delta f_o}{f_o} = -\frac{2g_1 + 2g_2 - 2g_1 g_2}{\pi} \quad (9)$$

The limited bandwidth not only shifts the center frequency and introduces out-of-band noise into the signal band, but also sets an upper limit on the sampling frequency, because g_1 increases with sampling frequency and severely affects the shift.

The LDI type resonator was simulated in SWITCAP2 for different DC gains and bandwidths. Simulation results show the serious effects (Fig. 2) for f_s=40 MHz.

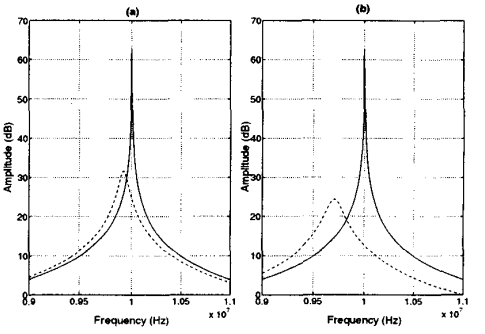

Figure 2: Simulation results of the LDI type resonator from SWITCAP2 with f_{clock}=40 MHz (a) for different opamp DC gains; A_{dc}=120 dB (solid), 50 dB (dashed) (b) for different opamp bandwidths; $f_u = \infty$ (solid), f_u=160 MHz (dashed).

4. THE INTEGRATING-TWO-PATH LOW VOLTAGE RESONATOR

The proposed integrating-two-path (I2P) LV resonator architecture is shown in Fig. 3. I2P uses a pseudo-differential configuration for LV operation. There are two paths from the input to the output in this scheme. The upper two opamps form the first path and one of the pseudo-differential pairs. The lower two opamps form the second path and the other pseudo-differential pair.

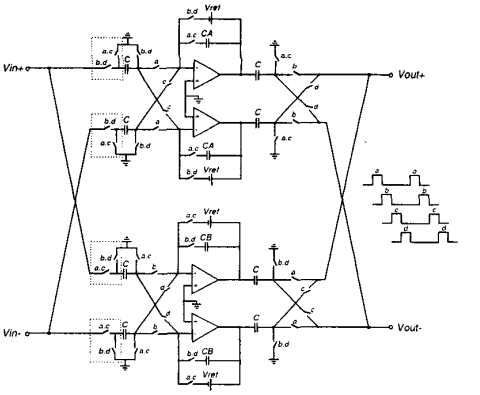

Figure 3: The integrating-two-path low-voltage resonator.

The technique used for providing the two clock cycle $(2T)$ delay in the previous circuits [1-6] was to apply positive feedback from the output to the input of a resonator. In all these circuits, there is charge transfer from the output to the input to realize the resonator transfer function. This charge transfer also integrates some error charges with a delay T. Hence, there is always a z^{-1} term in the denominator of the resonator transfer functions. This creates a shift in the center frequency, with different amounts from one architecture to the other. Additionally, there was severe gain loss in some of the previous implementations.

In this I2P structure, during odd clock phases, the differential output voltage, delayed by $2T$, is stored in capacitors CA. Then

the output of the differential pair is commutated to realize the resonator transfer function. The same operation is done by the other pair containing CB in the even clock phases. This operation prevents the introduction of odd order terms in the denominator and the mixing of gain and leakage errors. Hence, it leads to a transfer function yielding only non-critical m and p:

$$H(z) = \frac{mz^{-1/2}}{1 + pz^{-2}} \tag{10}$$

Because of the LV operation, the commutation operation is done at both the input and the output, instead of the feedback branch (an option for higher voltage circuit implementation), every two clock cycles. This will change the sign of the stored voltage on the path and hence introduce effectively positive feedback operation in the voltage domain.

The simulation results from SWITCAP2 are shown in Fig. 4. There is no change in the center frequency location when decreasing the DC gain or the bandwidth of the opamp. The gain loss (due to error term "p") is also decreased by the commutation operation.

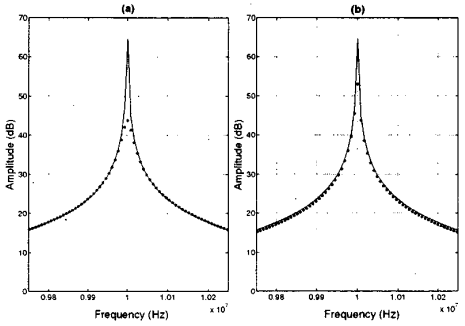

Figure 4: Simulation results of I2P type resonator from SWITCAP2 with f_{clock}=40 MHz (a) for different opamp DC gains; A_{dc}=120 dB (solid), 50 dB (dots) (b) for different opamp bandwidths; $f_u = \infty$ (solid), f_u=160 MHz (dots).

5. SIMULATION RESULTS

Simulation results for four different resonators are presented in Fig. 5. The resonators are the lossless-discrete-loop (LDI) [1], pseudo-two-path (P2P) [6], two-delay-loop (TDL) [2], and finally the proposed integrating-two-path resonator (I2P) circuit.

The peak resonances of all four resonators are obtained at 10 MHz for the ideal case where $f_u = \infty$, $A_{dc} = 120$ dB, and f_{clock}=40 MHz.

In Fig. 5 (b), the finite bandwidth and gain limitation of the opamp are simulated with $f_u = 160$ MHz and $A_o = 60$ dB. I2P has almost 16 dB gain loss, but no shift in the center frequency. P2P has 32 dB gain loss and 20 kHz center frequency shift. TDL has 37 dB gain loss and 55 kHz center frequency shift. As seen in the figure, the LDI circuit resonance is far off from the 250 kHz bandwidth around the center frequency.

From SWITCAP2 simulations, it can be seen that the SC resonator circuit is implementable with a good gain (Q) and frequency response which is insensitive to analog circuit imperfections. The LV I2P structure not only demonstrates performance enhancement

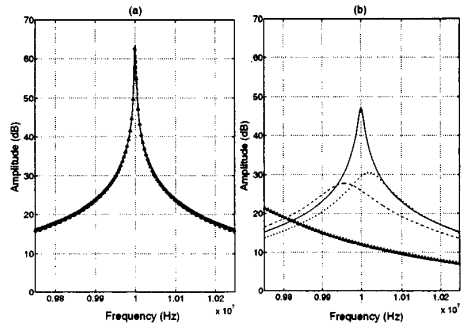

Figure 5: Simulation results of the LDI (triangle), P2P (dotted), TDL (dashed), I2P (solid) for f_{clock}=40 MHz (a) $f_u = \infty$ and $A_{dc} = 120$ dB (b) $f_u = 160$ MHz and $A_{dc} = 60$ dB.

but also allows the operation to remain functional down to 1 V supply voltage.

6. LOW VOLTAGE BANDPASS $\Delta\Sigma$ MODULATOR

The proposed LV SC resonator circuit was used to implement a fourth-order bandpass $\Delta\Sigma$ modulator. In the previous section, the I2P resonator and the others were simulated in single-sampling mode, where the clock frequency was equal to $f_{sampling}$ and the resonance occurs at $f_{clock}/4$. Our I2P structure inherently allows effective double sampling operation because the structure requires four distinct phases (see Fig. 3). SWITCAP2 simulation result is shown in Fig. 6 for f_{clock}=40 MHz with effective double-sampling (using four phases), hence f_{center}=20 MHz.

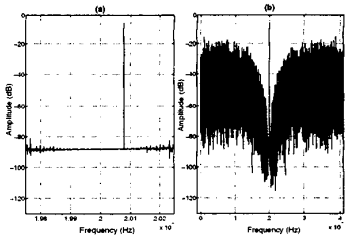

Figure 6: Simulation results for a low-voltage fourth-order bandpass $\Delta\Sigma$ modulator (a) within a 500 kHz frequency interval (b) from DC to $f_{sampling}/2$.

There are double-sampling bandpass $\Delta\Sigma$ modulator implementations described in previous work [5-6] but they have mirror image problems because of the input-sampling path mismatch. The problem is that the input capacitors sample the signal with the clock frequency equal to $f_{clock}/2$, and hence any mismatch between input capacitors will introduce a mirror image, which is typically only 40 dB lower than the fundamental signal at passband. This limits the SFDR of the bandpass $\Delta\Sigma$ modulator [5-6].

In the double-sampling I2P structure, potentially, there are two mismatch problems. One is path mismatch and the other one is input capacitor mismatch.

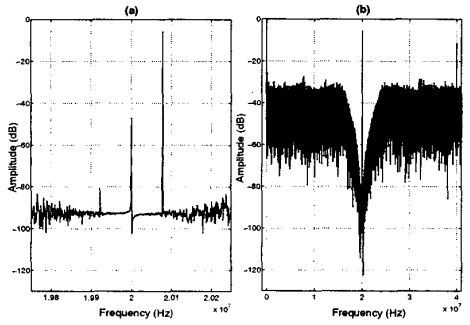

Figure 7: Simulation results with 1% capacitor mismatch and offset voltages up to 15 mV for 2^{17} FFT points (a) within a 500 kHz frequency interval (b) from DC to $f_{sampling}/2$

Our implementation affords low-voltage operation and also allows the circuit to work with double sampling without introducing large mirror images in the passband. In double-sampling mode I2P, the input capacitors will sample the signal at twice of the clock frequency. This means that the large mirror image will occur at $f_{sampling}$, instead of the passband.

The path mismatches are suppressed by the commutation operation. This operation reduces the mismatch problem inside the differential pair, because it changes the flow of the charges every two clock cycles, from the upper path to the lower path.

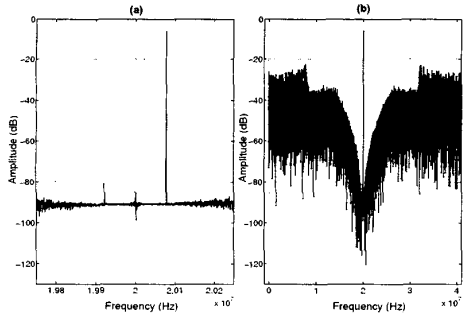

Figure 8: Simulation results with 1% capacitor mismatch and large offset voltages using CDS (a) within a 500 kHz frequency interval (b) from DC to $f_{sampling}/2$.

The last problem, which may occur in the bandpass $\Delta\Sigma$ modulators is the shifting of offset voltages and $1/f$ noise of the opamps into the passband. Since we have $f_{clock} = f_{sampling}/2$ and also a four-phase clock, our structure will have these two noise sources shifted to the center frequency. Simulations show that the bandpass $\Delta\Sigma$ modulator is highly susceptible to first-stage offset voltages.

The simulations were done with 1% capacitor mismatch and random offset voltages up to 15 mV at the inputs of the opamps. The result is shown in Fig. 7. The tone level at $f_{clock}/2$ is about 40 dB below the signal level.

To improve this performance, we have implemented CDS in the bandpass $\Delta\Sigma$ modulator with 8 additional capacitors in order to cancel the offset voltage effects. CDS reduces these effects [9], and restores the SFDR to about 80 dB. As can seen from Fig. 8, the tone at $f_{clock}/2$ is reduced to -80 dB.

7. CONCLUSIONS

In this paper, we have presented a novel low-voltage resonator (I2P), which is insensitive to analog circuit imperfections. We have compared the new structure with existing resonators. The results show that the sampling frequency can be increased without performance degradation. We have also simulated a fourth-order low-voltage bandpass $\Delta\Sigma$ modulator by using the I2P resonators. Simulations were performed to predict the effects of random offset voltage, $1/f$ noise, and mismatch. The results show an SFDR around 80 dB, which is adequate for wireless communication applications. Potentially, the sampling frequency can be increased to higher IF frequencies even with low dc gain and bandwidth.

8. ACKNOWLEDGMENTS

The authors would like to thank José Silva and Tetsuya Kajita for their valuable discussions.

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