RADIX-BASED DIGITAL CALIBRATION TECHNIQUE FOR MULTI-STAGE ADC

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ABSTRACT

This paper describes a digital-domain self-calibration technique for multi-stage analog-to-digital converter (ADC). An accurate calibration is achieved by using a modified radix-based calculation. The equivalent radix-based error term for each stage is extracted by measuring major carry jumps from the ADC transfer curve. A new multiplying digital-to-analog converter (MDAC) architecture using $V_{ref}/2$ (instead of V_{ref}) is used to reduce the number of error terms in each stage. The radix-based digital calibration technique calibrates capacitor mismatch as well as finite opamp dc gain, while the digital redundancy compensates for opamp and comparator offsets and signal-independent charge injection.

1. INTRODUCTION

The increasing demand for high-resolution ADCs has stimulated many innovative design solutions to overcome the finite accuracy set by analog building blocks. One of the most innovative solutions in recent years is the digital calibration technique which does not require manually modifying nor having extra analog circuitry [1]. The key concept of this technique is to measure component mismatch by the converter itself, and then the measured value is either directly subtracted from the digital output [2]-[5] or used for linearizing the ADC output [6], [7]. The former approach can only calibrate front-end conversion stages. The calibration accuracy is also limited by the remaining conversion stages which equally suffer from analog inaccuracy (e.g. component mismatch). In the latter approach, the technique described in [7] is only applicable to a single-stage algorithmic converter and the one reported in [6] requires extra calibration DAC for each pipeline stage.

In this paper, a digital calibration technique for multi-stage ADC is described. The new technique compensates capacitor mismatch and finite opamp dc gain. Use of digital redundancy also compensates for opamp and comparator offsets and signal-independent charge injection. The key advantage of this technique is that the calibration accounts for each stage's error so that the calibration accuracy is not limited by the remaining stages.

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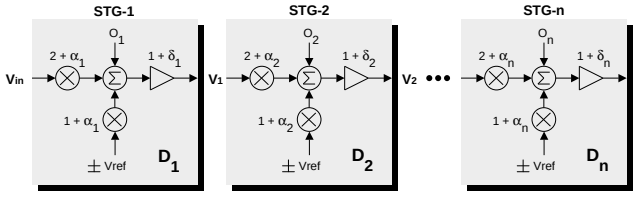

Figure 1: Block diagram of a multi-stage ADC with error sources.

2. PROPOSED DIGITAL SELF-CALIBRATION

Fig. 1 shows the block diagram of a multi-stage ADC, with 1-bit-per-stage architecture. Non-ideal terms including capacitor mismatch, offsets, and finite opamp dc gain are denoted by terms α_i, o_i, and δ_i, respectively. These error sources, shown in Fig. 1, are based on the $\times 2$ MDAC with widely used "capacitor flip-over topology". The constant offset does not affect the ADC linearity and unimportant for most applications. Assuming that the ADC is ideal, the digital output can be calculated as follows:

$$\begin{aligned} D_{out} &= D_n + D_{n-1}\cdot(2) + D_{n-2}\cdot(2)^2 \\ &\quad + D_{n-3}\cdot(2)^3 + D_{n-4}\cdot(2)^4 + \cdots \end{aligned} \quad (1)$$

However, in the presence of error terms, α_i and δ_i directly affect the ADC performance. Eq. (1) would be directly affected and would no longer provide a linear transfer curve. For a special case, as in a single-stage algorithmic ADC, where $\alpha_i = \alpha$ and $\delta_i = \delta$, the residue voltage can be expressed as

$$V_i = ra \cdot V_{i-1} + D \cdot V_r, \quad (2)$$

where $ra = (2+\alpha)\cdot(1+\delta)$, $V_r = (1+\alpha)\cdot(1+\delta)\cdot V_{ref}$, and $D = \pm 1$ (depending on the input level). V_r is a newly defined reference level, which is a changed gain term and not

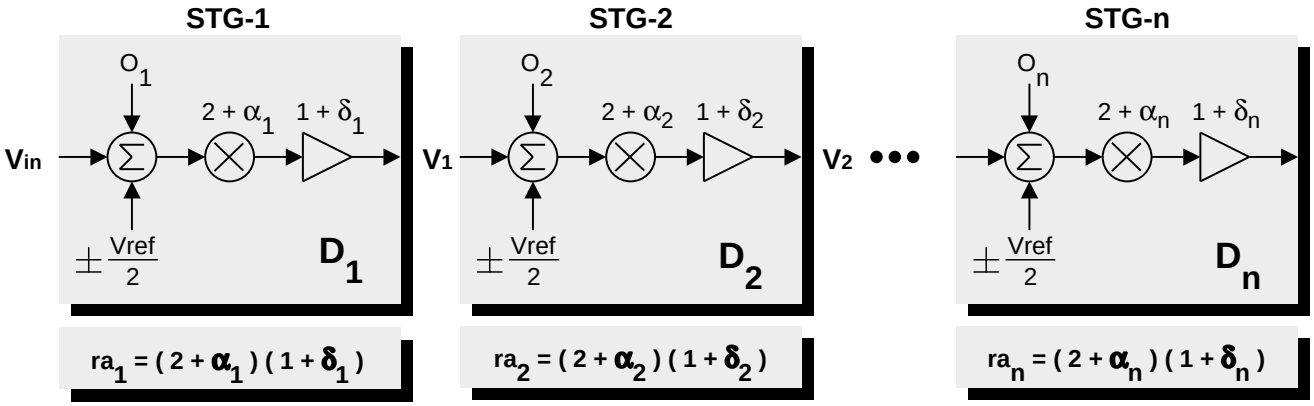

Figure 2: Block diagram of a proposed multi-stage ADC.

a linearity error. As a result only one equivalent error term ra exists. The output of the ADC can now be calibrated with a simple radix calculation based on the modified radix number [7]:

$$\begin{aligned} D_{out} &= D_n + D_{n-1}\cdot(ra) + D_{n-2}\cdot(ra)^2 \\ &\quad + D_{n-3}\cdot(ra)^3 + D_{n-4}\cdot(ra)^4 + \cdots \end{aligned} \quad (3)$$

In a multi-stage ADC, however, the residue voltage at the i^{th} stage can be as shown:

$$V_i = ra_i \cdot V_{i-1} + D \cdot V_{ri}, \quad (4)$$

where $ra_i = (2+\alpha_i)\cdot(1+\delta_i)$ and $V_{ri} = (1+\alpha_i)\cdot(1+\delta_i)\cdot V_{ref}$. Unlike the single-stage case, reference levels do not match between stages, which means V_{ri} is also an error. To properly calibrate these, two errors for each stage, ra_i and V_{ri}, should be measured. The resulting calibration calculation would become much more complicated than the form of Eq. (3).

The newly proposed calibration scheme focuses on two things: (1) having only one error term for each stage and (2) measuring the error term for each stage. Once (1) and (2) are successfully resolved, the multi-stage ADC can be calibrated with a form similar to Eq. (3). Fig. 2 shows the proposed ADC block diagram. To have a set of single equivalent error term per MDAC, both input and reference should see the identical error terms. Instead of using a V_{ref} as in the conventional MDAC, $V_{ref}/2$ is injected. The residue voltage for each stage can now be described by a single modified radix, which includes all error terms.

$$V_i = ra_i \times (V_{i-1} + D \cdot V_{ref}/2). \quad (5)$$

The calibrated digital output would be

$$\begin{aligned} D_{out} &= D_n + D_{n-1}\cdot(ra_1) + D_{n-2}\cdot(ra_2)(ra_1) \\ &\quad + D_{n-3}\cdot(ra_3)(ra_2)(ra_1) + \cdots \\ &\quad + D_1\cdot(ra_{n-1})(ra_{n-2})\cdots(ra_2)(ra_1). \end{aligned} \quad (6)$$

The MDAC based on Fig. 2 can be implemented as shown in Fig. 3. Unlike the conventional "capacitor flip-over topology", a dedicated feedback capacitor C_f is used. During the sampling phase (ϕ_1), input is sampled onto the sampling capacitors C_1 and C_2 while the opamp is reset. During the amplification phase (ϕ_2), the voltage $\pm V_{ref}/2$, is sampled and subtracted from the input so that the residue voltage takes on the form of Eq. (5).

To calibrate this ADC, the error terms for each stage should be measured accurately. The accuracy of the measurement decides the overall ADC resolution. One difficulty is that the exact radix for each stage cannot be known precisely in advance. Estimated initial value will be used to start iterative calculations. In this paper, detailed discussions of a two-stage algorithmic ADC example will be used to illustrate the calibration process.

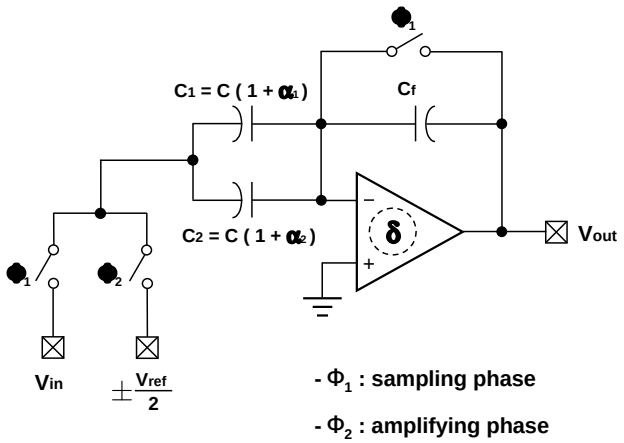

Figure 3: Proposed MDAC schematic.

The measurement procedure starts by monitoring the major-carry jumps. Fig. 4 illustrates a nonlinear transfer

curve of the ADC. The discontinuities occur at the point where the MSBs (we are referring to the first two bits which result from this two-stage algorithmic ADC structure) change from zero to one. These discontinuities are referred to as the *major carry* jumps that are supposed to be 1-LSB under ideal conditions. However, the difference between the radix estimate and the actual value of the equivalent radix causes these jumps to be different from 1-LSB. The first and second major-carry jump errors are caused by the combination of the first and second stage radix estimation errors. By using the 1-LSB as the desirable value of all major-carry jumps, the estimated radix correction can be made as follows:

$$ra_i[n+1] = ra_i[n] - \Delta \cdot (mcarry[n] - 1LSB) \quad (7)$$

where n is the iteration index and Δ is updated step size. The $mcarry$ can be extracted by forcing MSBs to the ADC.

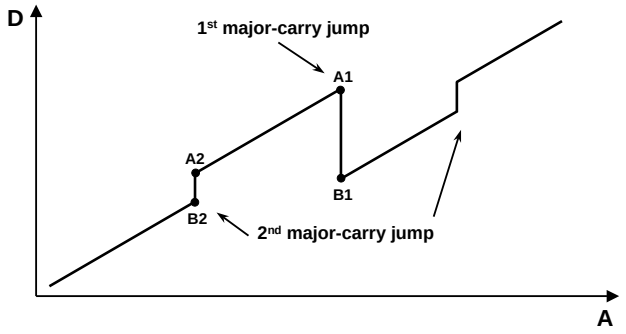

Figure 4: Nonlinear ADC transfer curve.

First, during ra_2 measurement, the estimate ra_1 should be fixed. As shown in Fig. 5(a), "0" is forced to STG-1 and "1" to STG-2. During ra_2 measurement, the very first analog input of STG-1 and STG-2 should be set to zero to obtain the residue of

$$V_{2A} = -(ra_2) \times V_{ref}/2 \quad (8)$$

This voltage is then digitized during the remaining conversion cycles by the ADC itself. With this process, digital output of $A2$ in Fig. 4 can be extracted. Next, "0" is forced to both STG-1 and STG-2 to obtain the residue of

$$V_{2B} = (ra_2) \times V_{ref}/2 \quad (9)$$

which is also digitized to extract $B2$ (of Fig. 4). The second major-carry jump can now be calculated as follows:

$$\begin{aligned} A2 - B2 \quad = \quad & (D_{MSB}[0\ 1] + D_{LSB}[V_{2A}]) \\ & -(D_{MSB}[0\ 0] + D_{LSB}[V_{2B}]). \end{aligned} \quad (10)$$

With the extracted $mcarry$, ra_2 is updated using Eq. (7) and stored in the memory for ra_1 measurement.

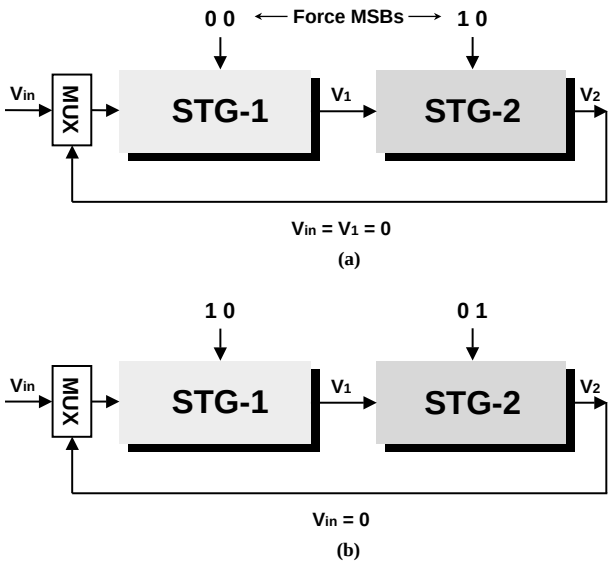

Figure 5: Conceptual block diagram of (a) ra_2 measurement and (b) ra_2 measurement.

Second, for ra_1 measurement, the sequence "1 0" and "0 1" are forced to STG-1 and STG-2, as shown in Fig. 5(b). This time only V_{in} is set to zero. The residues would be obtained as follows:

With "1 0"

$$V_{2A} = -(ra_1) \cdot (ra_2) \times V_{ref}/2 + (ra_2) \times V_{ref}/2 \quad (11)$$

With "0 1"

$$V_{2B} = (ra_1) \cdot (ra_2) \times V_{ref}/2 - (ra_2) \times V_{ref}/2 \quad (12)$$

Each residue extracts $A1$ and $B1$ of Fig. 4, respectively. The first major-carry jump can be calculated as follows:

$$\begin{aligned} A1 - B1 \quad = \quad & (D_{MSB}[1\ 0] + D_{LSB}[V_{2A}]) \\ & -(D_{MSB}[0\ 1] + D_{LSB}[V_{2B}]) \end{aligned} \quad (13)$$

The radix ra_1 is also updated according to Eq. (7) and stored before going back to the calculation/update of ra_2. Since the overall ADC range is composed of a combination of two radices, they are updated alternatively based on one another's latest values until the overall transfer function is fully linear. The update/iteration loop is purely mathematical after initial measurements are made for major carry jumps. This calibration sequence can be extended to an architecture with any number of stages.

3. SIMULATION RESULTS

Fig. 6 shows a behavioral simulation illustrating the measurement of ra_1 and ra_2 based on a 20-bit two-stage algorithmic ADC. Actual values for ra_1 and ra_2 are 1.954321

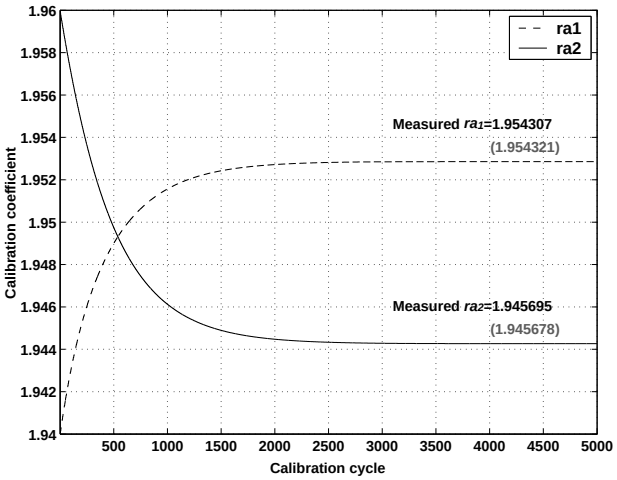

Figure 6: Radices measurement.

and 1.945678. The final iteratively reached values are $ra_1 = 1.954\mathbf{307}$ and $ra_2 = 1.945\mathbf{695}$. The step size Δ should be smaller than 1-LSB step size. In this simulation, 2^{-24} is used. Fig. 7 shows the FFT plots of the resulting calibrated ADC (Fig. 7(b)) in comparison to the ideal one (Fig. 7(a)). The calibrated output spectrum is nearly identical with the ideal one.

4. CONCLUSIONS

A radix-based digital self-calibration technique for multi-stage switched-capacitor ADCs was described. The calibration scheme is enabled by use of equivalent radix architecture, major carry measurements, and mathematical update/iteration loop. The proposed technique corrects for both capacitor mismatch error and opamp finite dc gain error, while digital redundancy compensates for opamp/comparator offsets and signal-independent charge injection.

5. REFERENCES

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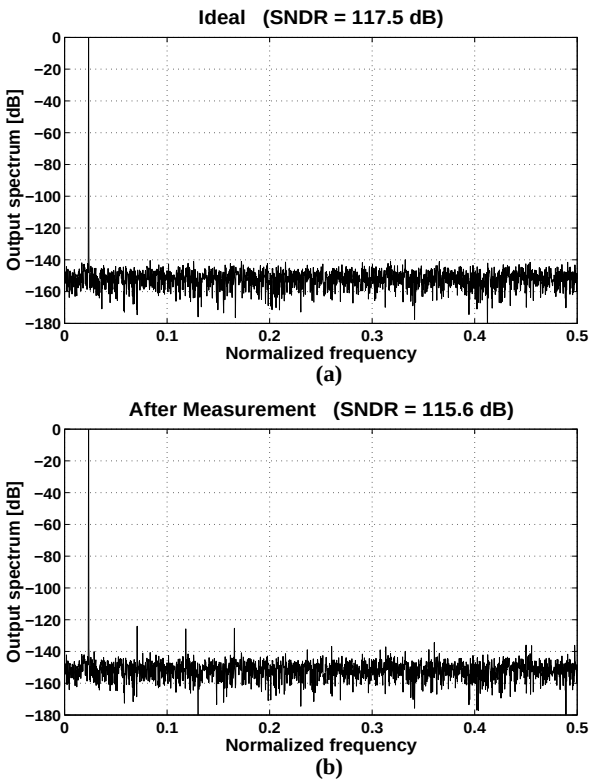

Figure 7: FFT plots of (a) ideal and (b) calibrated ADC.

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