DIGITAL CORRELATION TECHNIQUE FOR THE ESTIMATION AND CORRECTION OF DAC ERRORS IN MULTIBIT MASH $\Delta\Sigma$ ADCS

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ABSTRACT

A fully digital algorithm is described for acquiring and correcting the errors of the feedback DAC used in a multibit $\Delta\Sigma$ MASH ADC. The method operates in the background and is highly accurate. It is particularly useful for wideband ADCs, where mismatch error shaping becomes ineffective. Combined with an improved digital adaptive compensation technique, which greatly reduces the raw quantization leakage in MASH architecture, it makes the design of fast and accurate ADCs using inaccurate components possible.

1. INTRODUCTION

In most state-of-the-art $\Delta\Sigma$ ADCs, multibit internal quantizers are used to obtain improved stability and resolution. The key problem then is how to deal with the inherent nonlinearity of the feedback DAC. Various techniques [1]-[7] have been suggested to improve the effective DAC linearity. These included randomization [1], mismatch error shaping (see, e.g., [2]), direct error correction [3][4] and digital error correction[5][6][7]. Randomization eliminates harmonics, but raises the noise floor; mismatch error shaping is highly effective for high oversampling ratios (OSR > 32), but not useful for wideband ADCs where OSR values as low as 4 may have to be used. The digital correction technique of [5] needs extra DAC unit elements and a modified noise transfer function, while the method of [7] needs an auxiliary ADC. This paper describes a fully digital correction method which acquires a digital estimate of the DAC element errors from the DAC input signal and the overall ADC output signal, after both signals were digitally preprocessed. Like the algorithm recently proposed by Galton to improve the accuracy of pipeline ADCs [8], the method uses the correlation of these digital signals. It can be used even for very low OSRs, and hence it is applicable to wideband signals. Simulations indicate that very accurate results can be obtained in a relatively short time after power-up. Since the process operates in the background, the correction process can follow any drift effects caused by environmental changes (e.g., temperature variations).

The method is here proposed in the context of MASH (or cascaded) architecture, which suffers from raw quantization noise leakage, but it should be applicable to single-loop ADCs as well. The digital adaptive leakage compensation technique of [9] is here accelerated and used with the proposed technique. These two fully digital calibration techniques together make it possible to build highly accurate ADC, wideband $\Delta\Sigma$ from inaccurate analog circuitry.

2. THE PRINCIPLE OF THE DAC CORRECTION SCHEME

Fig. 1 shows a MASH $\Delta\Sigma$ ADC which uses the proposed technique. The first stage of the ADC is a second-order structure with relaxed linearity requirements on the first integrator, as proposed in [10]. Here, it uses a multibit quantizer. Errors of the DAC in its feedback path limit the overall conversion linearity and need to be corrected. The DAC has $M + 1$ levels and M unit elements, so the thermometer-coded output of the ADC, $d(k)$, has a wordlength of M. A scrambler (SCR) precedes the DAC which randomly reorders these M bits. $b(k)$ is the scrambled data, each bit of which determines the use of one unit element. Suppose each unit element has an ideal output value of 1. The average of their real outputs are α. The real output of the ith element deviates from α by αe_i, and

$$\sum_{i=1}^{M} e_i = 0. \tag{1}$$

Then, the output of the DAC is

$$a(k) = \alpha \sum_{i=1}^{M} b_i(k) + \alpha \sum_{i=1}^{M} b_i(k) \cdot e_i + v_{off}, \tag{2}$$

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where v_{off} is the constant DAC offset. Each error e_i is modulated by a sequence $b_i(k)$.

In the output $y(k)$ of the ADC, the modulated errors are also affected by the DAC error transfer function, as shown below:

$$\begin{aligned} y(k) &= u(k) \circledast stf(k) + q(k) \circledast ntf(k) \\ &\quad + \alpha \sum_{i=1}^{M} [b_i(k) \circledast etf(k)] \cdot e_i + v_{off} \circledast etf(k), \end{aligned} \tag{3}$$

where $u(k)$ is the input signal and $q(k)$ is the quantization noise introduced by the quantizer in the second stage, while $stf(k), ntf(k)$ and $etf(k)$ are the impulse responses of signal transfer function, noise transfer function and DAC error transfer function, respectively. The symbol $\circledast$ denotes discrete convolution.

To acquire the error values from the ADC output, we need to suppress sufficiently the interferences from the input signal, quantization noise and DAC offset. The input signal is at lower frequencies, and hence can be partially suppressed by a high-pass filter, HPF, which also suppresses the DAC offset. This filtering will not attenuate the modulated errors too much, because due to the random scrambling the $b_i(k)$ have their power distributed over a wide spectrum. For the quantization noise, which also has a wide spectrum, filtering does not work. However, quantization noise is a random signal and is uncorrelated with the modulated DAC errors. Therefore, correlating the high-pass-filtered ADC output with the modulating sequences $b_i(k)$ should suppress the quantization noise and extract the errors. Unfortunately, the sequences $b_i(k)$ used in the correlation are correlated among themselves, so the result contains linear combinations of the errors. To separate out single errors, which is necessary for later correction, the exact relationship between the sequences should be used.

The larger the power of the quantization noise, the more clock periods are needed to suppress it. MASH ADCs usually have much less quantization noise power in their final outputs than single-loop $\Delta\Sigma$ ADCs. This is the reason we propose the technique in the context of a MASH ADC here.

Sequences $b_i(k)$ can be separated into two parts: the mean value of all M bit streams plus the individual deviations $n_i(k)$ [11]:

$$b_i(k) = \frac{1}{M} \sum_{j=1}^{M} b_j(k) + n_i(k). \tag{4}$$

Here,

$$n_i(k) = - \sum_{j=1, j \neq i}^{M} n_j(k) \tag{5}$$

holds. The sequences $n_j(k)$ on the right side of (5) can be separated into two parts, a scaled version of $n_i(k)$ plus a sequence $m_i(k)$ which is uncorrelated with $n_i(k)$:

$$n_j(k) = -\beta \cdot n_i(k) + m_j(k), \qquad j = 1 \ldots M, j \neq i \tag{6}$$

Because the scrambling is random, all $n_j(k)$ $(j = 1 \ldots M,\ j \neq i)$ have equal status. It is reasonable to assume, and was also verified by simulations, that β is constant for all j's in (6). From (5), $\beta = (M-1)^{-1}$. Since the $n_i(k)$ $(i = 1 \ldots M)$ obey such simple relations, we can use them rather than the $b_i(k)$ as the correlating sequences. Combining (2), (1) and (4), we can write the DAC output as

$$a(k) = \alpha \sum_{i=1}^{M} b_i(k) + \alpha \sum_{i=1}^{M} n_i(k) \cdot e_i + v_{off} \tag{7}$$

and the MASH output as

$$\begin{aligned} y(k) &= u(k) \circledast stf(k) + q(k) \circledast ntf(k) \\ &\quad + \alpha \sum_{i=1}^{M} n_i'(k) \cdot e_i + v_{off} \circledast etf(k), \end{aligned} \tag{8}$$

where

$$n_i'(k) = n_i(k) \circledast etf(k).$$

The errors e_i are thus modulated by $n_i(k)$ in the DAC output.

On the basis of the derivation given above, the error acquiring and correction process is performed as follows (see Fig. 1): 1.$\overline{b}(k) = \frac{1}{M} \sum_{i=1}^{M} b_i(k)$ is subtracted from $b(k)$. 2.The estimate of $n_i'(k)$ is obtained in the digital domain by filtering $n_i(k)$ with a digital filter $\bar{E}\bar{T}\bar{F}$, emulating ETF (in this case just z^{-2}), resulting in $\hat{n}_i'(k)$. 3.The $n_i'(k-l)$ are correlated (in block CORR) with the high-pass-filtered ADC output $y'(k)$, giving

$$\hat{e}_i(k) = \left(\frac{M-1}{M} \right) \cdot \frac{\sum_{m=0}^{k} [y'(m) \cdot n_i'(m-l)]}{h_{HPF}(l) \cdot \sum_{m=0}^{k} [n_i'(m-l)]^2}. \tag{9}$$

$h_{HPF}(l)$ is the largest impulse-response sample of the HPF. Due to the HPF, y' contains delayed versions of $n_i'(k)$ multiplied by the correponding impulse-response samples of the HPF. They are uncorrelated between each other because the $n_i'(k)$ are white noises. We just choose the largest one $n_i'(k-l)$ to extract the DAC errors from.

The estimated results $\hat{e}_i$ are stored in the RAM and are updated in every clock period. They are read out to multiply the $\hat{n}_i'(k),\ i = 1 \ldots M$, and the result is subtracted from $y(k)$ to give the corrected output

$$z(k) = y(k) - \sum_{i=1}^{M} [\hat{n}_i'(k) \cdot \hat{e}_i]. \tag{10}$$

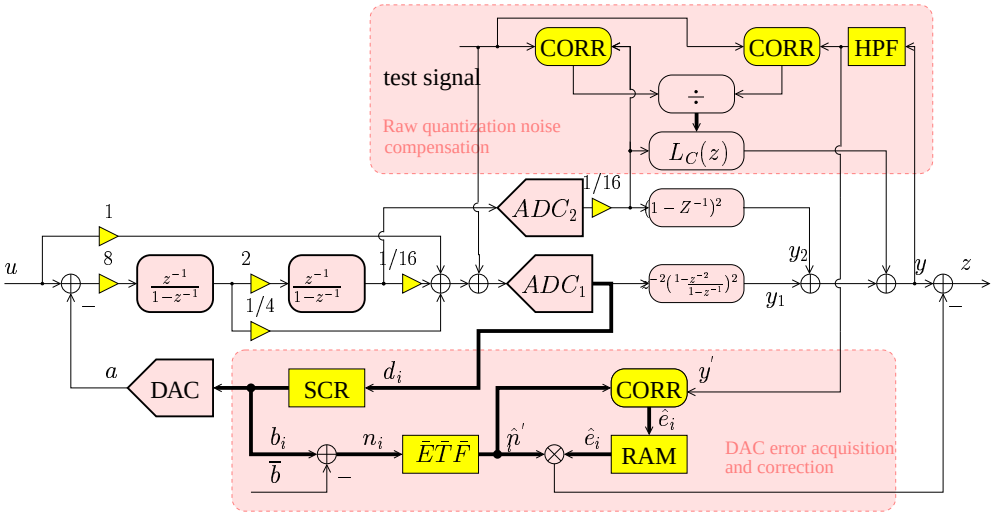

Fig. 1. MASH ADC with adaptive compensation and DAC error correction.

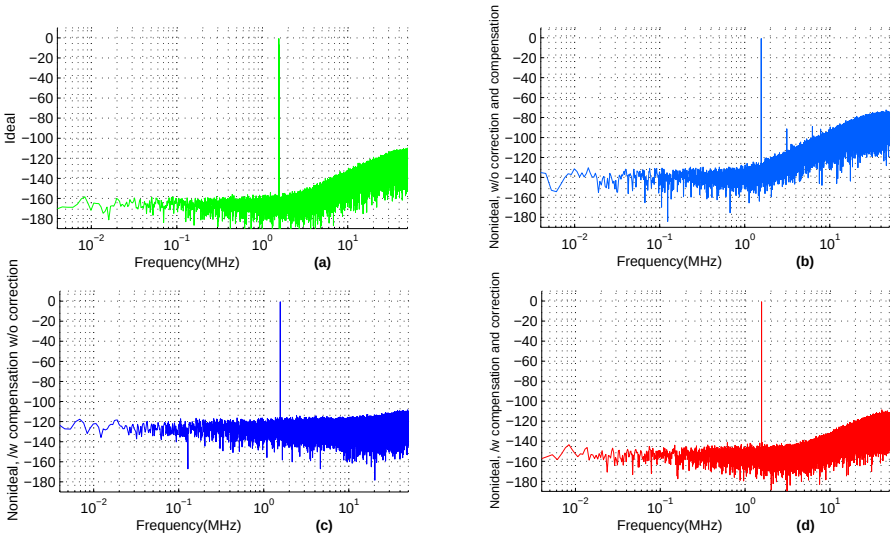

Fig. 2. Simulation results of the DAC error correction working with the adaptive compensation.

3. SIMULATION RESULTS

The DAC correction method is here proposed in the context of MASH $\Delta\Sigma$ ADCs, which suffers from the quantization noise leakage. A fully digital adaptive compensation technique was presented in [9] to solve this problem.

The system in Fig. 1 also includes an improved adaptive compensation. The high-pass filter is also used in the adaptation process. Moreover, instead of fixed adaptation step, adjustable adaptation step is used. Due to these modification, the adaptation process is greatly accelerated.

Fig. 2 shows the simulation results. All simulations were done using Simulink and the Schreier Toolbox for $\Delta\Sigma$ Modulators [12]. The multibit DAC in the first stage was assumed to have 33 levels and 32 unit elements. A random 0.1% rms error was introduced into the unit elements when modeling the real DAC. 40 dB opamp gains were assumed. With a 1.56 MHz, -0.92 dB sine-wave input, the output SNDR drops from 101.8 dB in the ideal case (Fig. 2(a)) to 62.3 dB in the nonideal case (see Fig. 2(b), where both the quantization noise leakage and DAC errors were present). After 8 blocks of adaptation, in which each block contained 131,072 clock periods, the leakage was perfectly compensated but the DAC errors were still there (Fig. 2(c)), resulting in a SNDR of 82.6 dB. A correction process, lasting 131,072 clock periods following the adaptation process, removed the DAC errors and brought the SNDR up to 100.9 dB (Fig. 2(f)) which is very close to that of the ideal case. In practice, the adaptation process and the correction process are continuously repeated to track the changing of parameters.

4. CONCLUSION

A digital algorithm was described for the correction of the nonlinear distortion introduced by the internal DAC in a multibit $\Delta\Sigma$ ADC. The correction scheme does not rely on a high oversampling ratio, and hence is particularly useful for wideband data converters which cannot use mismatch shaping for suppressing the inband DAC errors. A simulation example verifies the high accuracy of the ADC achievable by the proposed technique working the improve digital adaptive compensation which handle the quantization noise leakage in the MASH architecture.

5. REFERENCES

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