HIGH-SPEED PIPELINED A/D CONVERTER USING TIME-SHIFTED CDS TECHNIQUE

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ABSTRACT

A *time-shifted* correlated double sampling (CDS) technique is used to compensate for the finite opamp dc gain in the context of a pipelined analog-to-digital converter (ADC). This technique can significantly reduce the errors due to the finite opamp gain without compromising the conversion speed. This is particularly useful for the design of low-voltage and high-speed pipelined ADCs where the trade-off of opamp dc gain and bandwidth is critical. Behavior simulation results confirm the effectiveness of this new technique.

1. INTRODUCTION

The pipelined ADC architecture has become an attractive choice for applications such as high performance digital communication systems and waveform acquisition systems [**?**]. The rapid developments of these applications are driving the design of ADCs towards higher speed and lower power supply voltage with the CMOS technology scaling. This trend poses great challenges to conventional pipelined ADC designs which rely on high-gain operational amplifiers to produce high-performance converters, because at low power supply voltage and high speed operation, large open loop opamp gain is difficult to realize. As a result, the finite opamp gain is becoming a major hurdle in achieving both high speed and high resolution. Several analog and digital calibration techniques have been proposed to address the correction of the errors due to the capacitor mismatch and the finite opamp gain [**?**]-[**?**]. However, they faced practical limitations and added amount of complexity. Therefore, new, simple, and efficient opamp gain error correction techniques would be worthy of focused research.

In the following section , a *time-shifted* correlated double sampling (CDS) technique is described. The newly proposed technique is used for finite opamp dc gain compensation in the context of a low-voltage and high-speed pipelined ADC.

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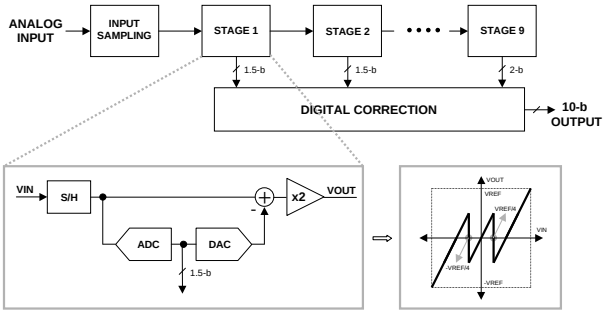

Fig. 1. Block diagram of a typical 10-bit (1.5-bit-per-stage) pipelined ADC.

2. TIME-SHIFTED CDS TECHNIQUE

Fig. **??** shows the block diagram of a conventional 10-bit pipelined ADC utilizing 1.5-bit-per-stage architecture. This architecture is commonly used due to its nice trade-off between speed and power consumption at architectural level. It consists nine cascaded stages. In each stage (except the last stage which has only a 2-bit flash ADC), the input signal is first quantitized by a sub-ADC (flash ADC), then the output digital code is converted back to an analog signal by a sub-DAC. This quantitized analog signal is then subtracted from the input signal, resulting in a residue that is amplified and then passed onto the next stage. In switched-capacitor implementation, the functions of sub D/A conversion, subtraction, and amplification are combined together. Typical switched-capacitor implementation of this block called multiplying digital-to-analog converter (MDAC) is shown in Fig. **??**. The output of this MDAC is given by

$$V_o = \left(\frac{C_s + C_f}{C_f}\right) \cdot V_i - \left(\frac{C_s}{C_f}\right) \cdot v_R + e, \qquad (1)$$

where V_R is $\pm V_{ref}, 0$ depending on the result of sub A/D conversion, and e is the error due to the finite opamp gain. It is given by

$$e = \frac{-1}{A}\left(1 + \frac{C_s}{C_f}\right) \cdot V_o. \qquad (2)$$

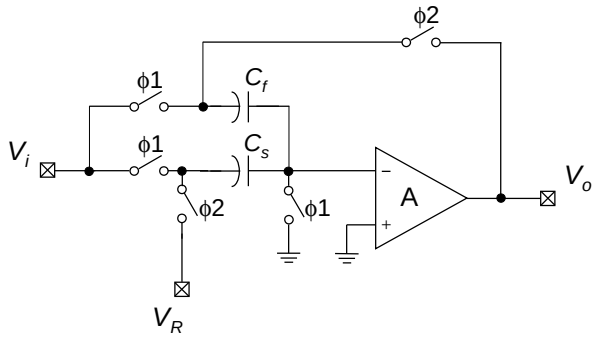

Fig. 2. A typical MDAC in a pipelined ADC with 1.5-bit-per-stage.

This error is inversely proportional to opamp gain A, and it will directly deteriorate the linearity of overall ADC.

Fig. **??** shows the proposed *time-shifted* CDS technique to be used in a 10-bit pipelined ADC. The proposed architecture has two pipeline paths working in parallel. One represents the predictive path which operates for the first five stages, and the other represents the main path which operates for all nine stages necessary for 10-bit ADC (1.5-bit-per-stage). The first five stages of the main pipeline are very similar to their corresponding stages in the predictive pipeline and they share one set of stage sub-ADCs. Both pipeline paths process the same input signal from the first sample-and-hold (S/H) stage. But the signal in the main pipeline is delayed by half clock cycle (one phase) by an additional S/H following the first S/H. The gain error correction is done as follows: The input signal is first processed by the predictive pipeline, and the errors due to finite opamp dc gain are stored and then passed onto the corresponding stages in the main pipeline half clock cycle (one phase) later to cancel the gain errors of those stages. This approach effectively behaves as predictive CDS.

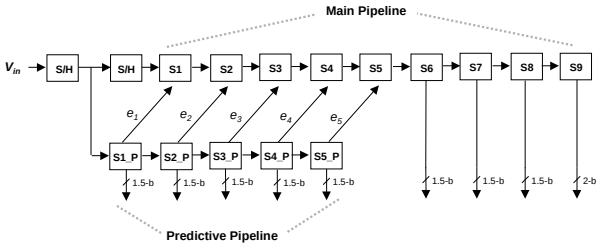

Fig. 3. Proposed pipelined ADC architecture.

In switched capacitor implementation of this architecture, the MDACs of predictive pipeline and main pipeline can be combined together. Fig. **??** shows one such MDAC.

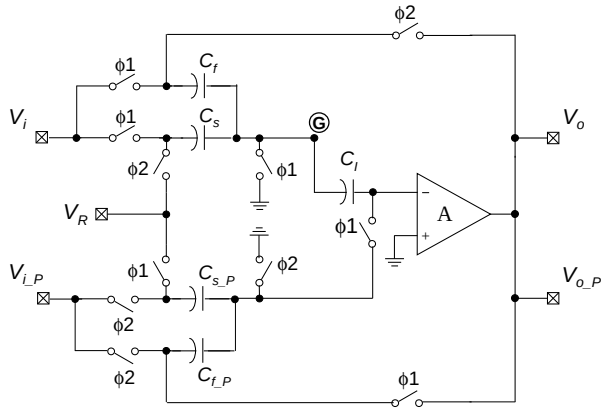

Fig. 4. Proposed MDAC structure.

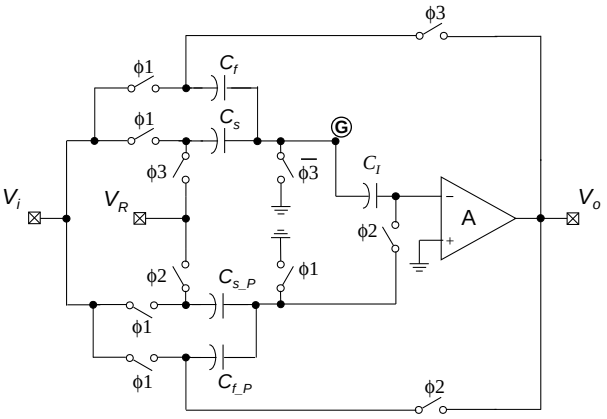

Fig. 5. MDAC employing conventional predictive CDS scheme.

V_i and V_o are the input and output of one stage in main pipeline , whereas V_{i_P} and V_{o_P} are the input and output of the corresponding stage in predictive pipeline. The capacitors are chosen such that $C_{s\_P} = C_{f\_P} = C_s = C_f$. This MDAC employs a similar finite opamp dc gain error correction principle as the conventional predictive CDS technique [**?**]. In the proposed *time-shifted* CDS scheme, the sampling and amplifying operation is actually performed twice. The first operation is done by C_{s_P} and C_{f_P}, the resulted non-zero error voltage due to finite opamp dc gain at the negative input of opamp will be stored in C_I. Then during the second operation done by C_s and C_f, C_I will be connected between the negative input of opamp and node G (the common node of C_s and C_f). Through these operations, a much more accurate virtual ground than the negative input of opamp is created at node G for C_s and C_f if V_{o_P} and V_o are close to each other. Thus the effect of finite opamp gain

will be significantly reduced for the second operation.

The main difference between this proposed *time-shifted* CDS technique and conventional predictive CDS technique described in [**?**] is that the input has to be held constant over two operations in each stage for the conventional CDS technique[**?**], while in the proposed scheme the input signal goes through two separate paths, and the inputs of the MDACs in these two paths are allowed to be slightly different down the pipeline while allowing slightly less effective operation of CDS. If we were to apply conventional CDS technique directly to a pipelined ADC, we would need one extra clock phase to hold the input signal constant over two clock phases. The resulted three clock phase scheme puts a large penalty on the speed of A/D conversion which is unacceptable for the designs pursuing maximum speed. Fig. **??** shows a possible MDAC scheme employing conventional CDS technique. Note three clock phases are used and the output capacitive load is doubled because two sets of capacitors sample at the same time. While for the proposed approach, only two clock phases are needed (unchanged from the regular switched capacitor circuit) and the effective capacitive output load is not increased as it would be in a standard three-phase operated predictive CDS. Therefore The proposed technique can compensate for finite opamp dc gain while maintaining the same speed potential and power dissipation as the regular MDAC without CDS. Only overhead is the need for two sets of capacitors in each MDAC, which would be necessary in all CDS schemes.

Some design issues must be considered when applying the proposed architecture. First, since the inputs of MDAC are not the same for predictive path and main path, the effect of error correction won't be as good as conventional CDS technique as in [**?**] because the effect of error correction relies on the similarity of the inputs of two path. The output error in stage i in main pipeline is given approximately by:

$$e_i = \frac{-i}{A^2}\left(1+\frac{C_s}{C_f}\right)\left[\left(1+\frac{Cs+C_I}{C_f}\right)\cdot V_{oi}(n) - \left(\frac{C_I}{C_f}\right)\cdot V_{oi}(n-1)\right], \qquad (3)$$

where $V_{oi}(n)$ is the current output in the main pipeline, and $V_{oi}(n-1)$ is the output of previous clock cycle in the main pipeline. Note that the error is inversely proportional to A^2. However it will increase linearly from stage to stage down the pipeline. This is because the discrepancy between the outputs of the predictive path and main path will get larger from stage to stage down the pipeline. The second design issue is that the *time-shifted* CDS technique will add extra offset to sub-ADCs in main pipeline. The reason is that the MDACs in main pipeline need to use the digital code generated by the sub-ADCs in predictive pipeline, and this is equivalent to putting an offset to the sub-ADCs in main pipeline. This offset must be corrected, otherwise it will cause code error. Fortunately , pipelined ADCs normally have stage resolution redundancy and employ digital correction to correct the errors come from the stage sub-ADCs. Therefore they can tolerate large offset of sub-ADCs ($\pm V_{ref}/4$ for 1.5-bit-per-stage structure). For this reason, the proposed *time-shifted* CDS technique should not be used for too many stages, lest the accumulated error can overflow the bounds of digital correction and the linearity of overall ADC will be degraded. Another point to be careful about is the size of C_I. If C_I is too large, the gain error of predictive pipeline would be also large, then the effect of error correction is degraded. If C_I is too small, the clock feed-through will change the charge stored in C_I, then the the effect of error correction is also degraded. In a practical design, the size of C_I can be optimized via simulation.

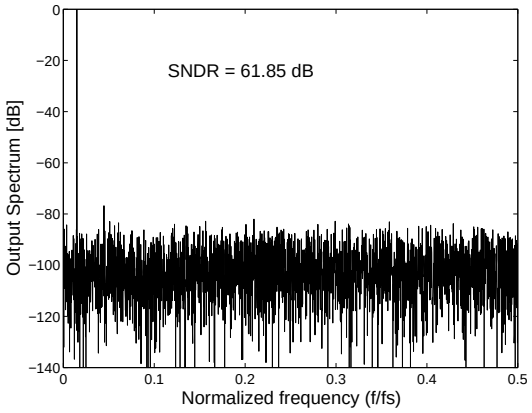

Fig. 6. Pipelined ADC employing conventional CDS technique.

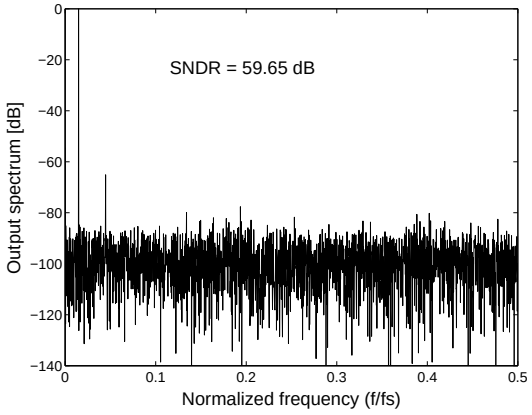

Fig. 7. Proposed pipelined ADC architecture applying *time-shifted* CDS to the first five stages.

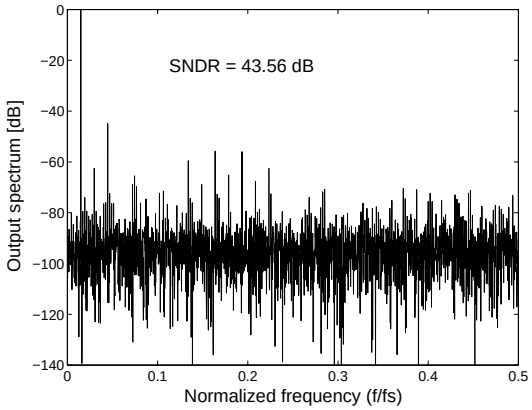

Fig. 8. Pipelined ADC without any gain error correction.

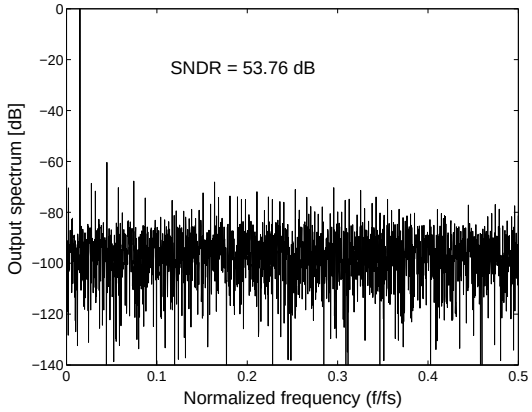

Fig. 9. Proposed pipelined ADC architecture applying *time-shifted* CDS to the first six stages .

3. SIMULATION RESULTS

Some behavior simulations have been done to verify the effectiveness of the proposed architecture. Simulation results of a 10-bit pipelined ADC(1.5-bit-per-stage) are shown in Figs. **??-??**. In simulation, opamp gain was chosen to be 40dB, the capacitor mismatch was assumed to be less than 0.1%, and the random offsets of sub-ADCs are assumed to be less than $\pm V_{ref}/8$. Fig. **??** shows the results of the architecture using conventional CDS technique (recall the extra capacitive load and extra clock phase overhead). Fig. **??** shows the results of the proposed architecture using *time-shifted* CDS technique in the first five stages. It can be seen their performance are very close in terms of SNDR, although the proposed architecture does face small but increasing degradation of error correction down the pipeline. The reason why this presumed degradation does not degrade the overall performance too much is that the opamp gain requirement is also reduced down the pipeline as MSBs are resolved. For comparison, the simulation results of regular pipelined ADC without any gain error correction is shown in Fig. **??**. Note that the SNDR is only about 43dB, that is 16dB lower than the SNDR of architectures with gain error correction. In order to see the effect of hidden degradation of gain error correction that exists in the proposed architecture, the simulation results of the proposed architecture with one more stage using CDS is shown in Fig. **??**. The SNDR decreases by about 6dB in this case. This indicates that the errors accumulated have overflowed the bounds of digital redundancy in sub-ADCs.

4. CONCLUSION

New *time-shifted* CDS technique that compensates for the finite opamp gain in the design of a pipelined ADC is described. The errors due to the finite opamp gain can be reduced significantly without increasing the power dissipation or adding extra clock phase. This new CDS technique demonstrates that CDS can be applied in the first few stages of pipelined ADC without the increased capacitive load or the need for extra clock phase as far as the accumulated error stays within the limits of digital redundancy budget.

5. REFERENCES

[1] J. Ming and S.H.Lewis, "An 8-bit 80-MSample/s Pipelined Analog-to-Digital Converter With Background Calibration," *IEEE J. Solid-State Circuits*, vol. SC-36, pp. 1489–1497, Oct. 2001.

[2] K. Nagaraj, "Area-efficient self-calibration technique for pipelined algorithmic A/D converters," *IEEE Trans. Circuits and Systems-II*, vol. 43, pp. 540–544, Jul. 1996.

[3] H.-S. Lee, "A 12-b 600 ks/s digitally self-calibrated pipelined algorithmic ADC ," *IEEE J. Solid-State Circuits*, vol. 29, pp. 509–515, Apr. 1994.

[4] J. M. Ingino and B. A. Wooley, "A continuously calibrated 12-b, 10-Ms/s, 3.3-V A/D converter," *IEEE J. Solid-State Circuits*, vol. 33, pp. 1920–1931, Dec. 1998.

[5] A.A.Ali and K. Nagaraj, "Correction of Operational Amplifier Gain Error in Pipelined A/D Converters," *Proc IEEE Int. Symp. on Circ. & Sys.*, Sydney,Australia, pp. 1.568–1.571, May 2001.

[6] K. Nagaraj, "Switched-Capacitor Circuits with Reduced Sensitivity to Amplifier Gain," *IEEE Trans. Circuits and Systems*, vol. CAS-34, pp. 571–574, May 1987.