Buck-Boost Switched-Capacitor DC-DC Voltage Regulator Using Delta-Sigma Control Loop

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ABSTRACT

This paper presents a delta-sigma control loop for a buck-boost dc-dc converter with fractional gains. The charge pump used to convert the input voltage acts as a D/A converter in the loop, and its output ripple is frequency shaped by the loop, which also provides the pulse frequency modulation needed for the conversion. Simulation results show that the delta-sigma loop results in spreading the tones in the frequency domain. A suppression of up to 50dB is observed in the 0-20kHz range.

1. INTRODUCTION

Burst mode and pulse frequency modulation control techniques suffer from tones in the frequency domain. The tones are hard to filter, as their frequencies are hard to determine. As a result, the circuits that use the regulated voltage are susceptible to noise in the region of operation. Furthermore, these tones can mix with unwanted signals outside the band of interest and modulate into the desired signal band.

A system is presented which spreads the tones using a delta-sigma control loop around the burst mode or pulse frequency based regulator. For implementation, we have applied the new control loop architecture to an existing buck-boost fractional gain regulator designed at National Semiconductor Corp. [1].

2. FRACTIONAL CHARGE PUMP ARCHITECTURE

Fractional gains can be realized by connecting external capacitors to an on-chip switch array, as shown in Fig. 1 [2]. The switch array is configurable to 7 different gains (G): 1/2, 2/3, 3/4, 1, 4/3, 3/2, and 2. Each gain is implemented in 2 phases of a 1MHz clock. For example, Fig. 2 shows the switches that are used to implement G=2/3.

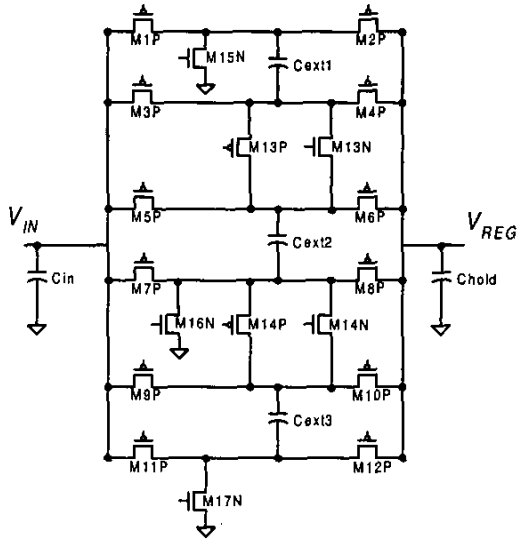

Figure 1: Switch array including external capacitors

To guarantee that current does not flow into the battery (which may result in damage to it) we have to ensure that $G>V_{REG}/V_{IN}$, where V_{REG} = desired output voltage and V_{IN} = unregulated battery voltage. And to maximize efficiency, G must be as close to V_{REG}/V_{IN} as possible. The gain that satisfies these conditions is defined to be the minimum gain, G_{MIN}.

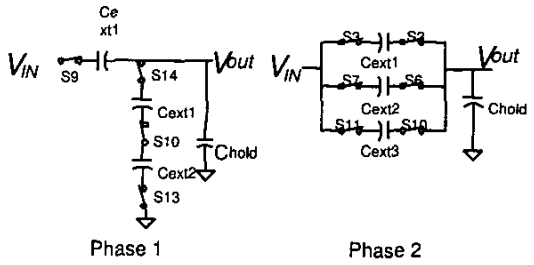

Figure 2: Switch configuration for G=2/3

When the pump provides the gain G_{MIN}, the largest current that it can deliver to the load is approximately

$$I_{MAX} \cong (G_{MIN} * V_{IN} - V_{REG}) / R_{OUT},$$

where R_{out} is the equivalent output impedance of the switch array. Each gain configuration has a unique R_{out}, which is a function of switching frequency, capacitor size and the switch impedances. Selecting a gain larger than G_{MIN} increases I_{MAX}. By increasing the gain only when needed, power is delivered to the load more efficiently.

The diagram example in Fig. 3 shows the minimum gain regions versus V_{IN} for $V_{REG} = 3.3V$.

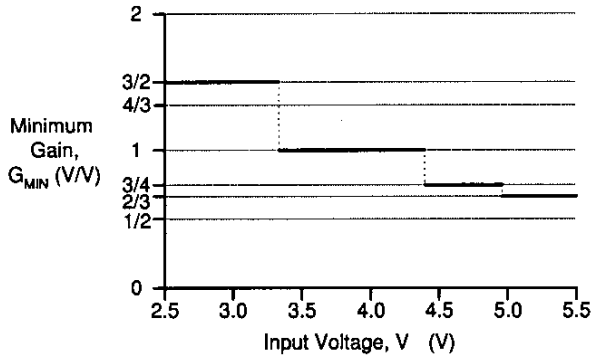

Figure 3: G_{MIN} vs. V_{IN} (for V_{REG}=3.3V)

The simplified block diagram of the regulator is shown in Figure 4. The architecture contains a feedforward path and a gain hopping delta-sigma control loop nested inside the PFM feedback loop. The feedforward path sets G_{MIN} as a function of V_{IN}. The delta-sigma loop consists of a voltage reference, an integrator and a 4-bit flash A/D.

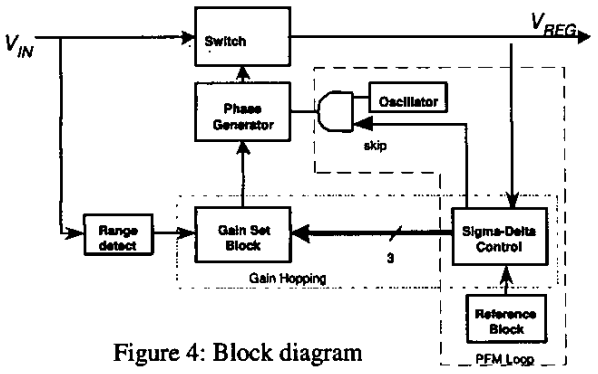

Figure 4: Block diagram

3. CHARGE PUMP MODEL

The LM3352 is a dual phase charge pump, with every second phase being a rest phase. One can model the charge pump by writing charge conservation equations. The modeling can be explained using the gain of 2/3 (Fig. 2). The corresponding steady state output voltage for this gain setting is shown in Fig. 5.

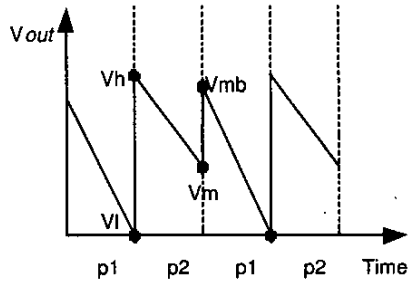

Figure 5: Steady state output for G=2/3

We can compute each of the four voltages marked (Vl, Vh, Vm, Vmb) which signify the switch-over points between the two phases. Each of these can be expressed as a function of circuit parameters and the previous output voltage, i.e,

$$V_h = f(V_l, V_{in}, C_{hold}, C, I_{load});$$
$$V_m = f(V_h, C_{hold}, C, I_{load});$$
$$V_{mb} = f(V_m, V_{in}, C_{hold}, C, I_{load});$$
$$V_l = f(V_{mb}, C_{hold}, C, I_{load}).$$

Thus the charge pump can be modeled as a lossy integrator (Fig. 6) with a loss factor a and constant gain b. The values of a and b change dynamically depending on the present gain, load and input voltage of the charge pump. The relationship with gain, G, for fixed load and input is shown in Fig. 7.

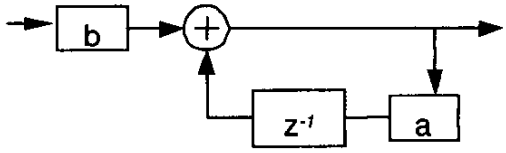

Figure 6: Charge pump model

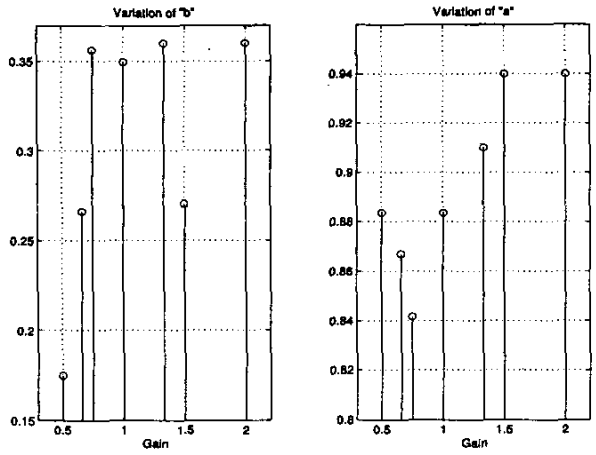

Figure 7: Variation of b and a for different gains with a load of 100mA

3. CONTROL SYSTEM ARCHITECTURE

The system consists of an integrator and a 4-bit flash A/D converter with the charge pump (boxed region) as the D/A converter, as shown in Fig. 8. The 3 MSBs select one of the 7 gain levels and the LSB controls the pump or skip cycle of the charge pump. The error between the desired voltage and the output voltage is integrated, and is fed into the 4-bit flash ADC. As the output voltage approaches the desired voltage, the error signal decreases, reducing the input to the A/D. This causes a smaller gain to be chosen until we are forced to use the minimum gain.

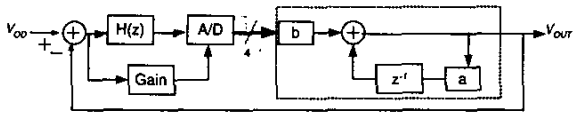

Figure 8: System architecture

Due to the charge pump, a second pole is created in the loop after the quantizer. In order to stabilize the loop, we have added a feed-forward path with a gain greater then 1. Simulations showed that the optimum value of this is 4. The loop also uses a dither signal, not shown in the figure.

The delta-sigma loop makes the gain selection more random and thus spreads the tones. The loop also ensures the use of the minimum gain more often and thus makes the system more efficient. It should be mentioned that the delay through the loop is critical, and that will effect the load and the line response of the regulator.

4. SYSTEM SIMULATION

The original regulator and the proposed architecture have been simulated at system level using C language. The system results for a given condition of input voltage, output voltage and load are shown in Fig. 9. We see that the original architecture employing the traditional pulse frequency modulation is highly tonal in nature all through the frequency range. The proposed architecture with the delta-sigma control loop spreads the tones and has a smoother spectrum. Above 100kHz the noise droops, unlike in a conventional delta-sigma modulator. This is due to the high frequency pole generated by the charge pump.

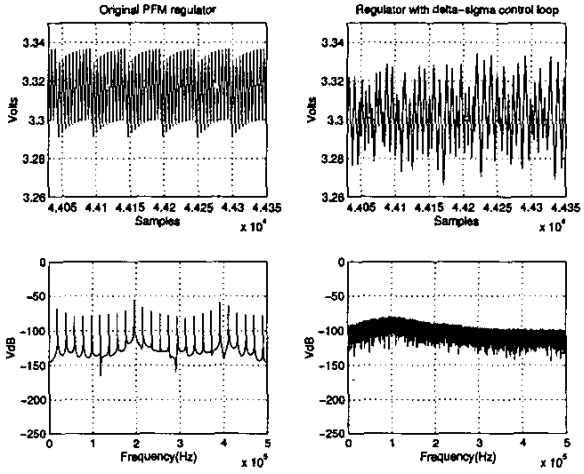

Figure 9: Comparison of the two architectures

The figure also shows the time-domain behavior of both architectures and we can clearly see that the delta-sigma loop makes the output voltage more random. The efficiency of the regulator is given by:

$$\text{Efficiency} = \eta = (V_{REG} / V_{IN} * (M/N)),$$

where M and N are integers and M/N is the gain G.

Using the proposed model of the regulator one can compute the amount of charge delivered by the supply on a cycle-by-cycle basis. This enables us to calculate the average current delivered by the input supply and the overall efficiency of the regulator. Figure 10 shows the efficiency, η, versus V_{IN} for the original and the proposed architectures. The peaks occur near $G_{MIN}*V_{IN}=V_{REG}$.

5. CIRCUIT DESIGN

The proposed architecture has been designed and is being fabricated in a 0.75um CMOS. Since the delta-sigma loop controls the gain selection with an LSB of 150mV single

ended circuitry was used. The integrator and the gain block are standard switched capacitor blocks. The unit capacitance used is 250fF. The A/D implemented is a 4 bit flash structure. There are 16 clocked CMOS comparators [3].

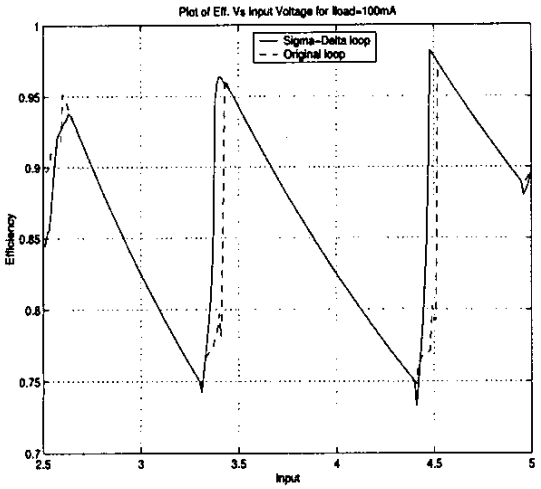

Figure 10: Efficiency plots for the two architectures

The comparator structure is shown in Fig. 11. A resistor ladder sets the voltage levels. The inverters have current sources in them to limit the current flow (power dissipation) through them.

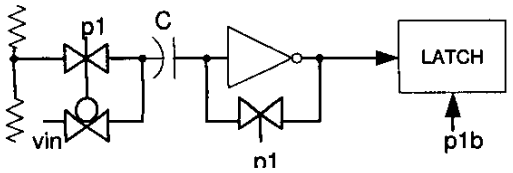

Figure 11: Clocked CMOS comparator

The existing hardware for LM3352 was combined with the delta-sigma control loop in the implementation. The reference generation is shown in Fig 12. There is a bandgap reference and a 7-bit DAC to generate the desired output voltage ranging from 2.5 to 5.5 volts.

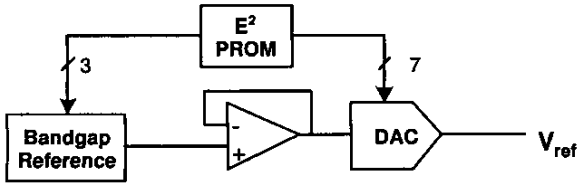

Figure 12: Reference block

The delta-sigma loop was simulated using Spectre and the results for a given set of input, output and load conditions is shown in Fig. 13. We see that the results of the circuit simulations are very similar to those provided by the system simulations in Fig. 9.

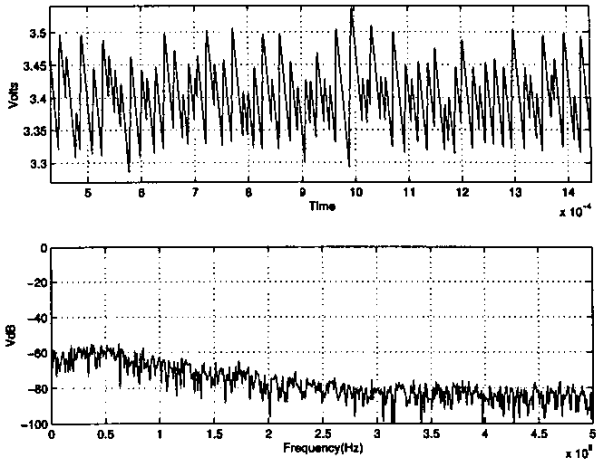

Figure 13: Spectre simulation of delta-sigma loop

6. CONCLUSIONS

This paper described techniques to spread the tones in the burst-mode or pulse-frequency-mode regulators. The simulation results show that we could achieve about 50dB suppression up to 20kHz, and remove the tones from the frequency spectrum. The additional delay through the loop increases the ripple slightly in some cases. The target output voltage may be programmed via a E^2PROM to be any voltage from 1.8V to 4V in 0.1V increments. The input voltage range of 2.5V to 5.5V supports the normal LiIon battery discharge cycle.

ACKNOWLEDGMENT

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