Continuous-Time, Frequency Translating, Bandpass Delta-Sigma Modulator

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Abstract

This paper introduces the concept of frequency-translating, bandpass delta-sigma modulator in continuous-time. The system level design and simulation results of the delta-sigma modulator are presented. The DAC jitter performance of the continuous-time, frequency translating bandpass delta-sigma modulator is presented. The DAC jitter performance of the frequency translating modulator and conventional lowpass delta-sigma modulator are compared

1 Introduction

Bandpass delta-sigma modulators [1] are well suited for the digitization of narrowband signals modulated on a carrier signal. Radio receivers based on direct digitization of intermediate-frequency (IF) signals or radio-frequency (RF) signals are easy to integrate. This is because, once the IF signal is digitized, most of the signal processing tasks like channel filtering, demodulation etcetera can be easily done in the digital domain. This scheme also offers high degree of programmability and is ideal for multi-standard radio receivers.

Unfortunately the design of bandpass delta-sigma modulators tuned to IF signals at high frequency, say 100MHz, in CMOS technology is no easy task. It is very difficult to design a low noise, linear, high Q bandpass loop filter precisely tuned to the intermediate frequency. Moreover the delta-sigma modulator has to be clocked at very high frequency, usually four times the IF signal frequency and the modulator suffers from DAC jitter.

In this paper we introduce a new delta-sigma modulator architecture, in which the IF signal is down converted in to baseband after amplification by a low Q, wideband bandpass filter. The down converted IF signal is digitized by a continuous-time, second-order, lowpass delta-sigma modulator. The output of the lowpass delta-sigma modulator is upconverted and fedback in to the low Q, wideband bandpass filter [2]. The non idealities of all the important blocks in the loop are suppressed by the passband gain of the bandpass filter. Directly mixing the input signal and digitizing it requires low noise amplifier stages in the front end. Unlike the conventional delta-sigma modulators, the new architecture makes use of an integer number of sinusoidal pulses for feedback. Thus the feedback basis function is inherently bandpass. This considerably improves the performance of the delta-sigma modulator in the presence of time-delay jitter and pulse-width jitter in the DAC. Also the sampling frequency of the modulator can be less than the center frequency to which the modulator is tuned. A prototype continuous-time, frequency-translating delta-sigma modulator to digitize IF signals at 100MHz and 200kHz bandwidth at a sampling frequency of 100MHz was designed in $0.35\mu m$ process. Transistor level simulations show that an SNR of 80dB is achievable at a power dissipation of 80mW.

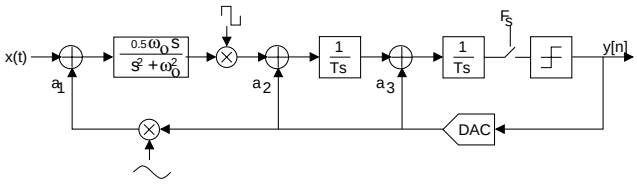

Figure 1: Continuous-time, frequency-translating bandpass delta-sigma modulator

2 System Level Design

The proposed architecture is shown in Fig. 1. The loop feedback coefficients, a_1, a_2, a_3 should be determined such that the delta-sigma modulator is stable. Let us cut the loop infront of the DAC and go thorough the loop inorder to determine the loop gain. The 'non return to zero' (NRZ) single-bit DAC feedback pulse is modulated up by a sinusoidal wave and is amplified by the bandpass filter. The output of the bandpass filter is down converted by the local oscillator to the baseband. The transfer function of the bandpass filter is given by (EQ 1). The transfer function of the bandpass filter evaluated at s = j$(\omega_o + \Delta\omega)$, $\frac{\Delta\omega}{\omega_o} \ll 1$ is given by (EQ 2). it is evident from (EQ 2) that the bandpass filter acts as like an integrator, for frequencies close to the center frequency.

$$H_{bpf}(s) = \frac{0.5\omega_o s}{s^2 + \omega_o^2} \tag{1}$$

$$H_{bpf}(j\Delta\omega) = \frac{\omega_o}{j4\Delta\omega} \tag{2}$$

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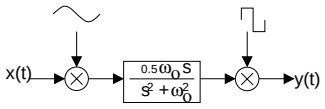

Figure 2: Frequency-translating block

The upconverting mixer, bandpass filter and the downconverting mixer, Fig. 2 together act as a lowpass integrator. Since the downconverted signal bandwidth is much smaller than the center frequency of the delta-sigma modulator, the sampling frequency of the continuous-time delta-sigma modulator can be less than the center frequency of the bandpass delta-sigma modulator. Assuming the sampling frequency is equal to the center frequency and also taking in to account of the gain of the demodulating mixer, the transfer function of the equivalent lowpass integrator is given by (EQ 3), where T is the sampling time period.

$$H_{integrator}(s) = \frac{1}{Ts} \tag{3}$$

Thus the frequency-translating bandpass delta-sigma modulator can be mapped in to an equivalent continuous-time, third-order lowpass delta-sigma modulator. The feedback coefficients for continuous-time, third-order lowpass delta-sigma modulators are $a_1 = -0.05$, $a_2 = -0.3$, $a_3 = -0.6416$ [3]. The same coefficients can be used for frequency-translating bandpass delta-sigma modulator. The response of the frequency-translating portion of the bandpass delta-sigma modulator to a NRZ DAC pulse, of 10ns pulse width is compared to that of its equivalent integrator in Fig. 3. Note that a 4^{th} order lowpass Butter Worth filter was used to remove the high frequency signals resulting from mixing down of the output of the bandpass filter. This explains the time delay between the two responses. The equivalent continuous-time lowpass delta-sigma modulator shown in Fig. 4. The simulated output spectrum of the continuous-time frequency-translating bandpass delta-sigma modulator is shown in Fig. 5.

3 DAC Jitter Performance

In a conventional lowpass delta-sigma, the feedback signal is usually a rectangular current pulse, Fig. 6, the polarity of which depends on the quantizer output. The DAC feedback pulse is characterized by time delay and pulse width. The time delay and pulse width of the DAC feedback signal can vary randomly from clock cycle to clock cycle due to jitter in the clock synchronizing the DAC. It can be shown that the lowpass continuous-time delta-sigma modulator is insensitive to random variations in the time delay associated with the DAC pulse. For a n^{th} order lowpass continuous-time delta-sigma modulator, the noise from DAC time delay jitter

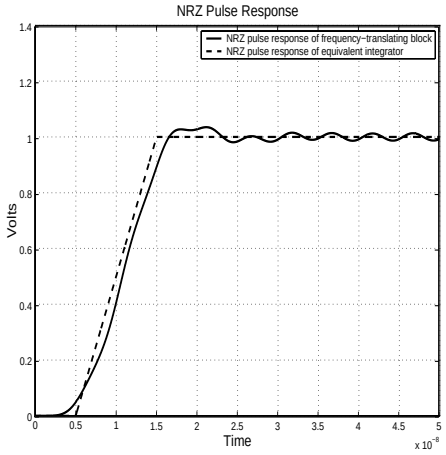

Figure 3: NRZ pulse response of the frequency-translating block and its equivalent integrator

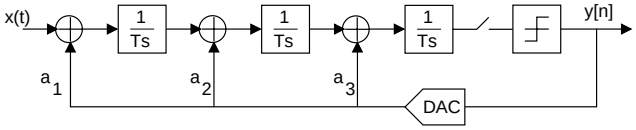

Figure 4: Equivalent continuous-time lowpass delta-sigma modulator

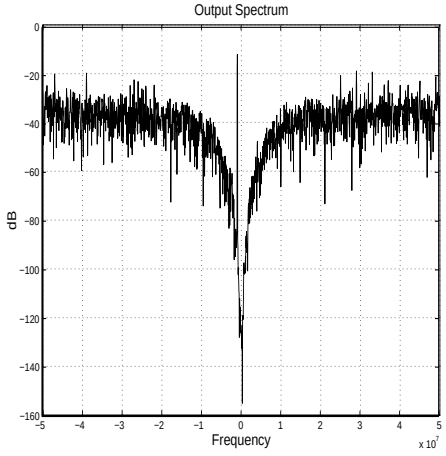

Figure 5: Output spectrum from system level simulations

is $(n-1)^{th}$ order noise shaped [4]. The noise due to pulse width jitter appears directly at the output and limits the maximum SNR achievable. If we can generate the DAC feedback pulse by edge triggering, i.e from a monostable multivibrator, we can reduce the sensitivity of the delta-sigma modulator, to DAC jitter.

The equivalence of continuous-time frequency translating bandpass delta-sigma modulator to continuous-time lowpass delta-sigma modulator was shown in the previous section. The DAC jitter performance of the continuous-time frequency translating bandpass delta-sigma modulator is similar to that of a continuous-time lowpass delta-sigma. The DAC pulse in the case of the frequency translating modulator is given in Fig. 7. Note that the sinusoidal current pulse is chopped at the zero crossings, depending on the quantizer output, to generate the feedback pulse. The frequecny translating modulator output spectrum with 20ps delay jitter and 20ps pulse width jitter are given in Fig. 8 and Fig. 9 respectively. Simulations show that the DAC time delay jitter does not affect SNR in frequency translating bandpass delta-sigma modulator. Frequency translating bandpass delta-sigma is less sensitive to pulse width jitter than the conventional continuous-time lowpass delta-sigma modulator. The pulse width jitter performance of the equivalent lowpass delta-sigma modulator is shown in Fig. 10. Frequency translating bandpass delta-sigma modulator showed 10dB better SNR than its equivalent continuous-time lowpass delta-sigma modulator. This is because sinusoid DAC pulses change their polarity at the zero crossing, there by reducing the noise energy due to switching at the wrong time instant. Note that 'return to zero' DAC feedback was used in the simulations for DAC jitter performance. The center frequency of the delta-sigma is 200MHz and input signal frequency is 200KHz. The phase noise in the sinusoid DAC feedback signal was not considered in these simulations. Simulations show that the phase noise in the sinusoid DAC feedback signal does not modulate the quantization noise in to the baseband. However simulations show a 'phase noise skirt' aroud the I/Q output signals, thus degrading SNR.

4 Conclusions

A new bandpass delta-sigma architecture based on demodulation within the delta-sigma loop is presented. Continuous-time, frequency translating bandpass delta-sigma modulator can be mapped in to an equivalent continuous-time lowpass delta-sigma modulator. Thus the system level design can be done in lowpass domain and do not need tedious calculations. In this architecture the sampling clock frequency can be less than the center frequency to which the modulator is tuned. The modulaor is less sensitive to DAC pulsewidth jitter and time delay jitter.

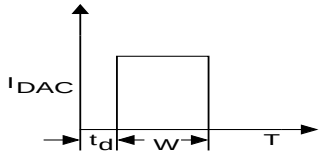

Figure 6: DAC feedback pulse

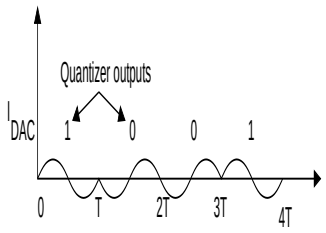

Figure 7: DAC pulse in frequency translating delta-sigma modulator

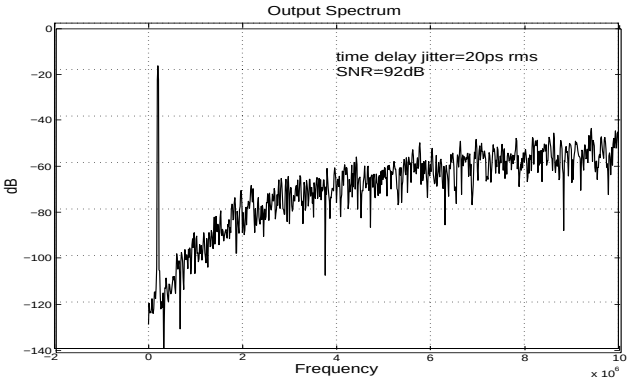

Figure 8: Time delay jitter performance of frequency translating bandpass delta sigma modulator

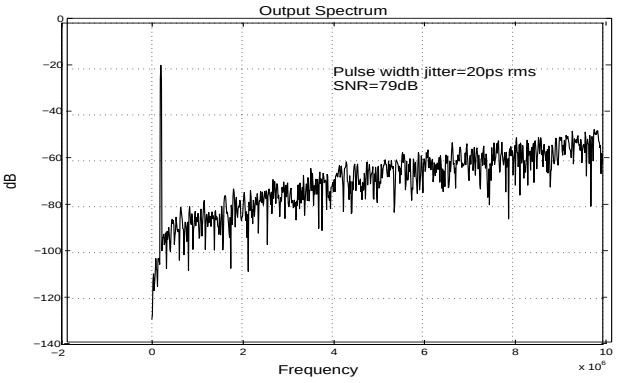

Figure 9: Pulse width jitter performance of frequency translating bandpass delta-sigma modulator

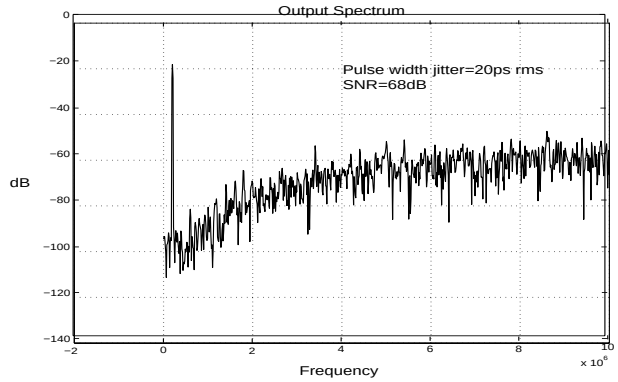

Figure 10: Pulse width jitter performance of continuous-time lowpass delta-sigma modulator

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