AN IMPROVED ALGORITHMIC ADC CLOCKING SCHEME

Min Gyu Kim, Gil-Cho Ahn, and Un-Ku Moon

School of Electrical Engineering and Computer Science
Oregon State University, Corvallis, OR 97331, USA

ABSTRACT

An improved algorithmic ADC clocking scheme is presented. Using an *optimized clock generator*, a significant improvement in conversion speed is achieved in the converter. This proposed *optimized clock generator* removes the wasted time which exists during all conversion cycles except for the first one. This technique can improve the conversion speed up to 82% compared to conventional algorithmic ADCs. Alternatively, static power consumption can also be reduced for a given conversion speed. An algorithmic ADC using the new clocking scheme is validated using MATLAB behavioral simulations.

1. INTRODUCTION

The algorithmic ADC architecture has chosen for applications requiring low power, small chip area, and high-resolution. Several techniques have been developed for high speed algorithmic ADC to improve performance [1], [2]. These techniques all offer improvements to the analog core blocks. Unlike the pipelined architecture, an algorithmic ADC essentially recycles the sample-and-hold amplifier (SHA) and the multiplying digital-to-analog converter (MDAC). With the conventional algorithmic ADC clocking, every conversion step takes the same amount of time although the minimum required conversion time decreases as the number of remaining bits decreases with each step. As a result, the conventional algorithmic ADC wastes time after first conversion cycle. The proposed clock generator can minimize this wasted time. Our proposed clocking scheme offers a significant conversion speed improvement without any change to the ADC analog core blocks.
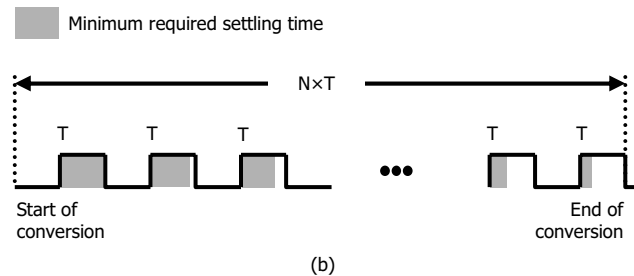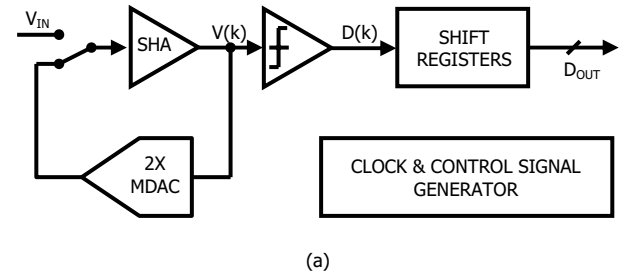
(a)

(b)

Fig. 1. (a) The Conventional N-bit algorithmic ADC structure and (b) the clock diagram of (a).

2. ALGORITHMIC ADC STRUCTURE

A simplified 1-bit/cycle algorithmic ADC structure is shown in Fig. 1(a). For the first bit (MSB) conversion time, $V(1) = V_{IN}$, and the SHA output voltage is doubled in amplitude and added to a reference, resulting in $V(k+1) = 2V(k) + D(k)V_{REF}$. The output of the single bit comparator, $D(k)$, is either +1 or -1. The signal residue is propagated to the next cycle.

For accurate SHA output settling, the minimum required time is

$$t_{SHA} = (n + 1 - k) \cdot \ln 2 / \omega_{SHA}, \qquad (1)$$

where n is the bit number of the algorithmic ADC, k is the number of conversion step, and ω_{SHA} is the bandwidth of the SHA.

The minimum time required for the accurate MDAC output settling can be described as

$$t_{MDAC} = (n-k) \cdot \ln 2 / \omega_{MDAC}, \qquad (2)$$

where ω_{MDAC} is the bandwidth of the MDAC.

Minimum output settling time decreases with the number of conversion bits. Therefore, the wasted time increases as shown in Fig. 1(b). The SHA and MDAC in the algorithmic ADC have to be reused for each conversion step, and they have to satisfy the minimum settling time requirement of the first conversion step. Therefore, the conventional algorithmic ADC wastes time after the first conversion step.

3. OPTIMIZED CLOCK GENERATOR

The proposed clock generator increases conversion speed without changing the analog core blocks. The basic concept of the new clocking scheme is to use optimum timing for every conversion step (instead of the same timing of a conventional design) as shown in Fig. 2(a). In other words, each step is performed as quickly as it can be.

The new clocking scheme can be made from predetermined M phases. Examples of optimized clock sequence for a 10 bit ADC made from 4 phases and 10 phases (conventional = 1 phase) are shown in Fig. 2(b) and Fig. 2(c), respectively. In the example shown in Fig. 2(b), the four different period widths T, 0.75T, 0.5T, and 0.25T are used properly for the ten conversion steps instead of using one same period T. The total conversion time is improved to 65% of the conventional conversion scheme. This translates to an overall conversion rate improvement of 54%. In the example shown in Fig. 2(c), ten different timings from T to 0.1T are used for the ten conversion steps instead of same period T. The total conversion time is improved to 55% of the conventional conversion scheme. This translates to an overall conversion rate improvement of 82%.

To enable the new clocking scheme, the input clock must have some additional phases for generating the optimized clock. Two feasible solutions are shown in Fig. 3(a) and Fig. 3(b). One solution is to provide an input clock with a frequency M times higher than needed for the first stage, as shown in Fig. 3(a). Another solution is to employ integrated PLL/DLL to generate the necessary phases, as shown in Fig. 3(b). This PLL/DLL does not need to be high performance because clock jitter is not important in later stages. Only the first conversion step
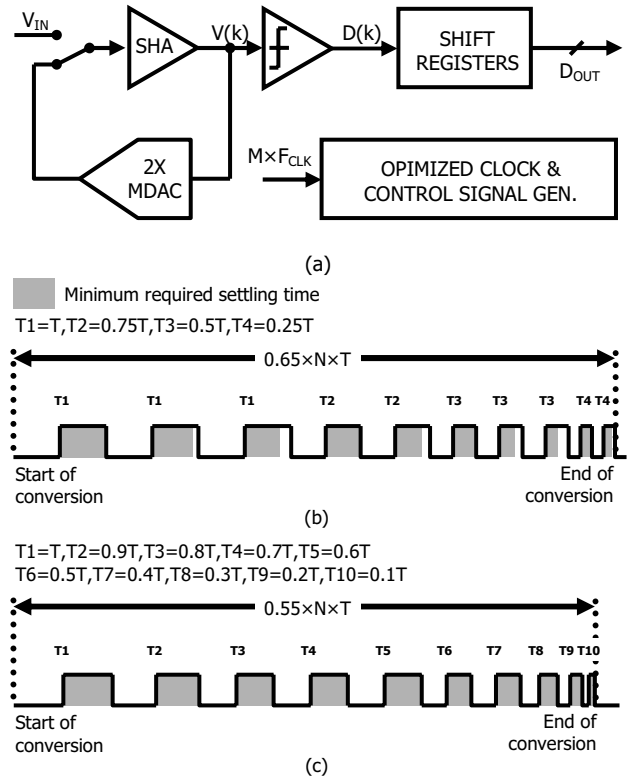

(a)

(b)

(c)

Fig. 2. (a) The proposed N-bit algorithmic ADC structure, (b) a optimized clock diagram which uses 4 phases for 10bit ADC, and (c) a optimized clock diagram which uses 10 phases for 10bit ADC.
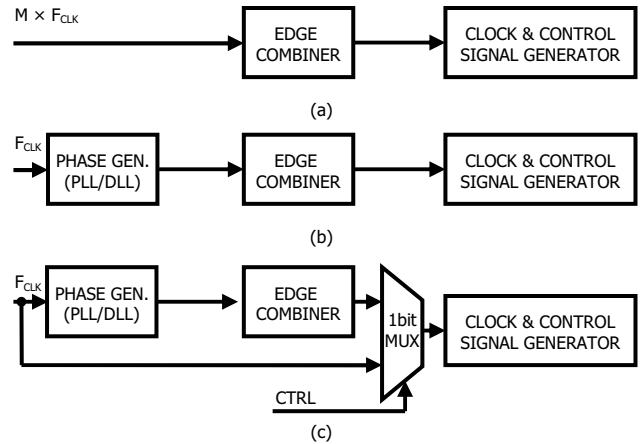

(a)

(b)

(c)

Fig. 3. The optimized clock generator structure: (a) M×F$_{CLK}$ is received directly. (b) Phases are generated from an internal low cost PLL/DLL. (c) The timing for first conversion step is bypassed from phase generator.

where input signal sampling occurs is sensitive to clock jitter, as long as the latter stages/cycles have enough time to settle. Jitter which occurs in the first conversion step is critical as in all ADCs because this can directly limit the input SNDR. Therefore, as illustrated in Fig. 3(c), the timing for first conversion is propagated directly from the external clock input.

The number of phases required to generate the optimized clock is a trade-off between circuit complexity and improvement in conversion speed. For example, if we use 4 phases, then we can achieve 54% more speed as compared to the same ADC without any other notable disadvantages.

4. SIMULATION RESULTS

The proposed clock scheme was compared to a conventional clock scheme using MATLAB Simulations. The algorithmic ADC is modeled with following assumptions: the conversion rate is 3 MS/s; the resolution is 10 bit; the number of phases for optimized clock generation is four; and the SHA and MDAC employ two stage Miller-compensated op-amps which have 70dB DC gain, 33 MHz unity-gain bandwidth, and 60 degrees phase margin.

SNDR simulation results and FFT plots for the two clock schemes are shown in Figs. 4, 5 and 6, respectively. With the new clocking schemes, the conversion speed increases from about 3 MS/s to 4.62 MS/s, the anticipated conversion speed improvement of 54%.

5. CONCLUSIONS

An efficient optimized clock generation scheme for algorithmic ADCs is proposed. With this technique, up to an 82% in conversion speed can be achieved in comparison to a given conventional algorithmic ADC. Alternatively, static power consumption can also be reduced for a given conversion speed. This is achieved by employing simple additional digital circuits.

6. REFERENCES

[1] Z. Zheng, B. Min, U. Moon, and G. Temes, "Efficient error-cancelling algorithmic ADC," *Proc. IEEE Int. Symp. Circuit Syst.,* pp. I.451-454,May 2000.

[2] A. Kitagawa et al.,. "A 10b 3MSample/s CMOS cyclic ADC," *ISSCC Dig. Tech Papers,* pp. 280-281, Feb. 1995.

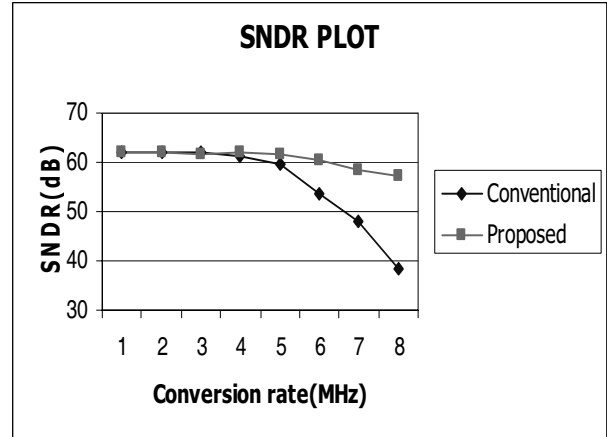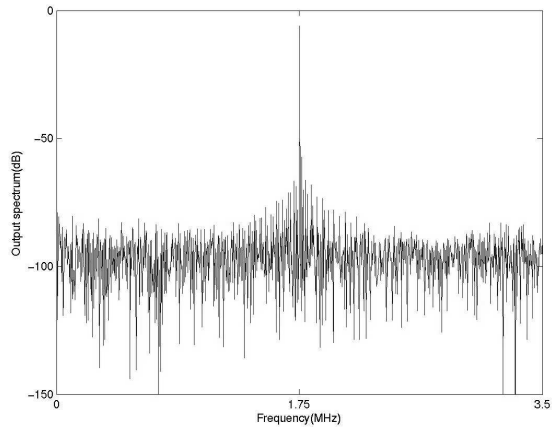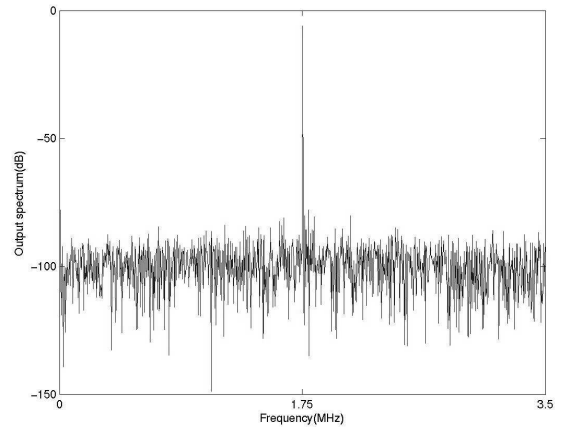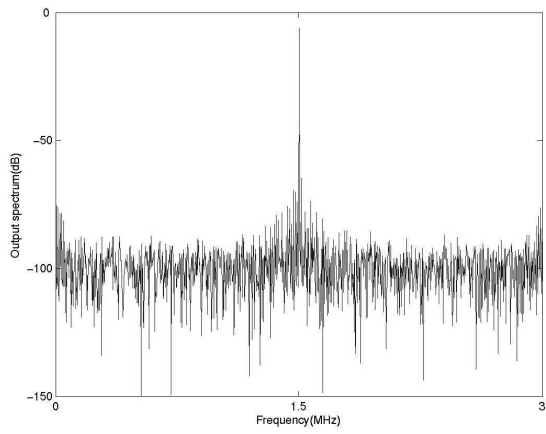Fig. 4. Conventional vs. proposed clock scheme SNDR plot of 10bit algorithmic ADC

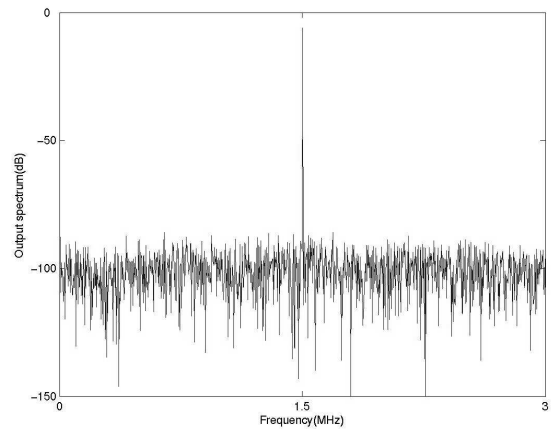(a) F$_{IN}$=1.75MHz, F$_S$=7MHz

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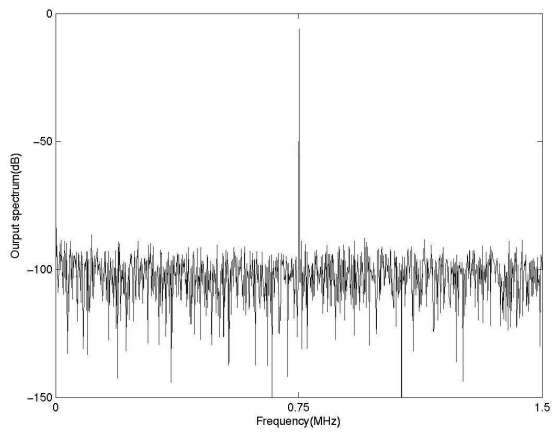
(c) F$_{IN}$=0.75MHz, F$_S$=3MHz
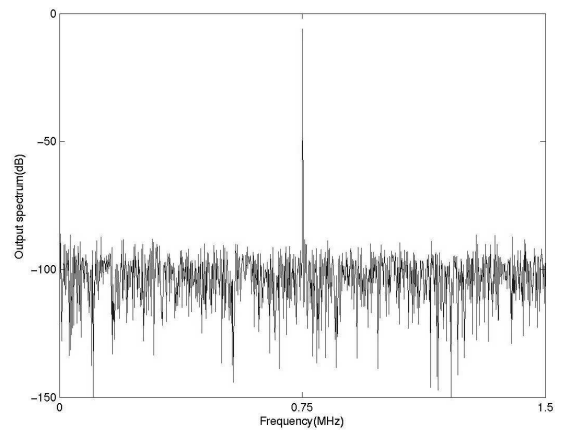
(c) F$_{IN}$=0.75MHz, F$_S$=3MHz

Fig. 5. FFT plots of algorithmic ADC with conventional clocking scheme.

Fig. 6. FFT plots of algorithmic ADC with new clocking scheme.