A TUNABLE DUTY-CYCLE-CONTROLLED SWITCHED-R-MOSFET-C CMOS FILTER FOR LOW-VOLTAGE AND HIGH-LINEARITY APPLICATIONS

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ABSTRACT

A switched-R-MOSFET-C filter with tunable corner frequency is described. The tunability is achieved by varying the clock duty cycle using an automatic tuning circuit. This tuning method does not involve a change in any gate voltage, and is therefore particularly suitable for low-voltage and high-linearity applications. The advantages of the proposed method are illustrated with the design and simulation of a high-Q biquad filter.

1. INTRODUCTION

One important trend of modern integrated circuit (IC) design is the fast downscaling of transistor dimensions, which brings two important problems. First, circuits are required to operate in very low supply-voltage environments. As a result, it becomes necessary to develop new circuit architectures and to improve many existing ones to keep the performance comparable to that achieved with higher supply voltages [1]. One particular example is the floating switches in the signal path of a switched-capacitor (SC) filter. The floating switches see the full-signal swing and may not operate properly for low gate voltages. Special techniques may be required to solve this problem [2]. Second, it is more difficult to achieve good matching of physical elements, which in turn affects the accuracy of circuits that rely on element sizes and ratios.

One critical issue with continuous-time filters is the RC time-constant variation problem, which is typically compensated by some tunable elements. The main drawback in these tunable elements is their inherent nonlinearity, which can be suppressed significantly using a R-MOSFET-C input branch [3]. Automatic tuning of the gate voltage may be used to counteract this variation, but the tuning range may be limited when the supply voltage is low. Tsividis *et al.* reported a signal processing technique that relies on variable timing rather than variable voltages [4], [5], [6] to adjust the time constants. The transistors were turned on and off using programmable pulses, the duty cycles of which determined the transfer function coefficients.

In this paper, a high-Q biquad filter is proposed with highly linear performance even for low-voltage applications. The RC time constant is kept stable by tuning the duty cycle of the clock of the filter automatically, using a switched-capacitor branch as a reference. Simulation results show that the corner frequency can be accurately controlled by changing the clock's duty cycle. There is a great potential for this technique in low-voltage applications, since the tuning does not require changing the magnitude of the gate voltages, and does not affect the linearity significantly.

The paper is organized as follows. Section 2 describes the principle of operation of the proposed technique. Section 3 describes the duty-cycle tuning scheme. Section 4 shows how the proposed technique can be used to design a high-Q biquad section. Section 5 describes simulation results, followed by concluding remarks in Section 6.

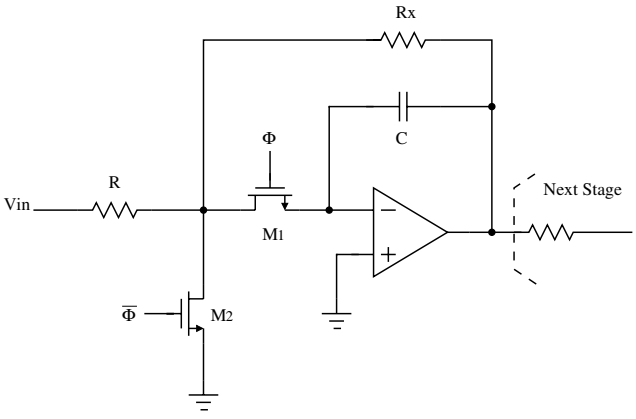

Fig. 1. A first-order filter with switched R-MOSFET-C input branch.

2. OPERATION FUNDAMENTALS FOR THE PROPOSED TECHNIQUE

The basic principle of operation can be illustrated using a first-order filter, shown in Figure 1.

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When the duty cycle of Φ is changed, the time available for the input signal V_{in} to charge C is also changed. Consequently, a multiplication factor relying on the duty cycle of Φ can be realized, which will in turn affect the transfer function [4]. The input MOSFET transitor M1 mainly functions as a switch. The resistor R in series with M1 will help to improve the linearity significantly, since most of the input voltage is dropped across the linear resistor. Including M1 in the feedback loop will further increase the linearity [3]. There are no floating switches in the circuit, and all terminal-to-terminal voltages are smaller than V_{DD} at all times. Therefore, the proposed configuration is suitable for low-voltage applications.

3. AUTOMATIC DUTY-CYCLE TUNING SCHEME

The automatic duty-cycle-tuning scheme uses a configuration containing a switched-capacitor circuit with an accurate time constant C_2/f_cC_1 as a reference for the rest of the

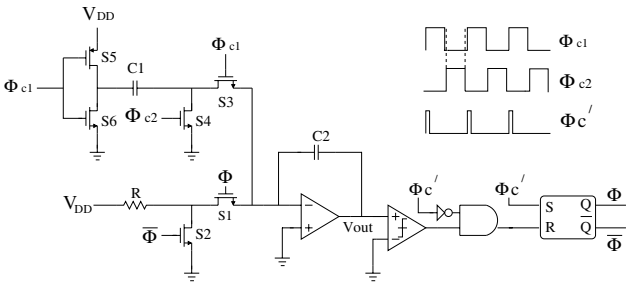

Fig. 2. Clock duty-cycle tuning scheme.

circuit (Figure 2). The resistive branch uses similar components to that of the main circuit. The switched-capacitor path to V_{out} is non-inverting, and it is controlled by a fixed clock, while the resistive path is inverting, and controlled by the variable duty-cycle clock. Both paths are providing currents to the integrator in opposite polarities. Therefore V_{out} will be driven positive if the switched-capacitor branch provides more current, and negative if the resistive branch provides more current. The balance will be achieved by tuning the duty cycles of Φ and $\overline{\Phi}$ based on V_{out}. A comparator is used to compare V_{out} with zero.

The variable duty-cycle clock phases Φ and $\overline{\Phi}$ are created by an SR latch. It starts with a SET pulse (Φ_c' in Figure 2) obtained from the master clock, and stops with a RESET pulse which is provided by the comparator. The SET pulse is made very narrow because its width determines the minimum duty cycle.

4. HIGH-Q BIQUAD FILTER DESIGN

A differential high-Q biquad filter was designed at transistor-level for the TSMC 0.18 μm process and simulated using Spectre. (Figure 3). The filter has a target corner frequency

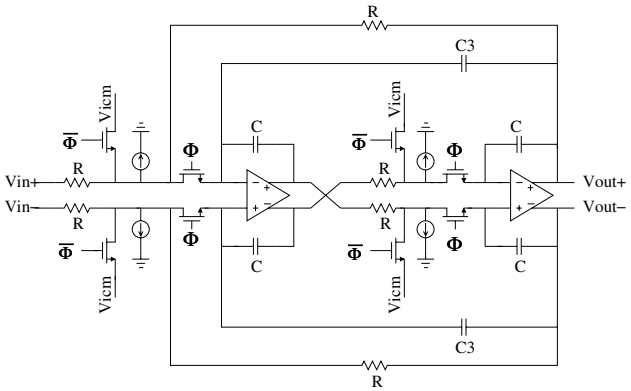

Fig. 3. Designed differential high-Q biquad filter

of 100 kHz, a Q-factor of 4, and the clock frequency runs at 10 MHz. The filter operates from a 1-V supply voltage. Identical current sources were introduced between the opamp inputs and the ground to bias the opamp input common-mode voltage near ground [7]. This biasing not only ensures there is no floating switch in the circuit, but also helps with the operation of the differential folded-cascode opamp which contains a PMOS pair in the input stage (Figure 4). The common-mode feedback (CMFB) used in this opamp design has notably simple configuration and is suitable for the low-voltage application. A simple approach was also taken for the comparator design, which consists a single-stage opamp and two inverters (Figure 5). The clock phases Φ and $\overline{\Phi}$ are generated from the tuning circuit similar to that shown in Figure 2.

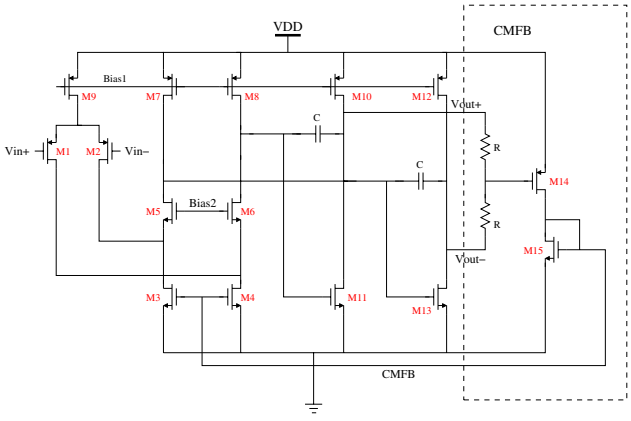

Fig. 4. Transistor-level opamp design

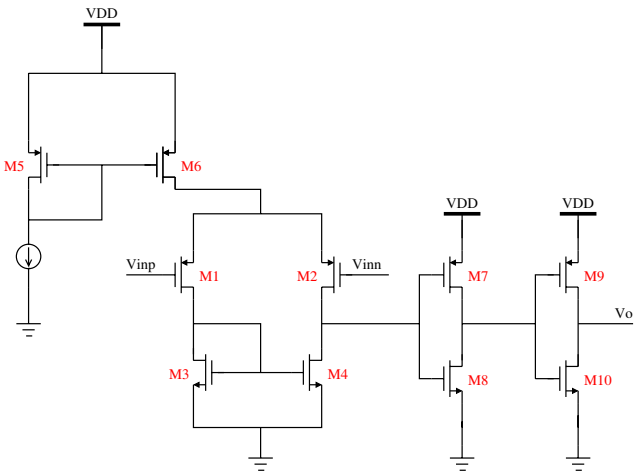

Fig. 5. Transistor-level comparator design

5. SIMULATION RESULTS

Due to the discrete-time nature of this filter, lengthy transient analyses would be required to obtain a frequency response. Instead, in this study, the "Periodic AC Analysis" (PAC) method [8] was used to find the frequency response . Transient analysis results were found to agree with the PAC analysis results.

5.1. Frequency response

The corner frequency of the biquad filter is tunable by changing the equivalent RC constant of the switched capacitor path (Figure 6). The curves show the frequency responses

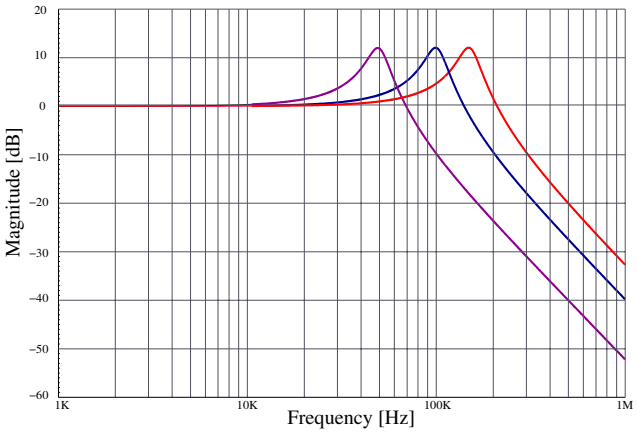

Fig. 6. Frequency responses of the biquad filter.

of the biquad filter for three different values of the reference time constant in the tuning circuit. The value of the capacitor C_1 in the reference branch was set to 120 fF, 240 fF, and 360 fF. The tuning circuit adjusted the clock duty cycle to 25%, 50%, and 75% respectively. The corresponding corner frequencies of the biquad filter are 50 kHz, 100 kHz and 150 kHz.

5.2. Harmonic distortion

For a conventional MOSFET-C filter, a total harmonic distortion (THD) of 40 to 60 dB is achievable. In the proposed filter, as illustrated in Figure 7, the simulated THD was -96.5 dB with the largest harmonics below -110 dB for a V_{in} (p-p differential) value of 400 mV. The filter has high linearity across a wide input range (Figure 8). For V_{in} (p-p differential) value up to 1 V, the THD was better than -78 dB (Figure 8), which is very good for a 1-V supply voltage. These values illustrate the potential that this tuning technique has for high linearity.

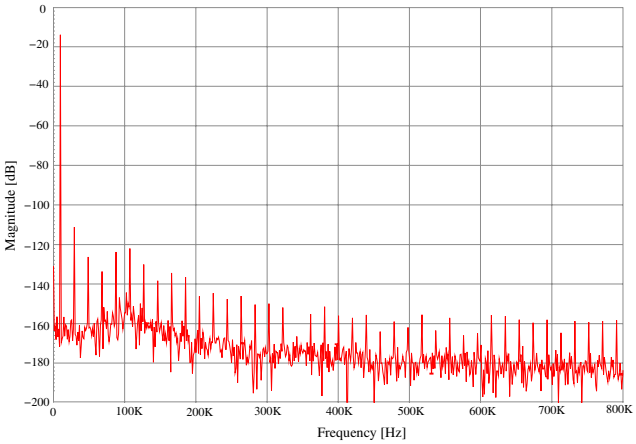

Fig. 7. FFT of the biquad filter output with a 9.7656-kHz signal frequency.

One of the reasons for high linearity in this circuit is that the switch in the input branch is included in the opamp feedback loop, which will suppress the nonlinear effects from this switch [3]. This surpression effect gets weaker with input frequency, so the filter linearity should decrease when the input frequncy increases. This can be demonstrated by analyzing the intermodulation (IMD) of the filter using a two-tone test (Figure 9).

5.3. Automatic Tunability

Figure 10 illustrates the time-domain operation of the tuning circuit. The capacitance in the reference branch was changed from 120 fF to 360 fF at 500 ns, corresponding to a change in the clock duty cycle from 25% to 75%. The circuit takes only one clock cycle to lock to the new time constant.

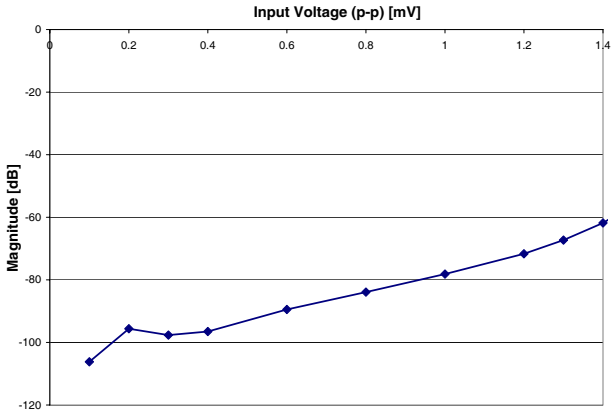

Fig. 8. THD vs. input voltage (V_{in} p-p differential)

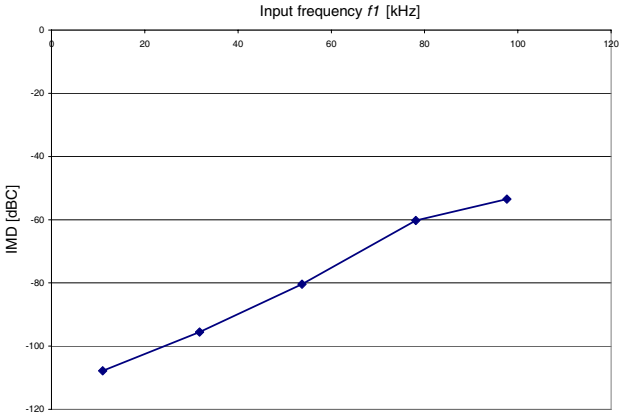

Fig. 9. IMD vs. input frequency

6. CONCLUSIONS

A switched-R-MOSFET-C filter with tunable corner frequency was described. The proposed automatic tuning circuit can rapidly lock the clock duty cycle to a reference time constant. It was shown that distortion levels better than -95 dB can be achieved for a high-Q biquad filter operating from a 1-V supply.

7. REFERENCES

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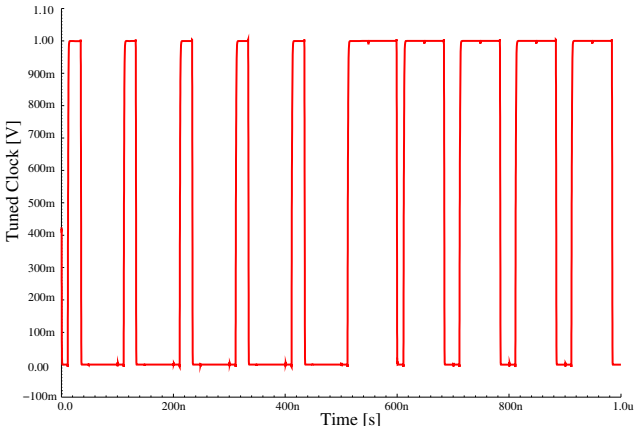

Fig. 10. Automatic clock duty-cycle tuning.

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