JITTER IN HIGH-SPEED SERIAL AND PARALLEL LINKS

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ABSTRACT

Jitter degrades the performance of both high-speed serial and parallel I/O links by limiting the maximum achievable data-rates. We present analytical expressions to evaluate the effect of jitter on the performance of high-speed links. These expressions enable simple calculation of worst-case voltage and timing margins in the presence of jitter. This analysis is also extended to equalized links. Finally, we show that the limited bandwidth of the channel can amplify high frequency jitter and present means to counteract jitter amplification.

1. INTRODUCTION

Recent uninhibited growth in the semiconductor technology led to aggressive scaling of transistors. This aggressive scaling pushed on-chip processing speeds into the multi-gigahertz range. However, off-chip (I/O) bandwidth has not scaled as aggressively. As a result, the performance of large digital systems based on high-speed chip-to-chip communication is limited by the I/O bandwidth. Also, as increasing data rates follow technology scaling, limited timing accuracy that is bounded by the unavoidable use of phase/delay locked loops can significantly degrade link performance. In a truly serial communication, the data and the clock are sent in a single serial stream. The receiver extracts the clock from the serial data stream using a clock and data recovery (CDR) system. We refer to this type of clocking as embedded-clocking. However, in the case of parallel links bundled-timing is employed in which a clock channel is shared among a number of data channels. Simple per-pin skew compensation is performed using delay locked loop (DLL) to account for channel mismatch between the data and the clock. We refer to this type of clocking as source-synchronous clocking. Both of these clocking schemes suffer from clock jitter which degrades the link performance. Link performance is typically measured in bit error rate (BER), however, verifying small BER requires very long simulation time. In order to estimate link performance without resorting to long simulation we present an analytical model to model the effect of jitter in both serial and parallel links.

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2. MODELING JITTER IN SERIAL LINKS

A generalized model of a serial link is shown in Fig. 1. A

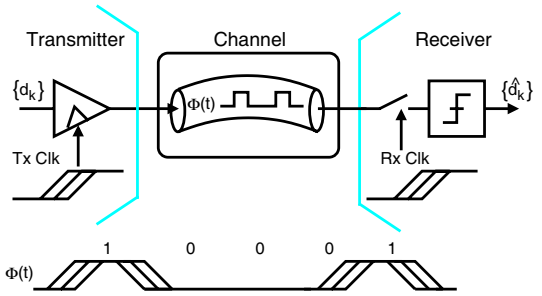

Fig. 1. Simplified block diagram of a serial link.

typical serial link consists of a transmitter which generates a train of pulses depending on the data symbols to be transmitted, and the pulse width is determined by the timing instant of the transmit clock at both begin/end edges. The receiver is generally a sampler followed by a decision circuit (e.g. high gain comparator). Even though other receiver architectures based on an integrating amplifier or sense amplifier exist, sampler type receivers are used primarily due to their high speed advantage [2] in multi-gigabit links. Communication channels for serial links are typically printed circuit board (PCB) traces or coaxial cables. While loss mechanisms can differ somewhat, linear and time-invariant approximations are valid for most physically realizable channels. Therefore, we characterize a channel by its impulse response. Non-return-to-zero (NRZ) pulses are commonly used as the basis function for discrete data transmission. Our analysis and discussions in this paper are formulated in the context of a two-level (single-bit-per-symbol) NRZ

transceiver system, as this is the most common modulation scheme used in serial links today. Some recent implementations employ four-level NRZ signaling (i.e. PAM-4) which doubles the bits-per-symbol rate. While our analysis and conclusions can easily be transferred to this and a variety of other signaling systems, we stay with the common two-level (binary) NRZ signaling scheme to focus our investigations on how PLL jitter impacts transceiver performance.

The transmitted bits can be denoted by an independent and identically distributed (i.i.d.) sequence $\{d_k\}$. The transmitter produces an output pulse corresponding to data bit d_k and variation in the pulse width is determined by the transmitter clock jitter generated by a PLL. The transmitted pulse train, $\phi(t)$, with jitter-free transmit clock can be written as [3]

$$\phi(t) = \sum_{k=-\infty}^{\infty} (d[kT] - d[kT-T]) \cdot u(t-kT)\,, \qquad (1)$$

where T is equal to the bit period and $u(t)$ is the unit step function such that $u(t) = 0$ for $t \leq 0$ and $u(t) = 1$ for $t > 0$. As mentioned earlier, the channel can be accurately characterized by an impulse response $h(t)$. The output of the channel, y(t), can be evaluated by convolving the input pulse train with the channel impulse response $h(t)$

$$\begin{aligned} y(t) &= \left[\sum_{k=-\infty}^{\infty} (d[kT] - d[kT-T]) \cdot u(t-kT)\right] \otimes h(t) \\ &= \sum_{k=-\infty}^{\infty} \left[(d[kT] - d[kT-T]) \cdot s(t-kT)\right]\,, \qquad (2) \end{aligned}$$

where $s(t) = u(t) \otimes h(t)$ is the step response of the channel. In this equation, the sampling instant kT determines the pulse width of the k^{th} transmitted data pulse/bit. The jitter in the transmitter can be included in the above equation by defining a jitter sequence $\{j_{tx}\}$ such that $j_{tx}[k]$ is the jitter associated with the k^{th} clock edge:

$$\begin{aligned} y(t) &= \left[\sum_{k=-\infty}^{\infty} (a[kT]) \cdot u(t-kT+j_{tx}[kT])\right] \otimes h(t) \\ &= \sum_{k=-\infty}^{\infty} \left[(a[kT]) \cdot s(t-kT+j_{tx}[kT])\right]\,. \qquad (3) \end{aligned}$$

where transition sequence $a[n] = d[n] - d[n-1]$. A clock-data recovery circuit locked to the serial data stream generates a receiver clock phase that is aligned with the incoming data such that the voltage margin is maximized at the input of the detector. But due to various noise sources (intrinsic device and power supply noise), the receiver clock has jitter associated with each of its edges. This jitter is denoted by the jitter sequence $\{j_{rx}\}$ such that $j_{rx}[n]$ is the jitter associated with the n^{th} sampling edge. The sampled channel output using the jittered receive clock can be written as

$$\begin{aligned} y(nT) = \sum_{k=-\infty}^{\infty} [(a[kT]) \cdot s(nT - kT \\ + j_{rx}[nT] + j_{tx}[kT])]\,. \qquad (4) \end{aligned}$$

The approximate solution for both the transmitter and receiver jitter can be derived using first order Taylor series expansion of the step response.

2.1. Taylor Series Approximation

We can approximate the step response using first-order Taylor series approximation for two variables (i.e. when $j_{tx}[k] \ll T$ and $j_{rx}[k] \ll T$) as follows:

$$\begin{aligned} s(nT - kT + j_{rx}[nT] + j_{tx}[kT]) \approx s(nT - kT) \\ + j_{rx}[nT] \cdot \left.\frac{ds(t)}{dt}\right|_{t=nT-kT} - j_{tx}[kT] \cdot \left.\frac{ds(t)}{dt}\right|_{t=nT-kT} \\ = s(nT - kT) \\ + j_{rx}[nT] \cdot h(nT - kT) + j_{tx}[kT] \cdot h(nT - kT)\,. \qquad (5) \end{aligned}$$

Putting Eqs. (4) and (5) together, we can write the channel output as

$$\begin{aligned} y[n] \approx a[n] \otimes s[n] + (a[n] \otimes h[n]) \cdot j_{rx}[n] \\ + (a[n] \cdot j_{tx}[n]) \otimes h[n]\,. \qquad (6) \end{aligned}$$

In the above equation, the first term $a[n] \otimes s[n]$, is the channel output when both the transmitter and recovered clocks are jitter-free. The second and third convolution terms represent the voltage margin degradation due to recovered and transmitted clocks respectively. The first order jitter model can be represented in a block diagram as shown in Fig. 2. Note that this model enables to evaluate the effect of the

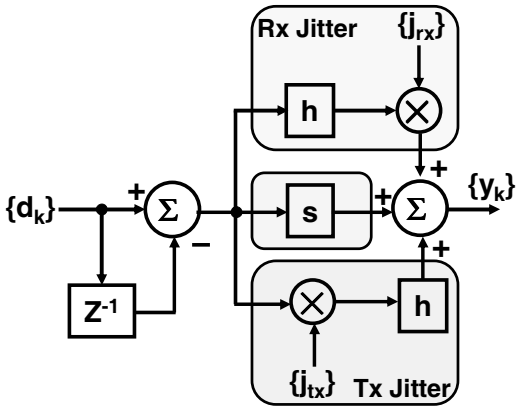

Fig. 2. Transmitter and Receiver Jitter Model.

transmitter and receiver jitter independently. This explicit separation enables us to evaluate the worst case or peak distortion due to jitter without performing prohibitively long time-domain simulations.

3. MODELING JITTER IN SOURCE-SYNCHRONOUS LINKS

A generalized model of a source synchronous link is shown in Fig. 3. A dedicated clock channel is used to send the

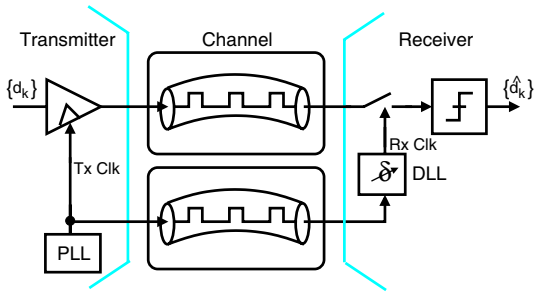

Fig. 3. Source Synchronous Link Model.

clock along with the data. The timing-recovery at the receiver consists of a variable delay element, for example, a delay locked loop (DLL), which adjusts the phase of the receive clock to maximize voltage/timing margins. One major advantage of a source synchronous link is that the phase adjustment can be done at power-up. Since the data and clock go through nominally identical paths the receive clock ideally tracks the data automatically. Similar to the embedded-clocking case, the transmitter and receiver jitter can be modeled using Eq. (6). However, in the case of source-synchronous clocking, the receiver jitter sequence j_{rx} is correlated to the transmitter jitter sequence j_{tx}.

Even though source-synchronous clocking scheme has excellent tracking ability, it suffers from two major limitations in links operating at multi-gigabit range over lossy channels. First, duty cycle error in the transmitted clock will result in time-varying common-mode shift, potentially resulting in the loss of receiver clock. Second, transmitter jitter can be potentially amplified due to limited bandwidth of the channel. This effect is shown in Fig. 4. Note that jitter amplification increases dramatically with higher data-rates. This indicates that source-synchronous interfaces will be extremely difficult to implement for multi-gigabit data-rates. Even though jitter amplification can be reduced by sending reduced frequency clock (quarter-rate or slower), a multiplying PLL or a multi-phase receiver is required both of which reduce the correlation between the data and the receiver clock and hence degrading the performance of the link.

4. BEHAVIORAL SIMULATIONS

The analysis presented thus far is verified using behavioral simulations in MATLAB. The channel model used is a 20″ FR4 trace with two connectors. The impulse response is

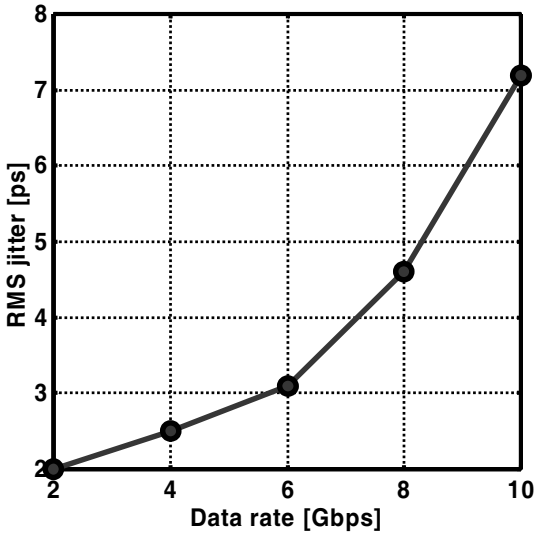

Fig. 4. Jitter amplification in source-synchronous links. The channel is 20” FR4 with 2 connectors. Receiver clock jitter is measured by transmitting a clock with 2ps RMS jitter.

derived from measured differential scattering parameters. The transmitter and receiver bandwidths are modeled using single pole transfer functions. Figures 5 and 6 illustrate the eye diagrams in the presence of 5ps RMS receiver sampling jitter. Fig. 5 is the “calculated” eye diagram, by which we mean the eye generated using Eq. (6) for a data stream length of 2000 data bits. On the other hand, the simulated eye diagram shown in Fig. 6 is generated using the same data and jitter sequence in a *time-domain*[1] simulation. The calculated and simulated eye diagrams are overlayed in order to compare them in Fig. 7. Note that the simulated and calculated eye diagrams are virtually identical, confirming that the error in the first-order Taylor series approximation is acceptable. One application of this analytical model is that it facilitates the calculation of worst case noise margin degradation. For example, Fig. 8 illustrates the worst case [2] for various jitter conditions.

5. CONCLUSION

We presented an analytical model to incorporate both transmitter and receiver jitter into both embedded clocking and source-synchronous clocking schemes. Based on linear time-invariant approximation, this model permits fast and accu-

[1] In a time-domain simulation the data sequence is convolved with the impulse response and the output is sampled appropriately to maximize the voltage margin. Jitter is incorporated by randomly varying the optimal sampling point.

[2] Worst case eye due to ISI alone is calculated [1] and the voltage noise due to jitter is subtracted from it to arrive at the worst case eye in the presence of jitter

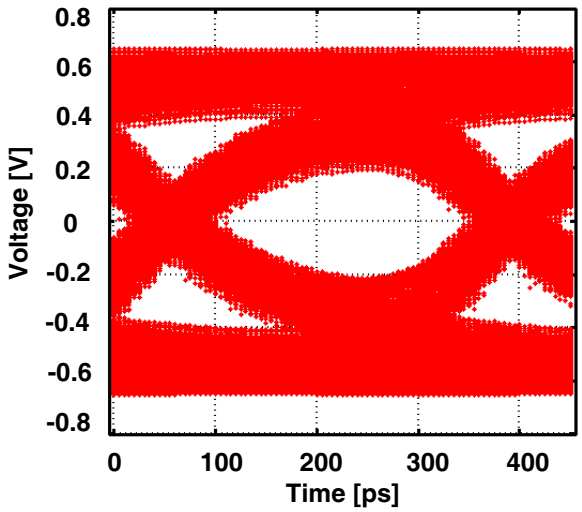

Fig. 5. Calculated eye diagram.

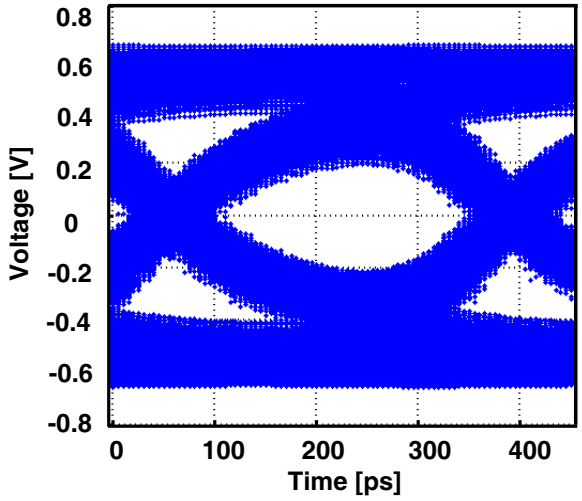

Fig. 6. Simulated eye diagram with 2000 random bits.

rate evaluation of worst case margins, thus obviating the need for prohibitively long time-domain simulations.

6. REFERENCES

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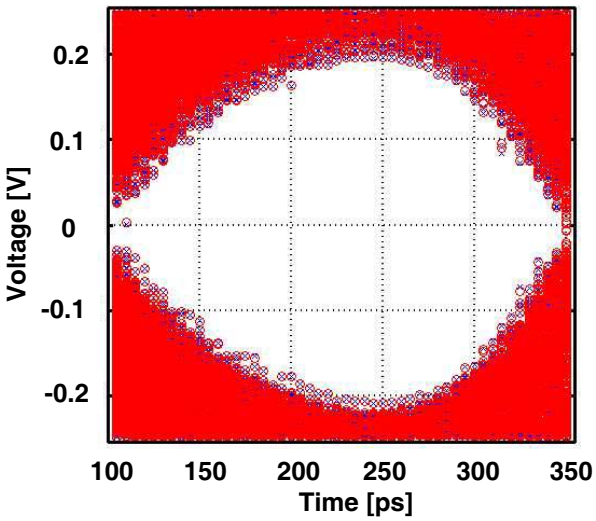

Fig. 7. Calculated (marker 'o') and simulated (marker 'x') eye diagrams with 2000 data bits.

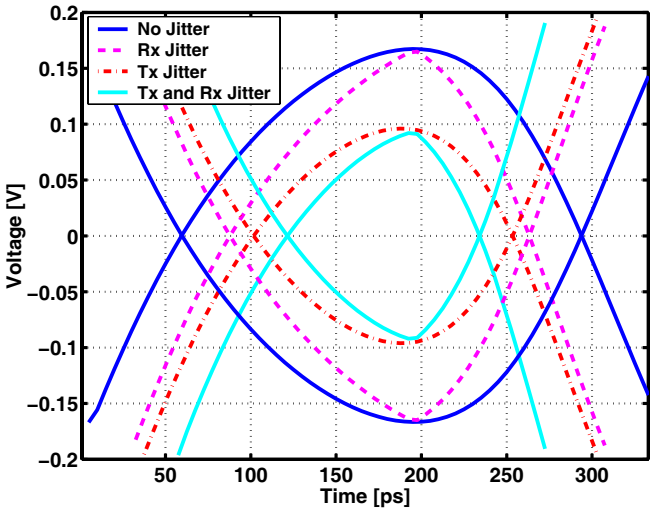

Fig. 8. Comparison of the effect of transmitter (Tx) and receiver (Rx) jitter on the worst-case ISI eye. 7σ peak transmitter jitter and 7σ peak receiver sampling jitter is assumed.