A Low Spur Fractional-N Frequency Synthesizer Architecture

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***Abstract*— A new architecture of a fractional-N phase-locked loop (PLL) frequency synthesizer is presented in this paper. The unique feature of the proposed frequency synthesizer is a loop filter with a discrete time comb filter which allows for the efficient suppression of fractional spurs. The proposed loop filter architecture can be efficiently implemented using switched capacitor techniques. The benefits of this approach are a low power frequency synthesizer design with low spur levels. An analysis of the fractional spurs in the fractional-N frequency synthesizers is also presented.**

I. Introduction

Fractional-N type of PLL's are commonly used in frequency synthesizers. A fractional-N PLL has benefits compared with classical integer-N implementations. Better phase noise performance, faster lock, and better spur levels can be obtained with fractional-N PLLs. The advantages of fractional-N PLLs come from a larger loop bandwidth which implies better voltage controlled oscillator (VCO) phase noise suppression and faster lock time, and from higher phase-frequency detector (PFD) update frequencies. However, fractional-N implementations have pitfalls as well, which are the fractional spurs and cycle slipping.

Fractional spurs can be eliminated by removing the deterministic nature of switching among different division ratios. This is commonly done by introducing delta-sigma control in the feedback divider [1]. In this case, fractional spurs are spread over the spectrum and become quantization noise which is shaped by the delta-sigma modulator to high frequencies. High frequency noise is filtered by the low pass characteristics of the loop filter. In order to obtain efficient filtering of the high pass shaped noise, the order of the loop filter must be equal to the order of the delta-sigma modulator plus one. This approach is efficient but might not lead to complete elimination of spurs, since a delta-sigma modulator can generate spurs by itself due to idle tones. To reduce idle tones, pseudorandom sequences can be mixed with the delta-sigma modulator input.

Thus the delta-sigma approach incorporates additional hardware for an all-digital delta-sigma modulator, pseudorandom sequence generator, and more complex loop filter. More hardware will lead to a higher power consumption, larger chip area and, in the case of additional digital blocks, to more switching noise which can be coupled through the common substrate and supply to analog blocks and degrade their performance [2].

Another way to suppress fractional spurs is to reduce the bandwidth of the PLL, but this results in a degradation of the noise performance and an increased of the lock time.

The approach proposed in this paper is an extension of the conventional fractional-N technique and incorporates a discrete-time loop filter with notches at spur frequencies. Notch frequencies can be programmable and depend on the fractional spurs. The benefits of this approach are a low power frequency synthesizer design with low spur levels. Also in our approach, the bandwidth of the PLL can be kept as large as permitted by the stability criteria.

II. Fractional spurs

Fractional-N frequency synthesizers generate spurs at the output of VCO. The nature of the spurs depends on a programmable feedback divider which can switch between two different integer division ratios in order to get a fractional one [3]. Assume a feedback divider can divide by N or $N+1$, the division modulus is M, and the reference frequency is f_{ref}. If a division by $N+1$ is chosen K times and a division by N is chosen $M-K$ times, the fractional division ratio N_f will be given by:

$$N_f = \frac{K \cdot (N+1) + (M-K) \cdot N}{M} = N + \frac{K}{M} \qquad (1)$$

It is clear that the frequency resolution is f_{ref}/M and the first harmonic frequency at the PLL control line is $f_{ref} \cdot K/M$. The control voltage harmonic content affects the VCO output voltage spectrum. In order to understand which harmonics at the control line are needed to be blocked, an analysis should be performed to determine how severely they affect the spectrum of a VCO.

Assume that the VCO control voltage is given by Eq. (2) which is a truncated Fourier series expansion:

$$V_{ctrl}(t) = V_0 + V_1 \cos(\omega_s t + \varphi_1) + V_2 \cos(2\omega_s t + \varphi_2) \quad (2)$$

where $\omega_s = 2\pi f_s$;
f_s - frequency of a spur;
V_i - amplitude of the i-th harmonic;
φ_i - phase of the i-th harmonic, which can be neglected for simplifying the derivations.

The output voltage of the VCO is given by:

$$V_{VCO}(t) = V_A \cos(\omega_0 t + \Phi(t)) \qquad (3)$$

where $\omega_0 = 2\pi f_0$;
f_0 - frequency of the free running oscillator;
V_A - amplitude of oscillation;
$\Phi(t)$ - phase of the oscillator.

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The phase of the oscillator can be calculated using Eq. (4)

$$\begin{aligned}\Phi(t) &= 2\pi K_{VCO}\int_{-\infty}^{t} V_{ctrl}(t)dt \\ &= 2\pi K_{VCO}(V_0 + \frac{V_1}{\omega_s}\sin(\omega_s t) \\ &\quad + \frac{V_2}{2\omega_s}\sin(\omega_s t)) \end{aligned} \quad (4)$$

Define:

$$\begin{aligned}\alpha_1 &= 2\pi K_{VCO}\frac{V_1}{\omega_s} = V_1\frac{K_{VCO}}{f_s} \\ \alpha_2 &= 2\pi K_{VCO}\frac{V_2}{2\omega_s} = V_2\frac{K_{VCO}}{2f_s} \end{aligned} \quad (5)$$

Using the above definitions, the output voltage of the voltage controlled oscillator can be written as:

$$\begin{aligned}V_{VCO}(t) &= V_A\cos(2\pi(f_0 + K_{VCO}V_0)t \\ &\quad + \alpha_1\sin(\omega_s t) + \alpha_2\sin(2\omega_s t)) \\ &= V_A\cos(\omega_c t + \alpha_1\sin(\omega_s t) \\ &\quad + \alpha_2\sin(2\omega_s t)) \end{aligned} \quad (6)$$

where $\omega_c = 2\pi f_c = 2\pi(f_0 + K_{VCO}V_0)$.

$V_{VCO}(t)$ can be represented as:

$$\begin{aligned}V_{VCO}(t) &= V_A\Re\{e^{j\omega_c t}e^{j\alpha_1\sin(\omega_s t)}e^{j\alpha_2\sin(2\omega_s t)}\} \\ &= V_A\Re\{e^{j\omega_c t}\sum_{n=-\infty}^{\infty} J_n(\alpha_1)e^{jn\omega_s t} \\ &\quad \cdot \sum_{m=-\infty}^{\infty} J_m(\alpha_2)e^{jm2\omega_s t}\} \\ &= V_A\sum_{n=-\infty}^{\infty}\sum_{m=-\infty}^{\infty} J_n(\alpha_1)J_m(\alpha_2) \\ &\quad \cdot\cos(\omega_c t + n\omega_s t + m2\omega_s t) \\ &= V_A\sum_{n=-\infty}^{\infty}\sum_{m=-\infty}^{\infty} J_n(\alpha_1)J_m(\alpha_2) \\ &\quad \cdot\cos(\omega_c t + (n+2m)\omega_s t) \end{aligned} \quad (7)$$

where $J_i(\cdot)$ is the i-th order Bessel function of the first kind (Figure 1).

The magnitude of each spur harmonic in the output voltage of a VCO can be determined from Eq. (7) simply by combining coefficients near a desired frequency. Define k as the number of the desired spur harmonic, then $k = n + 2m$, and $n = k - 2m$. The magnitude of the k-th spur harmonic V_{sk} is defined by Eq. (8):

$$V_{sk} = \sum_{m=-\infty}^{\infty} J_{k-m}(\alpha_1)J_m(\alpha_2) \quad (8)$$

Form Eqs. (7) and (8) it can be concluded that:

- each harmonic at the control line of a VCO will generate an infinite number of spurs at multiple frequencies around the carrier frequency of the VCO;
- the magnitude of a spur depends on the arguments of the Bessel functions (or modulation index), and thus depends on the K_{VCO} and the magnitude and the frequency of a harmonic at the control line;

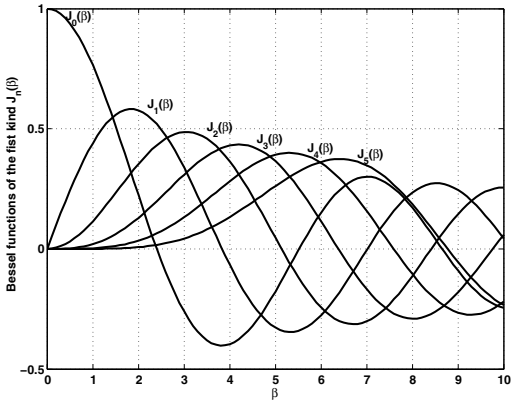

Fig. 1. Bessel functions of the first kind.

Therefore, a low K_{VCO} should be used and the fractional spurs should be moved to a higher frequency.

III. Blocking of the fractional spurs

The previous analysis shows that a number of harmonics at the control line have to be blocked in order to eliminate spurs at the VCO output. The blocking can be done by introducing notches at the spur frequencies on the PLL control line.

A conventional fractional-N PLL is shown in the Figure 2. The phase-frequency detector (PFD) together with the charge pump (CP) is basically a discrete-time block with sampling frequency equal to the PLL update rate. The phase error information is present in current pulses injected from the CP into the low pass filter (LPF). Since the absolute value of the CP current has to remain constant, the phase error information is stored in the width of the current pulses or in the amount of charge injected into the LPF. The key idea of the proposed spur blocking technique is to introduce switched capacitor discrete-time comb filters (DTF) to process charge injected from the CP before it reaches the LPF (Figure 3). Operating at the frequency of the PLL update rate, the comb filter places zeros at the frequency of the fractional spurs and thus filters them out.

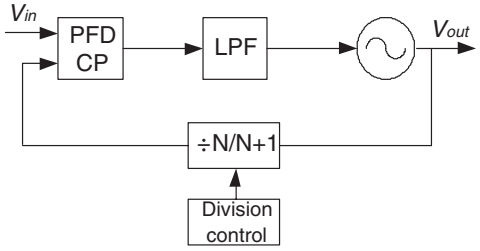

Fig. 2. Conventional fractional-N PLL.

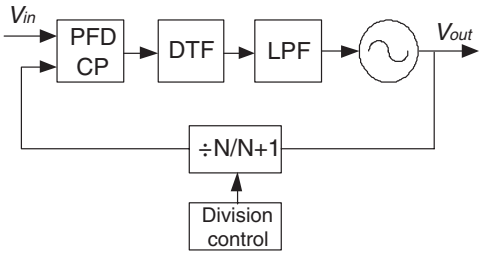

Fig. 3. PLL architecture with a discrete-time comb filter.

Generally, PLL analysis in the z-domain is more accurate because of the sampling nature of the PLL system. The z-domain analysis takes into account such effects as the discrete time phase-frequency comparison in the PFD, the folding and the delay through the loop [4], [5].

The two PLLs from Figures 2 and 3, a conventional PLL, and one with a discrete-time comb filter, have been modeled in Matlab. The PLLs have a reference frequency of f_{ref}=40MHz and bandwidth equal to 4MHz. For an output with 10MHz steps, the feedback divider should have the modulus M equal to 4. The frequency of the spurs depend on the feedback division ratio and the lowest possible frequency is given by f_{ref}/M and is equal to 10MHz in our case. Thus the comb filter transfer function should have 4 zeros around the unit circle with a 10MHz spacing and is given by:

$$DTF(z) = 1 - z^{-M} \tag{9}$$

where $M = 4$ is the modulus of the fractional-N PLL.

It can be seen that the DTF is a linear phase FIR filter and thus causes 180 degree phase degradation from DC to the first notch (first zero) [6]. To maintain stability of the system, the phase needs to be corrected. To correct the phase, a left half plane (LHP) real value zero-pole pair can be used as a phase correction filter (PCF) as in Eq. (10)

$$PCF(z) = \frac{1 - 0.9z^{-1}}{1 - 0.5z^{-1}} \tag{10}$$

The complete z-domain block diagram of the proposed PLL is presented in Figure 4.

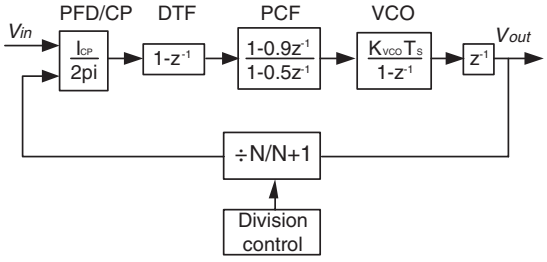

Fig. 4. z-domain block diagram of the PLL with a discrete-time comb filter.

Figure 5 shows the frequency responses of the open loop PLL. The solid line represents the s-domain model for the conventional PLL and the dashed line represents the z-domain model for the same PLL. Since the bandwidth of the PLL is only ten times less than its reference frequency, a difference between the s-domain and the z-domain models can be clearly seen. The dotted line shows the frequency response of the PLL with a discrete time comb filter, which has been designed for the same specifications as the conventional PLL.

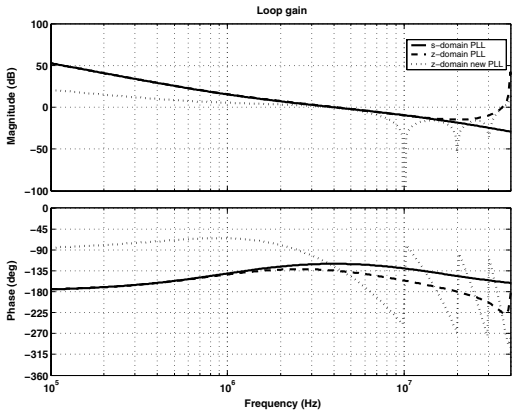

Fig. 5. Loop gain of the PLL.

To prove the robustness of the proposed technique, both PLLs have been simulated in Simulink. For the simulation, the output frequency is chosen to be 1.02GHz, thus the division ratio should be 25.5. In this case, the control voltage spectrum will contain harmonics of $f_s = f_{ref}/2$.

Figure 6 shows the voltage spectrum on the control line of a conventional PLL. As can be seen, the control voltage has several harmonics that cause spurs at the VCO output (Figures 7 and 8).

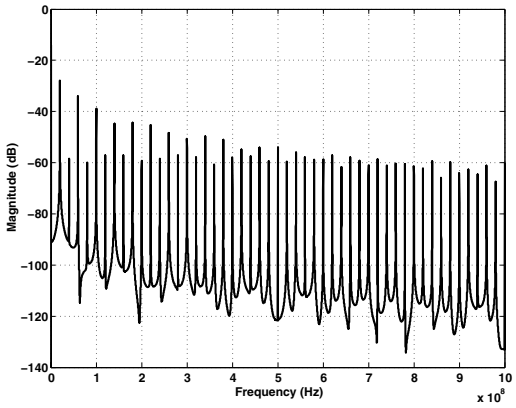

Fig. 6. Control voltage spectrum of the conventional PLL.

Figure 9 shows the voltage spectrum on the control line of a PLL with the DTF. As can be seen, the control voltage is free of harmonics and the VCO output spurs have been eliminated (Figures 10 and 11).

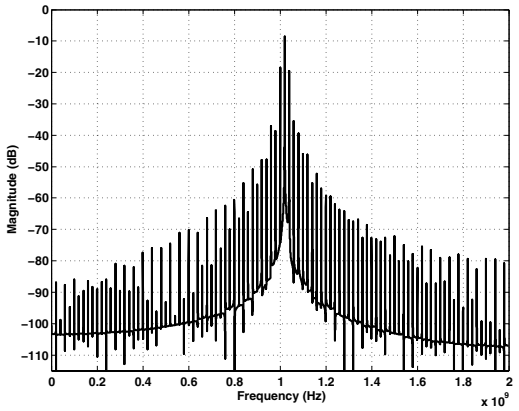

Fig. 7. VCO output spectrum of the conventional PLL.

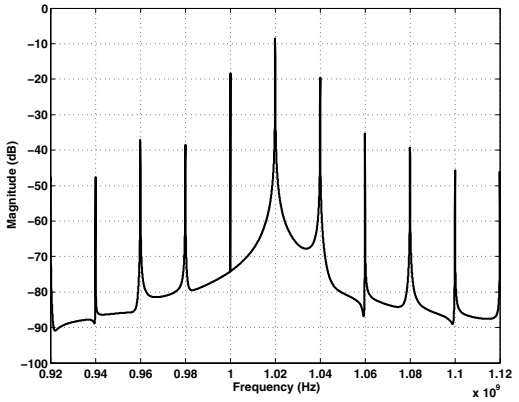

Fig. 8. VCO output spectrum of the conventional PLL (zoomed).

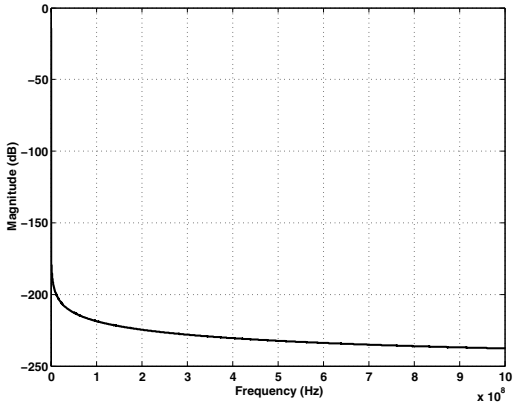

Fig. 9. Control voltage spectrum of the PLL with DTF.

IV. Conclusions

A new approach to the design of fractional-N frequency synthesizers with low fractional spurs is proposed. The key idea is to remove fractional spurs using a discrete-time comb filter, which can be implemented using switched capacitor techniques. Simulation results show that the use of a comb filter creates notches at the harmonic frequencies and eliminates spurs from the VCO output spectrum. The limitation of this approach is that it cannot be used if the spurs occur inside the PLL bandwidth. Also if the spurs are close to the PLL bandwidth, an additional zero might be needed to correct the phase and maintain the required phase margin.

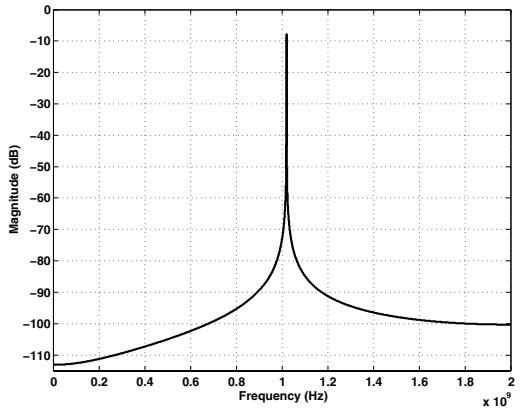

Fig. 10. VCO output spectrum of the PLL with DTF.

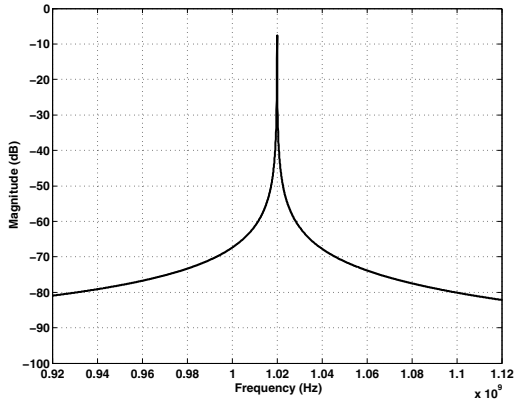

Fig. 11. VCO output spectrum of the PLL with DTF (zoomed).

Acknowledgment

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