CONSTANT TRANSCONDUCTANCE BIAS CIRCUIT WITH AN ON-CHIP RESISTOR

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ABSTRACT

A method to generate stable transconductance (g_m) without using precise external components is presented. The off-chip resistor in a conventional constant-g_m bias circuit is replaced with a variable on-chip resistor. A MOSFET biased in triode region is used as a variable resistor. The resistance of the MOSFET is tuned by a background tuning scheme to achieve the stable transconductance that is immune to process, voltage and temperature variation. The transconductance generated by the constant-g_m bias circuit designed in $0.18\mu m$ CMOS process with $1.5V$ supply displays less than 1% variation for a 20% change in power supply voltage and less than $\pm1.5\%$ variation for a $60°C$ change in temperature. The whole circuit draws approximately $850\mu A$ from a $1.5V$ supply.

I. INTRODUCTION

Constant transconductance (g_m) bias circuits are widely used in many analog integrated circuit applications, such as low-noise amplifiers (LNA) [1] and $G_m - C$ filters [2]. The constant transconductance is converted to a fixed current by using a voltage provided by a band-gap reference. If the transconductance and the reference voltage are process, voltage and temperature (PVT) independent then, naturally, the current generated using these parameters is also PVT independent and hence can be used as a master bias current on a large analog chip. There are several ways of implementing constant-g_m bias circuits. Of them resistor-referred constant-g_m bias circuit shown in Fig. 1 is the most commonly used. Assuming square-law devices and neglecting channel-length modulation and body effect, this bias circuit provides a g_m that is inversely proportional to resistor R. In practice to achieve constant g_m, a precise off-chip resistor is used.
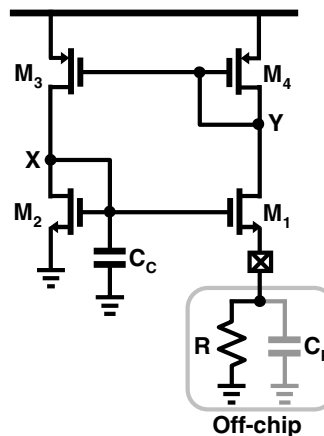

Fig. 1. A simple constant-g_m bias circuit.

This simple implementation has three major drawbacks. First, this circuit is sensitive to power supply variation. In the presence of supply noise, node X and node Y vary differently leading to current variation in the two branches due to channel-length modulation of M_1 and M_2. This leads to g_m variation with changes in supply voltage. Second, the stability is degraded by the large parasitic capacitor C_P associated with the pad and the off-chip resistor. Analysis in [3] shows that a large compensation capacitor C_C of the order of C_P is needed to make the circuit stable. Finally, the need for external components increases the overall cost of the system.

In this paper, we present an alternate constant-g_m bias circuit that uses an on-chip resistor and is less susceptible to power supply variation. We will focus on the tuning scheme that enables the use of an on-chip resistor to obtain constant g_m. This paper is organized as follows. The constant g_m bias circuit is presented in Section II. The tuning scheme used to achieve a constant transconductance with an on-chip resistor is discussed in Section III and the simula-

tion results are presented in Section IV. Finally, the important results are summarized in Section V.

II. CONSTANT G_M BIAS CIRCUIT

The bias circuit used in this design is shown in Fig. 2. The active current mirror formed by M_3 and
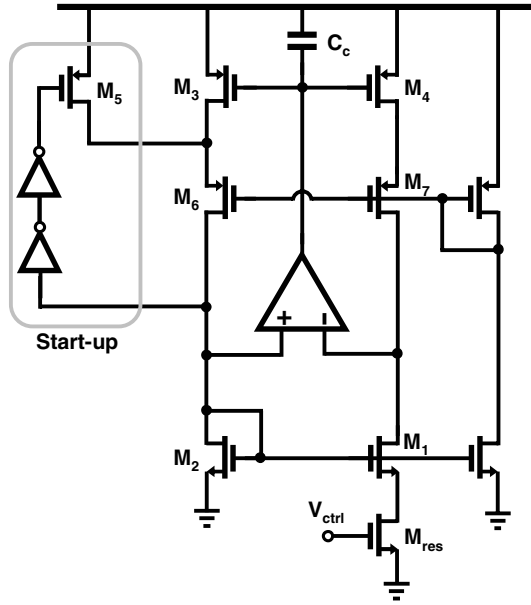

Fig. 2. An improved constant-g_m bias circuit.

M_4 in Fig. 1 is replaced by cascoded current sources (M_3, M_4, M_6 and M_7) and the precise off-chip resistor R is replaced by an on-chip MOS transistor M_{res} biased in triode region. The cascode transistors M_6, M_7 are biased by a separate bias branch, while the current source transistors M_3, M_4 are self-biased using an opamp in negative feedback. Additionally, this feedback forces the drain voltages of M_1, M_2 to be equal thus obviating the need for cascoding M_1 and M_2. The feedback loop is compensated using the capacitor C_c. The power supply noise immunity is improved due to the increased output impedance of the cascoded current sources.

Most of the self-biased circuits are susceptible to the lock-up state. In the bias circuit shown in Fig. 2, the condition in which all the transistors are OFF is a stable state. In order to avoid this undesired state, a simple start-up circuit consisting of two inverters and transistor M_5 is added. In the lock state, M_5 injects a small current into the source of M_6 to start-up the circuit. The inverters are designed to pull-up the gate

of M_5 to V_{DD} thereby disabling the start-up circuit during normal operation.

As mentioned earlier, the off-chip resistor is replaced by a MOS transistor M_{res}. The resistance of a MOS transistor biased in triode region varies by more than $\pm 20\%$ with PVT changes resulting in an unacceptable variation of the transconductance of the bias circuit. In the following section, we present a background tuning scheme that maintains a constant g_m by continuously tuning the ON resistance of M_{res}.

III. TUNING SCHEME

The tuning of a resistor to a specific value is a common problem in many classes of analog circuits. For example, resistors in continuous-time filters are tuned to achieve accurate bandwidth of the filter in the presence of PVT variation [4]. It is very desirable that the tuning be done in background without interrupting the tuned block. Many of such background tuning techniques are based on *master-slave* approach shown in Fig. 3. In this method, a *master* consisting of PVT invariant reference tunes the PVT variant *slave*. For example, in [5] the MOS resistor of the constant-g_m bias circuit (*slave*) is tuned by a phase locked-loop (PLL) (*master*) consisting of g_m locked oscillator. However, this design requires a full PLL resulting in a large area and power overhead. In this paper, we present a simple but effective alternative scheme to tune the resistor.
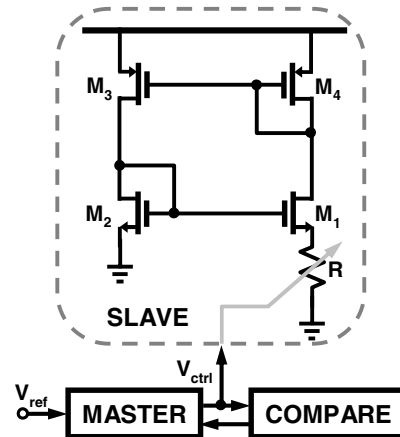

Fig. 3. Concept of master-slave tuning.

The *master* tuning block is shown in Fig. 4 [6] in which a switched-capacitor (SC) resistor is used as the reference element. It consists of an integrator
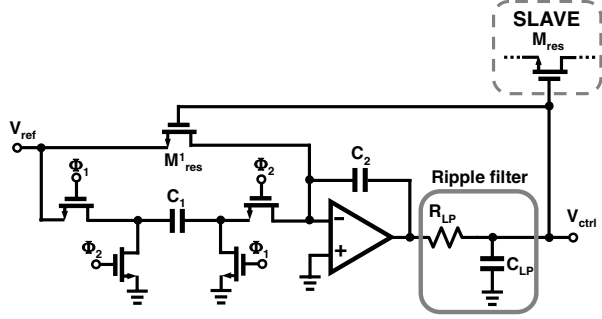
Fig. 4. Time constant matching tuning scheme.

with two separate branches, a replica resistor (M_{res}^1) branch and a SC resistor branch. The negative feedback generates the control voltage (V_{ctrl}) that forces the error current generated due to mismatch between the time constants of the two branches. In other words the following equality is achieved in steady state.

$$R_{M_{res}^1} C_2 = \frac{1}{F_{CK} C_1} C_2 \qquad (1)$$

The ripple-pole filter at the output of the integrator is used to suppress the ripple generated due to the sampling nature of the tuning circuit. Since the clock frequency F_{CK} and the on-chip capacitor ratio $\frac{C_1}{C_2}$ can be defined accurately, this tuning scheme achieves a precise time constant $R_{M_{res}^1} C_2$. Therefore, by matching M_{res}^1 and M_{res} a stable and PVT invariant transconductance can be achieved. Note that the absolute accuracy of the transconductance is limited by the absolute accuracy of the on-chip capacitor C_1.

By driving the gate of the variable resistor M_{res} with V_{ctrl} and forcing the reference voltage in the tuning circuit to be equal to the V_{DS} of M_{res}, the ON resistance of the *master* and *slave* (M_{res}^1 and M_{res}) can be accurately matched. The complete bias circuit along with the reference generation branch is shown in Fig. 5. The reference generation circuit consists of a replica branch biased with twice the current in M_{res} to support the two branches of the tuning circuit. By symmetry, V_{ref} is equal to V_X. One problem with this simple reference generation is clock feed-through from the tuning circuit into the constant-g_m bias circuit through the gate-to-source capacitance (C_{gs}) of M_8. First order passive low-pass filter consisting of R_{CF} and C_{CF} is used to suppress the clock feed through.
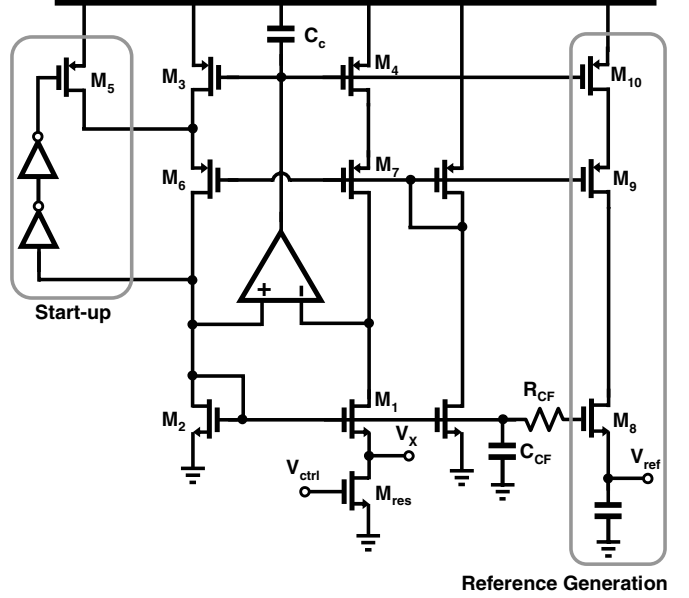

Fig. 5. Complete constant-g_m circuit with reference generation.

Stability is a major concern in any feedback system. Since the reference voltage in the constant-g_m bias circuit is generated by the tuning circuit, it is important to prevent interaction between the two circuits. The bandwidth of the tuning circuit is chosen much smaller than the constant-g_m bias circuit. This choice allows complete settling of the bias circuit before the tuning circuit makes the subsequent update of V_{ctrl}.

IV. SIMULATION RESULTS

The constant-g_m bias circuit along with the tuning circuit is implemented in $0.18\mu m$ CMOS process operating with $1.5V$ supply voltage. Fig. 6 depicts the control voltage settling transient of the tuning circuit. As mentioned earlier, a smaller bandwidth of the tuning circuit compared to that of the bias circuit leads to settling of the control voltage with out any overshoot. A supply voltage variation of $\pm20\%$ led to less than $\pm1\%$ variation in the transconductance. The dependence of the transconductance on the temperature is illustrated in Fig. 7. The transconductance varies by less than $\pm1.5\%$ for a $60°C$ variation in temperature.
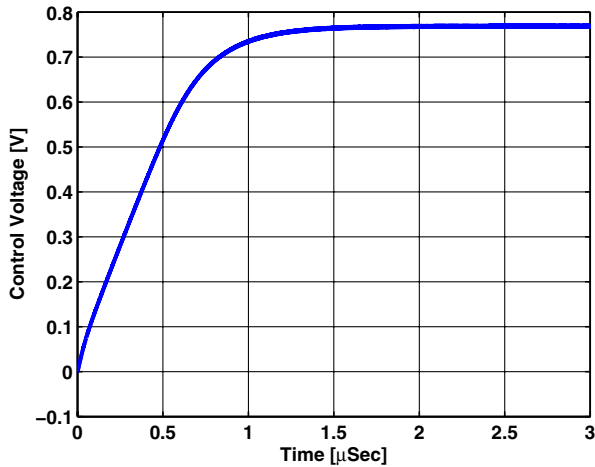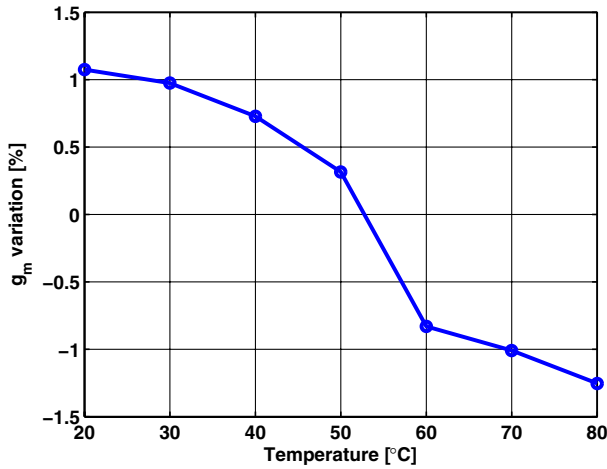
Fig. 6. Control voltage settling.

Fig. 7. G_m variation with temperature.

V. CONCLUSION

We presented a constant-g_m bias circuit along with a tuning circuit that obviates the need for an off-chip resistor. With an on-chip resistor, the problems associated with the external resistor such as stability and additional cost are eliminated. A *master-slave* tuning circuit based on time-constants matching is used to achieve stable transconductance that is immune to process, voltage and temperature variation. The bias circuit designed in $0.18 \mu m$ CMOS process has less than $\pm 1\%$ and $\pm 1.5\%$ variation of transconductance with 20% supply voltage variation and $60^{\circ}C$ temperature variation respectively.

VI. REFERENCES

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