The Effect of Switch Resistance on Pipelined ADC MDAC Settling Time

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***Abstract*— The goal of this paper is to provide an intuitive approach to switch sizing in SC circuits, focusing primarily on the MDAC of a pipelined ADC. Theory and simulation show that properly choosing the switch resistances to create a critically damped system can reduce the settling time of the circuit.**

I. INTRODUCTION

In the past decade, pipelining has become a dominant method for achieving mid-accuracy, mid-speed analog to digital converters, catering to applications like high-performance communication and video systems. The critical component of these converters is the first stage multiplying digital to analog converter (MDAC) that performs sampling, amplifying, and subtracting, typically in a single switch capacitor circuit. The performance of this block usually limits both the accuracy and maximum operating speed of the entire ADC.

A single ended version of the common "capacitor flip-over" implementation of a 1.5-b MDAC is shown in Fig. 1 [1]. During the first clock phase, the signal is sampled onto the sampling capacitors C_S and C_F. In the second phase, called the amplifying phase, C_F is switched into feedback around the amplifier and the bottom plate of C_S is connect to a voltage reference level, causing a charge redistribution that results in a signal amplification and subtraction by the voltage reference.

Unaddressed in most publications is the issue of sizing the CMOS transistors that perform the switching operations. There is a tradeoff between small sizes that can have switch resistances too large to allow proper settling of the MDAC, and large sizes that suffer from undesirable channel charge injection and clock feed-through due to parasitic capacitances. Designs aim to use the minimum sizes that do not adversely degrade the settling.

Traditional switch design involves matching all RC networks to a time constant approximately 3 to 4 times faster than the open-loop unity gain bandwidth of the network but ultimately relies on simulation to verify proper settling due to the complexity of the system.

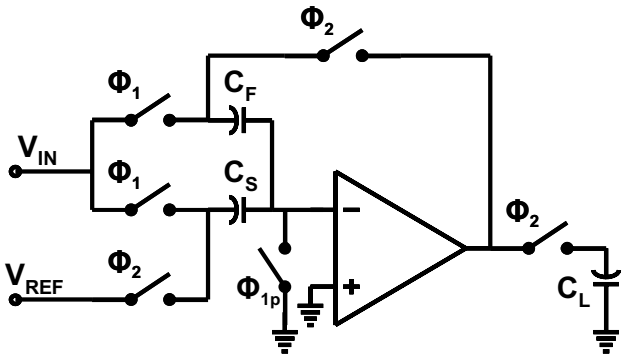

Fig. 1. Simplified "Capacitor flip-around" switched capacitor circuit commonly used as a pipeline ADC MDAC.

This paper aims to build intuition and provide insight into the effect of adding switch resistances as it relates to the step response and the pole/zero locations of the closed loop transfer function. Section II reviews damping of the ideal closed loop system for minimum settling time. Section III covers the effect of resistances in the sampling, feedback, and load branches of the MDAC during the amplify phase individually as well as together. Section IV gives simulation results using transistor level OpAmps, and Section V has concluding remarks.

II. DAMPING OF IDEAL MDAC

A. OpAmp Model

For many higher speed pipeline ADCs reported, single stage amplifiers are used, many with gain boosting [2],[3]. Therefore, the OpAmp model in this analysis is a g_m stage with an additional parasitic pole, expressed as (1). A large resistance at the model output determines the OpAmp gain.

$$\frac{I_o}{V^+ - V^-} = \frac{g_m \cdot a_2}{s + \omega_2} \tag{1}$$

B. Second Order MDAC Approximation

The open-loop transfer function of the inverting amplifier

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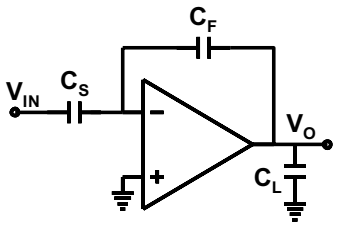

Fig. 2. Inverting amplifier configuration of MDAC amplify phase.

configuration gives the designer an estimate of the settling behavior of the step response, but knowing the pole/zero locations of the closed-loop system translates to the exact step response of the system.

The transfer function of the circuit shown in Fig. 2 is a second order system. By re-expressing the location of the OpAmp parasitic pole as a multiple of the loop unity gain bandwidth (2), the transfer function can be approximated as (4) with closed loop poles located at (6), natural frequency of (7), and damping factor of (8). The expression for the dominant pole approximated loop unity gain bandwidth (ω_u) of this circuit is (3). Finding the zero locations involves factoring F(s) (5).

$$\omega_2 = n \cdot (\omega_1 \beta A) = n \cdot \omega_u \tag{2}$$

$$\omega_u = \frac{g_m}{C_S + C_L\left(1 + \frac{C_S}{C_F}\right)} \tag{3}$$

$$\frac{V_O}{V_{IN}} \cong \frac{F(s)}{s^2 \frac{1}{n\omega_u} + s + \omega_u} \tag{4}$$

$$F(s) = \left(s^2 \frac{1}{\omega_2}\frac{C_S}{g_m} + s\frac{C_S}{g_m} - \frac{C_S}{C_F}\right)\omega_u \tag{5}$$

$$\omega_p = -\frac{1}{2} n \cdot \omega_u \left(1 \pm \sqrt{1 - \frac{4}{n}}\right) \tag{6}$$

$$\omega_n = \omega_u \sqrt{n} \tag{7}$$

$$\zeta = \sqrt{n}/2 \tag{8}$$

Depending on the relative spacing between the open loop poles, the closed loop system can be over- or under-damped, causing a slower transient or ringing respectively. Though a more precise settling optimization exists [4], a near optimal

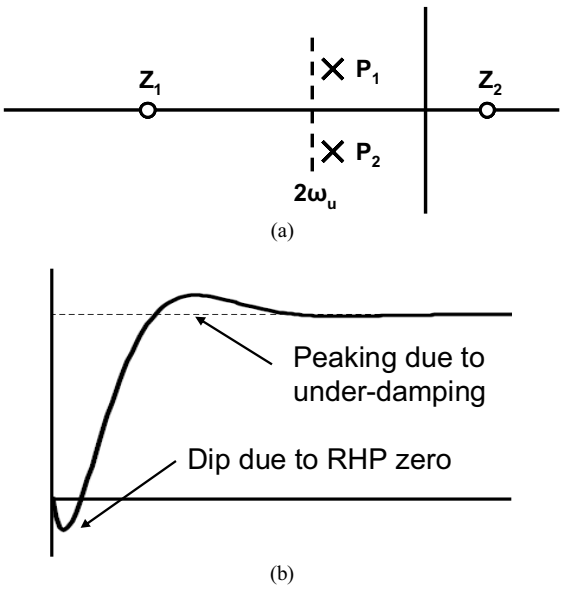

Fig. 3. (a) Pole/zero diagram of an under-damped, second order, inverting amplifier transfer function. (b) Corresponding step response

goal is critical damping for minimum settling time without overshoot. This occurs when the frequency of the parasitic OpAmp pole is 4 times greater than ω_u, corresponding to a 76 degree loop phase margin. In this case, the presence of the parasitic OpAmp pole reduces the settling time by 33% compared to a system without the parasitic pole. This is because the critically damped pole pair appears at twice the frequency of the loop unity gain bandwidth.

The pole/zero diagram for an under-damped example is shown in Fig. 3. The right half plane (RHP) zero causes an initial dip in the step response and is undesirable, while the LHP zero has a high enough frequency to have little effect.

Attaining a minimum settling time through critical damping is now extended to the cases where the feedback, sampling, and load branches also contain switch resistances.

III. Effect of Switch Resistances

Mathematically analyzing the response with added resistances is cumbersome. Instead, the pole/zero behavior is observed and compared to the no-resistance case.

From one amplify phase of the MDAC to the next, all switch resistances remain approximately constant except for the switches at the output of the OpAmp. For this analysis, all resistances are approximated as constants. A model MDAC in the amplifying phase with included switch resistances is shown in Fig. 4.

A. Sampling Switch Resistance, R_s

Adding a resistance in series with C_S dampens the system further and adds an additional pole without moving the zeros, as shown in Fig. 5(a).

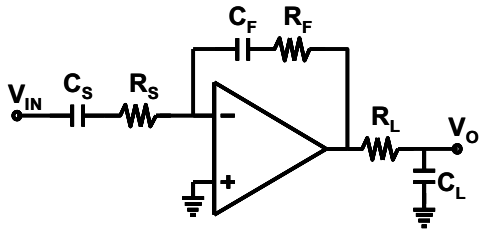

Fig. 4. Resistances are added to the inverting amplifier configuration to model the CMOS switches in the MDAC.

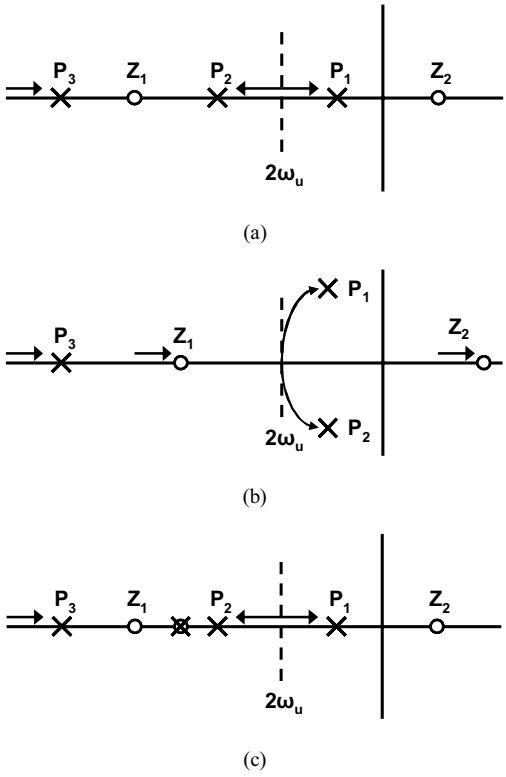

Fig. 5. Pole/zero diagrams showing the effect of adding series resistance to a critically damped inverting amplifier configuration in the a) sampling branch b) feedback branch c) load branch.

A unique case for adding sampling resistance to a critically damped system with equal capacitances ($C_S = C_F = C_L$) exists when the sampling branch time constant follows $\tau_S=R_SC_S=1/3\omega_u$. In this case, the dominant pole returns to ω_u, while the 2nd and 3rd poles converge on the LHP zero located at $6\omega_u$. In this example, the presence of R_F negates the effect of the OpAmp parasitic pole. Adding more resistance decreases the dominant pole frequency and creates a 2nd and 3rd pole doublet.

For an under-damped system with 60 degrees loop phase margin ($\omega_2=1.7\omega_u$), adding a resistance to achieve $\tau_S=1/0.6\omega_u$ reduces the required settling time by approximately 25% for 10-bit accuracy. Applying $\tau_S=1/\omega_u$ to a 45 degrees phase margin nearly halves the settling time compared to the case with no resistance.

B. Feedback Switch Resistance, R_f

When resistance is added in series with C_F in the critically damped system, it becomes under-damped. This also moves the RHP zero to a higher frequency, the LHP zero closer to the doublet, and introduces 3rd pole, as shown in Fig. 5(b). In most under-damped systems, adding any resistance of this kind decreases the speed of the circuit.

For the equal capacitance case, adding resistance as close as $\tau_F=1/2\omega_u$ to a critically damped system does not degrade the settling but adds a slight, 2% overshoot.

On the other hand, adding additional R_F to an over-damped system can increase the speed. In the rare case of a single pole system where ω_2 is non-existent, adding this resistance can be used to achieve up to near 50% reduction in settling time due to damping caused by the incoming pole and LHP zero.

C. Load Switch Resistance, R_L

A resistance in series with C_L changes the OpAmp output response similar to the sampling resistance, but also adds a zero. Though, when the response is calculated as the voltage across the load capacitor, the load RC pole cancels the added zero, as in Fig 5(c).

D. Corner Cases of Full System

Trends are difficult to identify while analyzing the system with the resistances included in every branche, but a few corner cases exist that reduce the complexity, assuming the capacitances are all equal.

1) $\tau_S = \tau_F = \tau_L = 1/\omega_2 = 1/4\omega_u$: In the case that all time constants are configured at 4 times the loop unity gain bandwidth, the system reduces to 2 poles located at ω_u and $4\omega_u$ respectively. Cancellation of the other poles/zeros also occurs at $4\omega_u$. Increasing τ_F to $3/4\omega_u$ reduces the settling time by 35% by reestablishing the critical damping and by moving the RHP zero.

2) $\tau_S = \tau_F = \tau_L = 1/\omega_2 = 1/2\omega_u$: When all time constants are configured at $2\omega_u$, the system again reduces to 2 poles, located at ω_u and $2\omega_u$. This case suffers a 10% increase in settling time for 10-bit accuracy compared to a system with a single pole at ω_u. Adding additional R_F shows little to no improvement in settling time, but reducing R_F actually decreases speed, suggesting that matching the resistor time constants is important.

In the second case, having 63 degree phase margin without resistances, matching all resistance time constants instead to $1/3\omega_u$ shows best performance, improving the settling time by over 25% compared to having no resistors. Therefore, adding resistors to an under-damped system can sometimes increase the speed because adding resistance to all branches in equal time constants often has an overall damping effect.

E. Changing the Feedback Factor

An MDAC that multiplies by more than a factor of 2 has decreased feedback factor (β) with C_S larger than C_F. Using a general capacitor scaling principle in this analysis of scaling the capacitors in each stage by the MDAC multiplying factor [5], C_L remains equal to C_F while C_S is varied to observe the effect of lower feedback factors. The gain of the OpAmp is also increased in this case to maintain the same bandwidth and phase margin.

1) $\beta=1/4$, $\tau_S = \tau_F = \tau_L = 1/\omega_2 = 1/4\omega_u$: A simplification through pole/zero cancellation once again, the two poles are located at $1.27\omega_u$ and $3.16\omega_u$. This is similar to the case with equal capacitances but closer to critical damping with pole/zero cancellation occurring at an even higher frequency. Increasing τ_F to $3/4\omega_u$ for critical damping reduces the settling time by approximately 25%.

2) $\beta=1/8$, $\tau_S = \tau_F = \tau_L = 1/\omega_2 = 1/4\omega_u$: Here, the two poles occur at $1.45\omega_u$ and $2.74\omega_u$, even closer to critical damping than for $\beta=1/4$. Increasing τ_F to $3/4\omega_u$ for critical damping reduces the settling time by around 14%.

Adding resistances to all branches in equal time constant amounts tends toward over-damping of the system, but configurations with smaller feedback factors experience less of the damping effect.

IV. Simulation

Analysis thus far is done with MATLAB and verified with models in a circuit simulator. Simulations with two different, transistor level, fully differential amplifiers are now presented. A 20mV differential step is applied to C_S and the linear settling of the output is observed across C_L.

With $C_S = C_F = C_L = 1$ pF and negligible OpAmp input capacitance, the gain-boosted, folded cascode OpAmp achieves a loop gain of 61 dB, a loop unity gain bandwidth of 150 MHz, and a phase margin of 85 degrees. In a closed loop configuration, this is an over-damped system that should settle to 10-bit accuracy in about 6.65 ns.

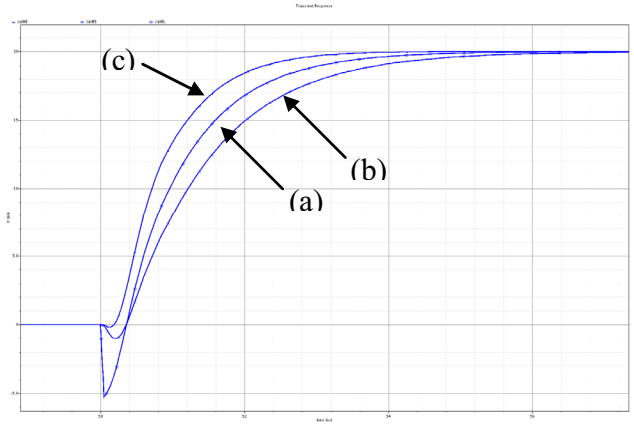

Fig. 6. Step response of the closed loop system with a) no resistance, b) with resistances that create equal time constants, 4 times faster than the loop unity gain bandwidth, c) additional resistance in the feedback path.

TABLE I
Step Response Settling Times

τ_S, τ_L	τ_F	Settling Time (ns)
0	0	3.6
$1/4\omega_u$	$1/4\omega_u$	4.2
$1/4\omega_u$	$1/2.67\omega_u$	3.2
$1/3\omega_u$	$1/3\omega_u$	4.77
$1/3\omega_u$	$1/2\omega_u$	3.74
$1/2\omega_u$	$1/2\omega_u$	5.8
$1/2\omega_u$	$1/1.33\omega_u$	4.25

Step response times for 10-bit settling of an inverting amplifier configuration in terms of the branch RC constants and the loop bandwidth.

Fig. 6 shows the step response of the closed loop system (a) without resistances, (b) with resistances satisfying $\tau_S=\tau_F=\tau_L=1/4\omega_u$, and (c) with additional feedback resistance such that $\tau_F=3.4/4\omega_u$.

Adding the resistances increases the 10-bit settling time from 6.5ns to 8.2ns, but providing the additional feedback resistance establishes critical damping of the system and lessens the initial dip by moving the RHP zero, changing the settling time to 4.5ns, a 45% time reduction.

Another example uses a folded, triple cascode amplifier with 100 fF input capacitance, $C_S = C_F = C_L = 300$ fF, 61 dB loop gain, 200 MHz loop unity gain bandwidth, and 70 degrees phase margin.

Simulation settling times for given resistances in this example are shown in Table 1. Note that in each of the cases with resistances, critically damping the signal involves increasing the feedback resistance such that $\tau_F = 1.5\tau_S$ which reduces the settling time by about 25%.

V. Conclusion

An intuitive description is provided for the effect of CMOS switch resistances on a typical pipelined ADC MDAC, as well as a demonstration of the necessity for proper switch sizing. In two example cases with transistor level OpAmp models, modifying the feedback resistance decreased the setting time by 45% and 25% respectively.

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