A High-Speed Delta-Sigma Modulator with Relaxed DEM Timing Requirement

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***Abstract*—This paper presents a high-speed digital feed-forward Delta-Sigma Modulator which relaxes timing requirement for the Dynamic Element Matching (DEM) algorithm. By making the main Digital to Analog Converter (DAC) process a small part of the input signal, the distortion from the DAC is suppressed. The proposed method allows eliminating the DEM circuitry in the critical data path for high-speed applications, thus achieving high-resolution without augmenting considerable silicon area. Analysis and simulation results verify the effectiveness of the proposed method.**

I. INTRODUCTION

A Delta-Sigma Modulator (ΔΣM) is a popular solution for high-resolution and low-power wideband telecommunication systems. This is due to the fact that low-accuracy circuit components can be utilized with less design effort via the trade-off between speed and resolution, compared to a Nyquist-rate data converter. Traditionally, ΔΣMs with a single-bit quantizer have been implemented in fully discrete-time topologies such as switched capacitor (SC) ΔΣMs. They can exploit good capacitor matching properties and inherently linear behavior of the single-bit DAC, and consequently they achieve highly accurate transfer functions and highly linear analog-to-digital conversion. However, the performance of a single-bit SC ΔΣM is limited by kT/C noise due to the inherent sampling nature at the input of the SC ΔΣM. Furthermore, the Operational Amplifiers (OpAmps) in the modulator should be fast enough to ensure a proper settling within a half clock period [1].

To obtain further performance improvement without the added stability problem and power consumption, a single-bit quantizer may be replaced with a multi-bit quantizer [1]. However, the multi-bit ΔΣM is prone to the Digital to Analog Converter (DAC) nonlinearity due to lithographic errors during fabrication that ultimately limit the Signal-to-Noise-and-Distortion Ratio (SNDR) to around 10 bits [1], [2] depending on the size of the DAC elements. So as to achieve better linearity performance, one can utilize a DAC linearization techniques such as the Dynamic Element Matching (DEM) techniques [3], [4], component sorting [5], or component sizing method [6]. Both the sorting and sizing methods, however, increase silicon area due to the fact that the sorting method requires the registers to contain comparison results and demands complex routing, and that the sizing method calls for larger components as the required resolution increases higher. On the other hand, the DEM method employs an averaging scheme, so that all of the elements in the DAC are equally used. As a result, silicon augmentation is minimal and the DEM technique effectively linearizes the nonlinear feedback DAC.

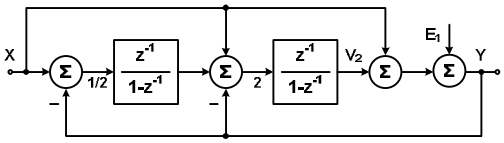

Figure 1. Conventional 2nd order wideband ΔΣM

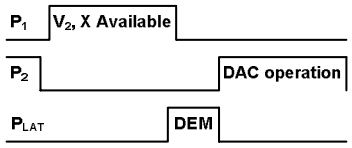

Figure 2. Timing diagram for the structure shown in Fig. 1

The DEM technique is not free from limitations, however. It needs considerable amount of time to execute the algorithm and is inappropriate in high frequency operation since it should be performed in the time slot (non-overlap time of clock phases) between quantization and DAC operations. This timing problem is more critical in a high-speed continuous-time ΔΣM as its operating frequency goes beyond half GHz [6]. Figs. 1 and 2 illustrate a conventional wideband ΔΣM [7] and a timing diagram related to the DEM operation, respectively. Ideally, the DEM algorithm can be processed before the DAC operation completes, but it burdens the first stage OpAmp in the modulator. In other words, the first OpAmp should be much faster to guarantee a

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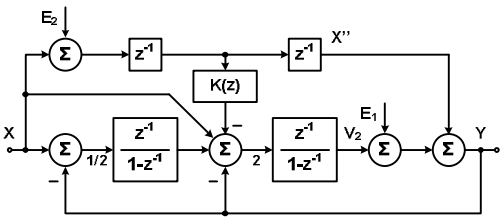

Figure 3. 2nd order wideband ΔΣM with digital feed-forward

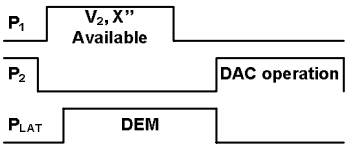

Figure 4. Timing diagram for the structure shown in Fig. 3

proper settling during the DAC operation.

Thus, it is necessary to develop a technique that allows the ΔΣM to operate at a higher clocking frequency without having to face a severe DAC nonlinearity problem. This paper is organized as follows. In Section II, detailed problem with the DEM in high-speed applications and operational principles are discussed. Various simulation results are presented in Section III. Finally, conclusions are given in Section IV.

II. DEM IN HIGH-SPEED APPLICATIONS

A. High-Speed ΔΣM

As the operating clock frequency increases, the OpAmps in the modulator become more power-hungry and so does the quantizer. To relax power consumption requirement, one can use the feed-forward technique in the analog [7], [8] or in the digital domain [9], [10]. As a result, the OpAmps are virtually independent from the input signal and process only the quantization noise.

Reference [7] and [8], however, have a tight timing specification for operating the DEM algorithm as shown in Fig. 2: The input signal X should be summed with the output of the 2nd integrator V_2, and the summed result should be resolved during phase 1 (P_1) to have a proper settling or charge distribution, depending on the type of analog adder used. Otherwise, the input signal is delayed and the signal transfer function of the modulator is not unity anymore.

On the other hand, [9] has relatively a relaxed timing for the DEM; since V_2 is already available at the end of phase 2 (P_2) and the delayed input signal is always ready for the entire clock cycle, the main quantizer, Q_1, can be activated at the beginning of P_1. Figs. 3 and 4 show the block diagram and the timing diagram of [10]. Despite the relaxed requirement, at a very high clocking frequency, it may still be difficult to perform a DEM algorithm in the main path which contains the main quantizer, Q_1.

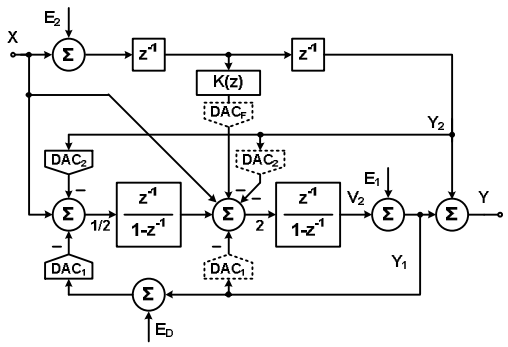

Figure 5. Redrawn block diagram

B. Relaxing the DEM timing requirement

A closer examination of the topology in Fig. 3 gives a possible solution to relax the DEM timing problem, and Fig. 5 shows a redrawn block diagram which is functionally equal to the one shown in Fig. 3.

Fig. 5 shows that the loop filter receives the input signal, X-Y_2. Deriving the system transfer function shows that

$$Y_{1,\,IDEAL} = 2(1-z^{-2})\,X + (1-z^{-1})^2\,E_1 - z^{-2}\,E_2 \text{ w/o } E_D \quad (1)$$

$$Y_{1,\,NON\,IDEAL} = Y_{1,\,IDEAL} + z^{-2}\,E_D \text{ with } E_D \quad (2)$$

$$E_2 = V_{REF} / (\text{Number of quantization levels of } Q_2) \quad (3)$$

where, Y_1 stands for the output of the main quantizer, X for the input signal, E_1 for the main quantization noise, E_2 for the auxiliary quantization noise, and V_{REF} for the reference voltage. The main DAC nonlinearity, E_D, however, is not shaped by the loop filter as shown in eq. (2) unlike the multi-stage noise shaping structure whose second stage is fed into a high-pass filter to cancel out the quantization noise of the first stage [1]. The distortion error of the main DAC shown in Fig. 5, however, is smaller than the DAC distortion error generated from the structure shown in Fig. 1. It is due to the fact that Q_1 ideally processes the quantization error of the auxiliary quantizer, E_2. As a result, DAC_1 creates negligible amount of distortion as the number of bits of Q_2 increases.

C. Quantization Levels of the Auxiliary Quantizer

As mentioned above, increasing the number of quantization levels of Q_2 helps to minimize the nonlinearity of DAC_1. E_2, however, cannot be infinitely small, since increasing the number of quantization levels of Q_2 requires more hardware, the implementation of which is typically a flash analog to digital converter (ADC) where the number of comparators would increase dramatically with the increase in the number of bits.

Another way to improve the resolution of Q_2 would be to replace the flash ADC with a two-step ADC or a pipeline ADC, so that the number of comparators would be reduced. This substitution does not consume a considerable amount of power since any error such as the OpAmp settling error and

the kT/C noise in the digital feed-forward path is cancelled out or at least shaped by the loop filter. This remains true even when there are path mismatches between the digital and analog paths [9], [10]. The number of stages of a pipeline ADC, however, is bound by the available time for the DEM operation in the digital feed-forward path.

D. DEM in the digital feed-forward path

In spite of the fact that the necessity of employing a DEM technique between the main quantizer and DAC is removed, the auxiliary DAC, DAC_2, still needs a DEM technique to linearize the DAC elements. This requirement, however, is no longer critical since it can use a full clock period or even more time (as much as the modulator is allowed to have). For example, in case of the 2nd order modulator, it is acceptable for the DEM operation to take two full clock periods. Since the output of the noise cancellation filter, *K(z)*, is injected into the input of the second integrator, it is shaped by a 1st order. Hence, the noise cancellation DAC does not require linearization/DEM.

III. Simulation Results

To demonstrate the validity of removing DAC linearization (DEM) in the main DAC, three 3rd order ΔΣMs are simulated using the MATLAB/Simulink® model [11], [12] under various conditions: one analog feed-forward ΔΣM [7] as a reference and two digital feed-forward ΔΣMs as illustrated in Fig. 6, one with a 4b auxiliary quantizer and the other with a 5b auxiliary quantizer. All simulations are carried out assuming that DAC_2 is linearized with the help of the DEM technique [10]. Simulation parameters are summarized in Table I.

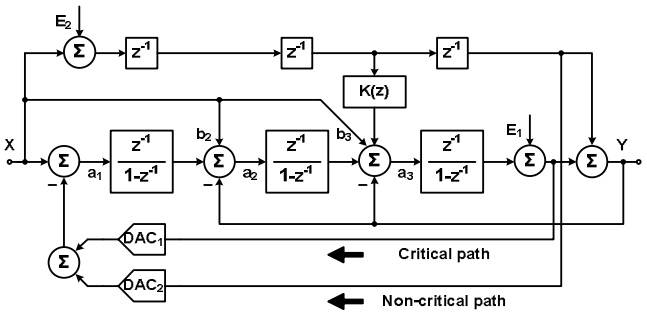

Figure 6. 3rd order ΔΣM without linearizing the main DAC, DAC_1

TABLE I. Simulation Parameters

Parameter	Value
Over sampling ratio	16
Signal bandwidth[a]	0.031
Input signal amplitude	-3dBFS
Number of points for FFT	65536
Main quantizer resolution	4-bit

a. Normalized to the sampling frequency

A. Main DAC nonlinearity

As expected from eqs. (2) and (3), the nonlinearity generated from DAC_1 is minimized as the magnitude of quantization error, E_2, decreases. Fig. 7 shows SNDR versus DAC_1 bit accuracy. It can be found that DAC_1 becomes insensitive to DAC nonlinearity, as the quantization error of Q_2 decreases. This, however, does not completely eliminate the harmonics. Fig. 8 shows power spectral density for 3 different modulators with the same 7b main DAC accuracy. SNDR degradation due to the nonlinear DAC, however, is not significant. The degradations are 3dB and 0.1dB for 4b and 5b auxiliary quantizer, respectively. Furthermore, the loss is less critical when other nonideal effects, such as kT/C noise and settling error, are considered. Table II summarizes the simulation results for each of these three cases with an additional baseline case involving ideal linear main DAC.

It is notable that the conventional modulator shows severe SNDR degradation. This is due to the fact that there is only one DAC which processes the whole input signal. In such conventional design, it is necessary to use a DEM algorithm (under tight/difficult time window allotted for this task) to suppress DAC nonlinearity.

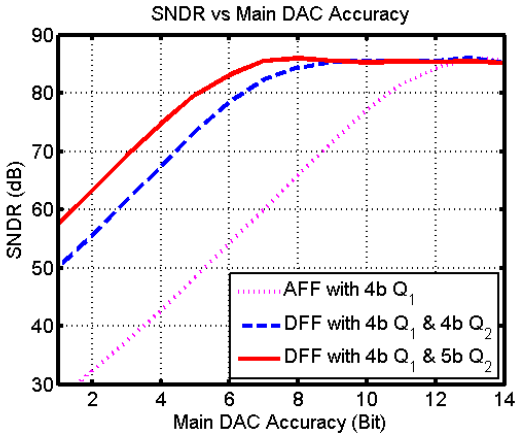

Figure 7. SNDR vs Main DAC accuracy

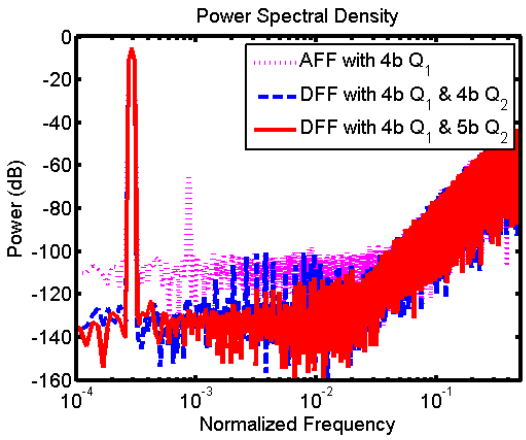

Figure 8. Power spectral density for 3 different cases

TABLE II. SIMULATION RESULTS

Modulator	SNDR
Ideal 3rd order AFF ΔΣM	85.5dB
3rd order AFF ΔΣM with DAC nonlinearity	60.0dB
3rd order DFF ΔΣM with DAC nonlinearity and 4b Q_2	82.4dB
3rd order DFF ΔΣM with DAC nonlinearity and 5b Q_2	85.4dB

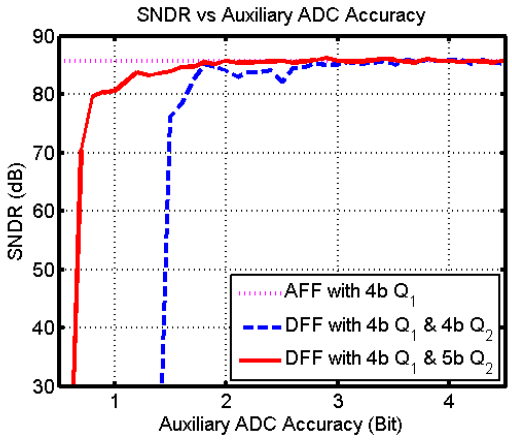

Figure 9. SNDR vs Auxiliary ADC accuracy

B. *Auxiliary quantizer nonlinearity*

Nonlinearity generated from the auxiliary quantizer is not detrimental since it is cancelled out at the modulator output as mentioned before. Fig. 9 shows that the modulator is robust to nonlinearity from the auxiliary quantizer but, after a certain point, the modulator performance is undermined due to the available swing limitation of the integrators. This condition, however, is easily avoided by decreasing the quantization error of the auxiliary quantizer.

The conventional modulator does not show any degradation in the figure, because the analog feed-forward path does not utilize an auxiliary quantizer. However, it is important to remember once again that the conventional topology is not suitable for high-speed applications due to the lack of time available for the DEM logic circuitry to work properly.

IV. CONCLUSIONS

A high-speed ΔΣM with a relaxed DEM timing requirement has been presented. By eliminating the DEM circuitry in the critical path between the main quantizer and the DAC, the proposed modulator can operate at much higher clocking frequency without increasing the power consumption of integrators. Employing the DEM in the feed-forward path becomes an easy task since this path can have more than a full clock delay (specifically two full clock periods in the example shown). Obviating the use of the DEM algorithm in the critical path enables the modulator to minimize the size of the DAC element without degrading modulator's performance, thus economizing silicon area. Furthermore, increasing the number of levels of the auxiliary quantizer may possibly be achieved by replacing the quantizer with a two-step or a pipeline ADC. Naturally this implementation possibility would depend very much on the number of delays in the digital feed-forward path. The presented ΔΣM example is suitable for high-speed and high-resolution applications.

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