Enhanced Multi-bit Delta-Sigma Modulator with Two-Step Pipeline Quantizer

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***Abstract*—A new delta-sigma Analog-to-Digital Converter (ADC) is presented in this paper. A two-step pipeline ADC is used as the quantizer of this delta-sigma modulator to reduce the quantization noise at the output of the modulator. The proposed structure relaxes the output swing and gain requirements of the integrators. In addition, the front-end DAC of the proposed modulator is simplified. Simulation results verify the effectiveness of the proposed architecture.**

I. INTRODUCTION

Delta-sigma ADCs are commonly used for applications with high over-sampling ratios and high resolution. However, as the demand for delta-sigma ADCs with higher bandwidth increases, designers have to contend with lower OSR. In order to maintain the performance at a reduced OSR, it is necessary to reduce the in-band quantization noise density. Most single-stage multi-bit modulators use low number of bits for internal quantization.

Each additional quantizer bit improves overall SNR by 6dB and also improves modulator stability, which permits aggressive noise shaping. However, the number of quantization levels is limited by the front-end digital-to-analog (DAC) converter due to the increased burden in the dynamic element matching (DEM) circuitry.

Cascaded modulators can overcome this problem by employing a high-resolution multi-bit quantizer as the second stage [1], but to minimize the quantization noise leakage at the output, high DC gain opamp should be used [2], making it power hungry in high-speed applications.

Modulators with two-step quantizers are the other choice for delta sigma ADCs with multi-bit quantizers [3, 4]. The main problem of these modulators is implementation of segmented input DAC; the performance of these modulators is limited to the linearity of front-end DAC.

In this paper, a new delta-sigma ADC is introduced. In the proposed structure, quantizer of single loop modulator is replaced with a two-step pipeline ADC and conventional modulator is modified to tolerate latency of two-step pipeline ADC. Moreover, segmented input DAC is avoided in the proposed architecture.

II. CONVENTIONAL DELTA-SIGMA MODULATORS WITH HIGH RESOLUTION QUANTIZERS

In this section, two well-known delta-sigma modulators with high-resolution quantizers are briefly studied.

A. TheDelta-Sigma Modulator with Two-Step Quantizer

The architecture of modulator with two-step quantizer is shown in Fig1. In practice, a flash converter with M-bits conversion performs the first coarse conversion. The output of loop filter is sampled by an MDAC at the same time the *ADC1* is triggered. Then the difference between the coarse conversion result and the sampled loop filter output is amplified by the MDAC and the error is A/D converted by an N-bit flash converter *ADC2* [3].

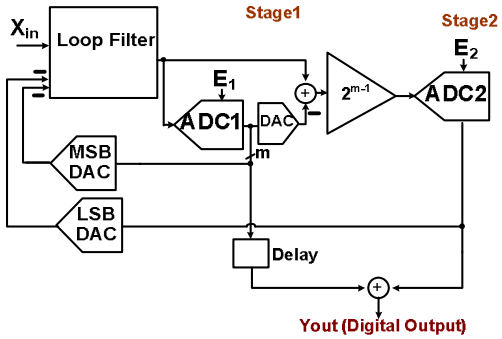

Figure 1 The conventional modulator with two-step quantizer

A second order delta-sigma modulator with two-step quantizer is shown in Fig.2. Here, half delay integrator stages are used to permit additional delay in the feedback path to all integrators except the last. This additional delay makes it possible to apply DEM to shape the first stage DAC noise digitally. Even though two half-delay integrators are utilized in Fig.2, this modulator has the same form of

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noise/signal transfer function as a standard second order sigma-delta modulator [4].

Similar to using two-step quantization to reduce the number of comparators in the flash ADC, one can use the segmented DACs to greatly reduce the number of unit elements in the DAC. Since the quantization noise of first quantizer (ADC1 in Fig.1) is supposed to be canceled at the input of modulator, LSB and MSB sections of segmented DAC segmented DAC should be considerably matched. Although the mismatch noise inside each individual section (LSB and MSB section) of segmented DAC can be filtered by two independent DEM circuits, part of coarse quantization noise caused by the mismatch between LSB and MSB sections leaks into system output with no noise shaping.

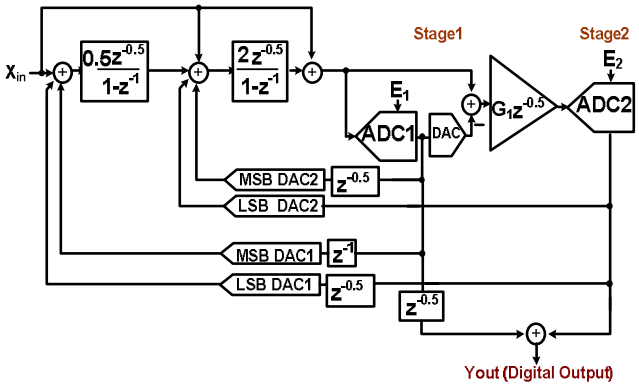

Figure 2 Example second-order modulator with two-step Quantizer

B. *Cascaded Delta-Sigma Pipeline Architechture*

A cascaded delta-sigma pipeline ADC is shown in Fig.3. in this architecture, a pipeline ADC is cascaded with a delta-sigma modulator and quantization noise of quantizer inside the modulator loop, E_1 is canceled at the output by employing a digital noise transfer function. In order to cancel E_1 effectively, high gain integrators should be used inside delta-sigma loop [1,5].

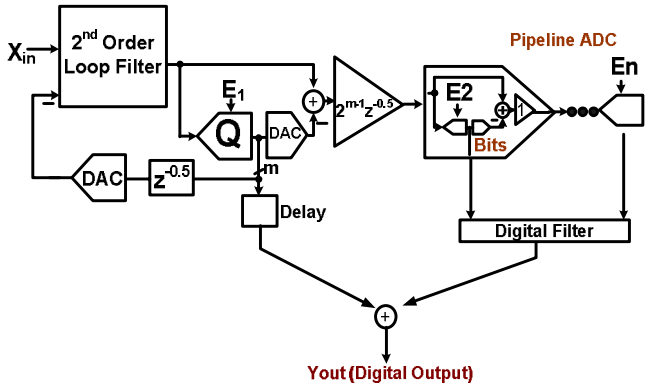

Figure 3 Cascaded Delta-Sigma Pipeline Architecture

Unlike the modulators with two-step quantizers, only digital outputs of first quantizer are fed back to the input .As a result complexity of input DAC is reduced compared to the modulators with two-step quantizers.

III. THE PROPOSED MODULATOR WITH TWO-STEP PIPELINE QUANTIZER

The architecture of the proposed second order modulator with two-step pipeline quantizer is shown in Fig.4.

The basic building block of the proposed structure is similar to conventional modulator with two-step quantizer, except that in the proposed structure, the need for segmented DAC or complex unit element DAC (7-8 bit DAC) is eliminated by feeding back only the digital outputs of first pipeline stage to the input of the modulator. These digital outputs contain both input signal of pipelined quantizer and first stage quantization error, E_1, as shown in Fig. 4. Furthermore, to cancel E_1 in the modulator loop, the analog residue of the first stage is subtracted from the digital feedback signal at the input of the modulator. This leaves the integrators to process only the quantization error of the second pipeline stage, E_2 which is provided by analog residue of second stage.

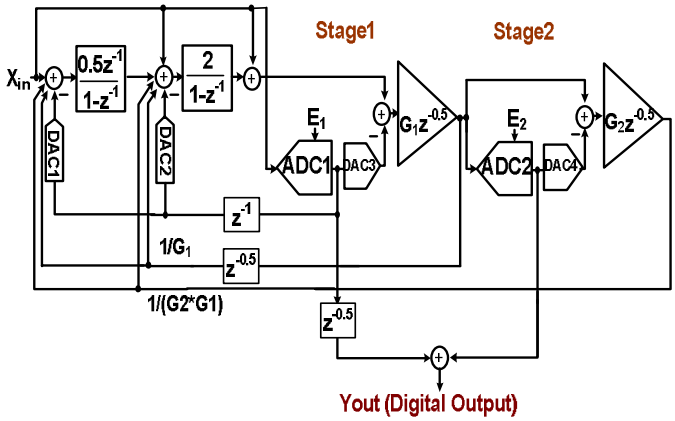

Figure 4 The Proposed Delta-Sigma Modulator

Similar to conventional modulator with two-step quantizer, loop filter should be modified to tolerate additional delays generated by pipeline stages. In order to achieve proper signal and noise transfer functions, one delay free integrator is used in the loop filter; digital output of first pipeline stage is fed back to the input with a delay while analog residue of this stage is fed back to the input with half-delay. As a result, the digital output of modulator can be expressed as:

$$Y_{out} = X_{in} + (1-z^{-1})^2.(E_1 - (1+\frac{1}{A_{res}})E_1) + \frac{E_2}{2^{m1-1}}(1-z^{-1})^2 \qquad (1)$$

Here X_{in}, E_i , m_1, and A_{res} denote the input signal; i^{th} stage quantization error ; number of bits resolved in the first stage

and DC gain of pipeline residue amplifier respectively. Since modulator with feed-forward is used as the loop filter, the signal transfer function is equal to one.

Fig.4 shows that one extra residue amplifier is needed in the proposed architecture compared to the conventional second order modulator with two-step quantizer. However, the need for the extra amplifier can be eliminated by sharing the residue amplifier between two pipeline stages.

Furthermore, the first quantizer, *ADC1*, is connected to the input signal, *Xin,* directly. Since the output signal of second integrator is fed back to the input of modulator through the analog residue feedback path, connecting the ADC1 to the input signal does not change the functionality of modulator.

The key feature of this architecture is utilizing analog residue of pipeline stages to avoid the complex front-end DACs in multi-bit delta-sigma modulators. This method can be applied to different delta-sigma modulators and even more pipeline stages can be used inside delta-sigma modulator by managing the pipeline delays properly.

IV. PRPERTIES OF THE PROPOSED DELTA-SIGMA MODULATOR

A. *Quantization Noise Leakage*

Although, quantization noise of first stage, E_1 is ideally cancelled out, quantization noise leakage will appear at the output due to limited DC gain of pipeline residue amplifier. However, this quantization leakage is shaped by the delta sigma modulator.

In the conventional modulator with two-step quantizer, mismatch between LSB and MSB DACs causes quantization noise leakage, too. Since unit elements of LSB DAC are much smaller than unit elements of MSB DAC (1/16 for two 4 bit DACs), satisfying the matching requirement in the conventional modulator is difficult.

In the proposed structure, E_1 is canceled out by subtracting the analog residue from digital feedback signal; thus, quantization noise leakage can be eliminated by sharing capacitors of front-end DACs of modulator (DAC_1 or DAC_2 in Fig.4) between digital and analog residue feedback paths.

B. *Gain Requirements of loop amlifiers*

Gain and swing requirements of the proposed and the conventional two-step modulator are similar. Equation (2) shows amount of quantization leakage of first stage and it shows that the gain of the integrators (A_{int}) used in the loop filter has no effect on the cancellation of E_1. Thus, the gain requirements of integrators in the loop filter are greatly relaxed. Fig.5 shows the output SNR against the first integrator opamp DC gain.

$$\text{Leakage} = (1+\frac{1}{A_{int}})^2.(1-z^{-1})^2.(E_1-(1+\frac{1}{A_{res}})E_1) \qquad (2)$$

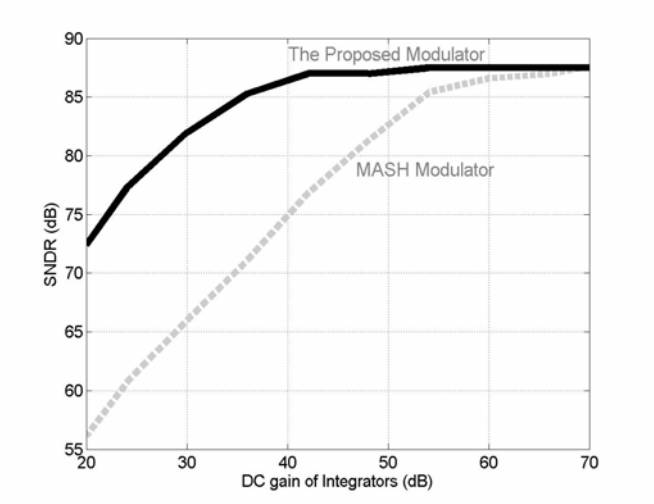

Figure 5 The output SNR against the first integrator opamp DC gain

C. *Linearity requirements of DACs in pipeline Stages*

Nonlinearities generated by internal DAC of first pipeline stage is shaped by the order of loop filter while nonlinearites generated by internal DAC of second pipeline stage is suppressed by the interstage gain of two-step pipeline quantizer. Fig.6 shows the output SNR versus linearity of DACs.

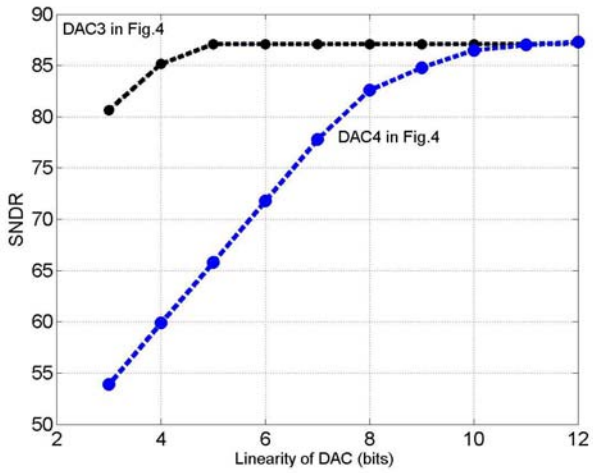

Figure 6 Linearity of pipeline DACs in the proposed modulator

V. SIMULATION RESULTS

The effectiveness of the proposed modulator is demonstrated in simulink. Simulation results show that overall SNR at OSR of 16 for a second order modulator with two-step quantizer, each resolving 3.5 bits, is 92 dB in ideal case. The overall SNR will be 80dB considering all non-idealities including DC gain of integrator, DC gain of residue amplifier, and nonlinearity of all DACs. The

simulation results are summarized in Table I and output spectrum is shown in Fig. 7. Fig.8 shows the output SNDR versus input signal.

TABLE I. SIMULATION RESULTS

OSR	16
Order of Modulator	Second Order
Resolution of Quantizers	Each stage (3.5 bits)
SNDR (Ideal)	92 dB
SNDR (w/ non-idealities)	79.42 dB =13 bits
Gain of Integrators (feedback factors = 1/2, 1/6)	34dB
Gain of Residue Amplifier (feedback factor = 1/16)	52dB
Linearity of DAC1	8 bits
Linearity of DAC2	8 bits
Linearity of DAC3	6 bits
Linearity of DAC4	8 bits

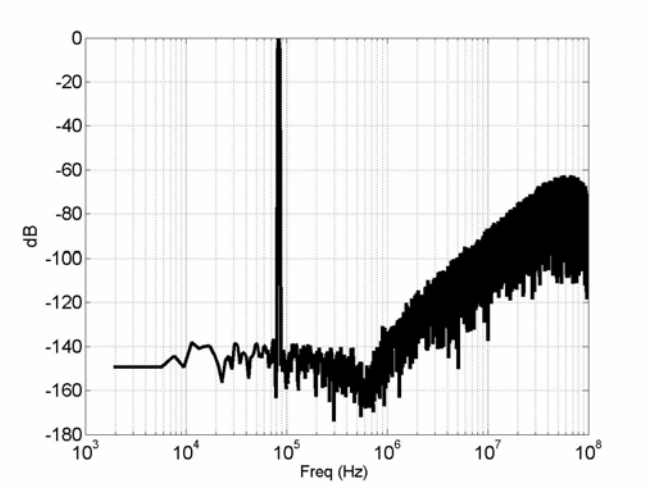

Figure 7 Output Spectrum of the Proposed Delta-Sigma Modulator

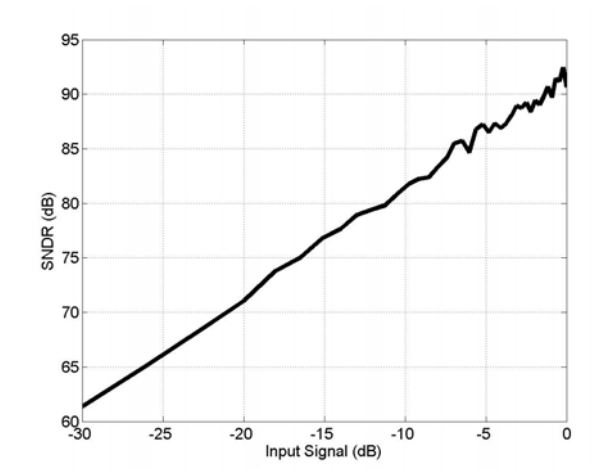

Figure 8 Output SNDR versus Input Signal

VI. CONCLUSION

A new delta-sigma modulator with two-step pipeline quantizer is proposed. The input DAC of the modulator is provided by the first stage of the pipeline ADC output, resulting in reduced hardware complexity. This structure effectively combines the advantages of a MASH delta-sigma modulator, i.e. simplicity of feedback DAC, and of a delta-sigma modulator with two-step quantizer, i.e. low gain and swing requirements, to provide improved SNDR. The relaxed modulator coefficient accuracy and reduced quantization leakage makes this structure suitable for high-accuracy and high-speed applications

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