Multi-Loop Efficient Sturdy MASH Delta-Sigma Modulators

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***Abstract*— An extended version of sturdy MASH delta-sigma modulators is presented in this paper. Improved performance is achieved using in-band zero optimization. The challenges towards high order multi-loop modulators are discussed and a new multi-loop modulator is presented. This modulator benefits from a MASH architecture in the final loop to preserve stability, while the main loop benefits from relaxed circuit building blocks of the SMASH structure. Extensive simulation results are provided to prove the efficiency of this structure.**

I. INTRODUCTION

Wideband analog-to-digital converters (ADCs) are one of the most critical parts in many digital communication systems. To minimize the channel bandwidth, high resolution signal quantization is required to maximize the transmission rate. Two commonly used ADCs in communication systems are pipelined ADCs and Delta-Sigma Modulators (DSMs). Pipeline analog to digital converters are well known for their wide signal band conversion with moderate accuracy, while delta-sigma modulators are most known for their noise-shaping attribute, suitable for high accuracy low-to-moderate band applications. Delta-sigma modulators architectures fall into two main categories. First are the single loop modulators, which benefit from relaxed circuit elements, but suffer from stability problems in high order modulators. Second are the multistage noise-shaping modulators (MASH). MASH modulators are well known for their stability, but they require digital filters to match with analog transfer functions, putting more burden on analog building blocks. Recently, a new multi-loop modulator was presented [1] which benefits from stability of simple multi-loop modulators, while the circuit requirements are relaxed.

In this paper, methods to optimize the performance of Sturdy MASH (SMASH) structure are presented, and a new mixed structure which uses both SMASH and MASH structure is presented (S-MASH^2). This paper is organized as follows. Section II provides the properties of the MASH structure and a brief review of the SMASH structure. Methods to increase the performance of the SMASH structure and their tradeoffs are presented in Section III. The proposed S-MASH^2 is presented in Section IV to solve the problems associated wide multi-loop SMASH structures. Extensive simulation results are provided in Section V to prove the efficiency of the proposed structure, and finally conclusions are drawn in Section VI.

II. MASH VERSUS SMASH

A general two-loop MASH structure is shown in Fig. 1, where L_{si}, L_{ni} and E_i denote the signal loop filter, noise loop filter and quantization error of the i^{th} stage, respectively. The basic concept of this architecture is to cancel all quantization errors at the output using digital filters H_i, except for the last stage quantization error which will be shaped by overall order of the modulator. However, due to path mismatch between analog signal transfer functions (STFs), noise transfer functions (NTFs) and digital paths, i.e. H_i, quantization noise of the preceding loops might leak to the output, degrading the overall performance [1]. Hence, highly accurate analog building blocks are needed to minimize this undesired effect, leading to higher power dissipation. Fig.2 shows a general form of the SMASH structure presented in [2]. The main advantage of SMASH is that it uses only analog filters, so digital filters are removed and analog circuit building blocks are relaxed. While the MASH architecture, in ideal case allows us to cancel the quantization error of all the preceding stages, the SMASH structure will shape all quantization errors with the overall modulator order.

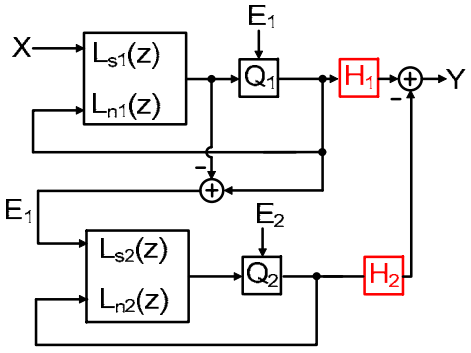

Figure 1. General MASH structure.

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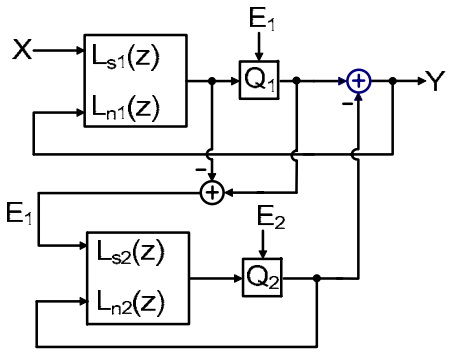

Figure 2. General SMASH strcuture.

The price paid is an additional DAC at the input of the modulator, and a slight increase in swing of the integrators. In general, there are no specific constrains on the signal and noise transfer function of the first loop. To minimize the number of the DACs in the first loop, structures such as [4] can be used.

In wide band applications it is more desirable to spread the zeros over the signal band. For example, using this technique one can improve the overall SNR of a 4^{th} order modulator by 13 dB at an oversampling ratio (OSR) of 32 [5]. Unfortunately, a 4^{th} order single loop modulator might suffer from stability issues. MASH can guarantee the stability, but the digital filters will become very costly and in some cases not practical, as they have to match complex analog transfer functions. However, the stability advantage of MASH structure allows employing very high order of noise shaping by cascading many stages (theoretically infinite number of stages can be cascaded, but the performance is limited to quantization noise leakage and circuit non-idealities). As it will be shown later, this approach can be applied to SMASH architecture with only a slight modification.

III. Efficient SMASH Structures

A simple 2+2 SMASH structure is shown in Fig. 3. The overall output is as follows

$$Y = STF_1 X + NTF_1 NTF_2 E_1 - NTF_1(1 - STF_2)E_2 \quad (1)$$

where

$$STF_2 = 2z^{-1} - z^{-2}. \quad (2)$$

Satisfying above equation will result in fourth order noise shaping for both E_1 and E_2, with all zeros placed at DC. As discussed in detail in [3], this structure is less susceptible to opamp DC gain compared to the traditional MASH structure. However, the price paid is decreased dynamic range of the modulator. Here, an important question arises: *What are the tradeoffs in high order multi-loop SMASH modulators*? To answer this question, first the optimization of SMASH is presented. Next, a detailed analysis of multi-loop SMASH modulators is provided.

As discussed before, for wideband applications it is more desirable to spread the zeros in the signal passband in order to

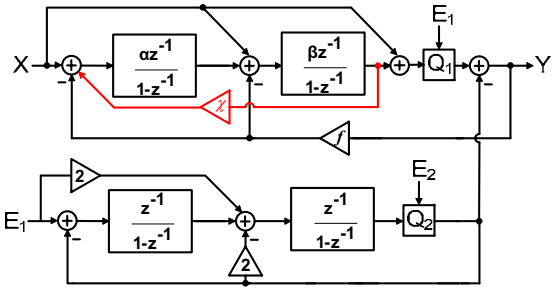

Figure 3. 2+2 SMASH structure with two in-band zeros.

minimize the noise power in the signal band. For the SMASH structure shown in Fig. 3, it can be seen that NTF_1 is shaping both quantization errors, while NTF_2 and $(1\text{-}STF_2)$ is shaping E_2 and E_1, respectively.

One simple way to put zeros in the passband is to keep second loop unchanged, and change only the first loop coefficients to achieve optimal zero placements. This is shown in Fig. 3. As it can be seen, the output of the second integrator is fed back to the input of the modulator, causing the zeros to move away from DC. With proper selection of the extra feedback coefficient, two complex zeroes will be placed at the edge of the signal band and the other pair will remain at DC. Fig.4 compares the performance of two different 2+2 SMASH structures; one with all zeros at DC and another with an in-band zero pair. It can be seen at OSR of 12, this simple technique adds extra 10 dB to the overall performance, without deteriorating the stability of the modulator. This advantage over traditional multi-loop structures, along with relaxed opamp DC gain, makes this structure suitable for low power wide-band applications. It is worth to note that in SMASH structure, the only constrain is the second stage signal transfer function, so first loop can be chosen with respect to design requirement needed. Another way to improve the performance of the modulator is to increase the order of the modulator. This can be done in two different ways. First is to employ higher order first or second loop. The second choice is to add more loops and repeat the same derivation for signal and noise transfer functions. From a stability aspect, the first option is not recommended, since a high order single loop has the potential to go unstable. As it will be seen shortly, the second option will also suffer from dynamic range degradation.

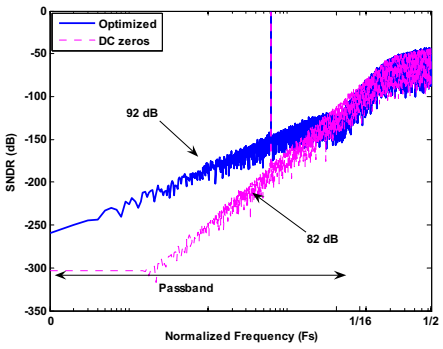

Figure 4. Comparasion between all zeros at DC and two zeros at edge of the signal band.

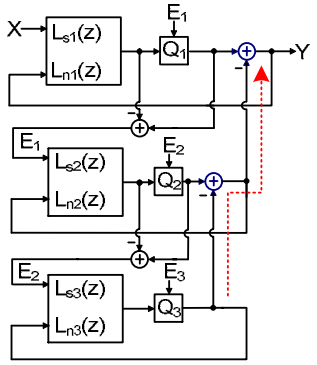

Figure 5. Cascaded SMASH loops.

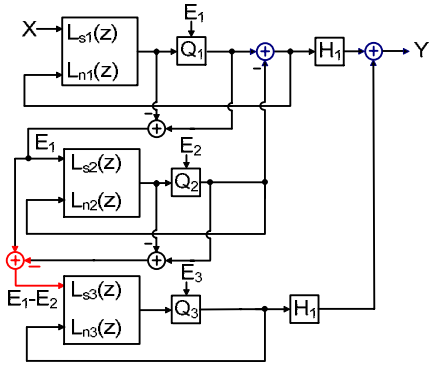

Figure 6. S-MASH^2 Structure.

Multi-loop SMASH architecture is shown in Fig 5. The same derivation as was done for the 2+2 SMASH structure, can be repeated for a 2+2+1 SMASH structure to achieve 5^{th} order noise shaping, yielding

$$y = STF_1X + NTF_1NTF_2NTF_3E_3 - NTF_1NTF_2[1 - STF_3]E_2 + NTF_1[1 - STF_2]E_1. \quad (3)$$

It can be calculated that if the signal transfer function of the last loop, i.e. STF_3, is chosen to be a delay, E_2 along with E_3 will be fifth order shaped. However, to shape the first stage quantization error, modification in the second loop signal transfer function is needed. In [3], this transfer function was calculated and one possible implementation was presented. From pure mathematic perspective, it is possible to increase the order of noise shaping even further, but as the order of noise shaping increase by adding extra loops, the first loop will start to saturate sooner. It is worth mentioning that the third loop output is added to the first loop via the second loop output, causing serious dynamic range degradation. To overcome this problem, a unique combination of SMASH and MASH is presented (S-MASH^2) which combines advantages of both structures without drawbacks such as high sensitivity to opamp DC gain and modulator saturation.

IV. S-MASH^2 Delta-Sigma Modulators

As discussed before, the idea of the MASH structure is to cancel out all the quantization errors except that of the last loop, which will be shaped by the order of the modulator. Unlike the MASH structures, in the SMASH structure, all quantization errors will be shaped by the order of the modulator. Hence, increasing the number of the loops will result in dynamic range degradation.

Combining MASH and SMASH could be done by feeding E_1 and E_2 to the third loop, and subtracting its output with the output of the first stage via digital filters, depicted in Fig. 6. Note that E_2 is added with a negative sign to the input of the third loop to cancel out the negative sign addition in the first loop. Combining equation (1) with the output of the third loop will yield

$$Y = H_1STF_1X + E_1(H_1NTF_1NTF_2 - H_2STF_3) - E_2[H_1NTF_1(1 - STF_2) - H_2STF_3] - E_3H_2NTF_3. \quad (4)$$

As in the MASH structure, E_1 and E_2 can be easily cancelled out by proper selection of digital filters, which in this case would be

$$H_1 = STF_3$$
$$H_2 = NTF_1NTF_2 = NTF_1(1 - STF_2). \quad (5)$$

Choosing digital filters as derived above will result in cancelation of both E_1 and E_2 at the output of the modulator. Consequently, and in an ideal case, the only quantization error which is going to appear at the output would be E_3, which will be fifth order shaped. This structure is extendable to higher order modulators by adding extra loops in a MASH configuration. It is important to note that unlike the MASH structure where path mismatch between analog and digital could result in serious performance degradation, in this structure, the need for highly accurate path matching is alleviated. In this structure, the last output will be compared with the product of the gains of the first and second loop, and will be fourth order shaped. This will be shown later in simulation results.

One possible implementation of 2+2+1 S-MASH^2 is shown in Fig.7. As it can be seen from this figure, the output of the third loop is subtracted from the output of the first loop via a digital filter shown with dashed lines. This digital filter is chosen to be equal to NTF_1NTF_2. Signal feed-forward is used in the first loop to relax linearity and swing requirements of the first and second integrators.

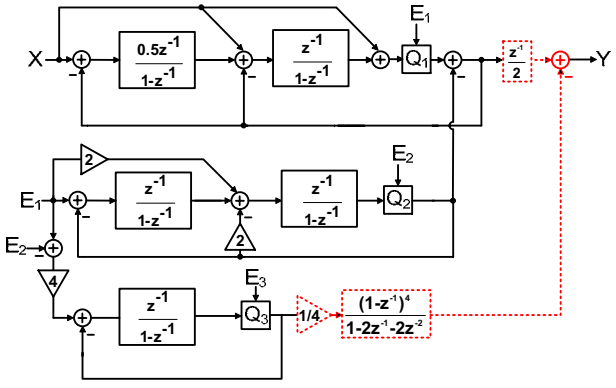

Figure 7. 2+2+1 S-MASH^2 example.

V. Simulation Results

The proposed S-MASH^2 shown in Fig. 7 was simulated and compared with 2+2+1 MASH structure. For these simulations, OSR of 12 was used. Both structures use 4-bit quantizer for the first and last loop, and 2-bit quantizer for the second loop. Interstage gain of 4 was used to utilize the full dynamic range of the last loop. Fig. 8 plots the SNR versus first integrator DC gain of S-MASH^2 and MASH structure while all the other integrators are ideal. As it can be observed from this figure, the proposed structure is less sensitive to opamp gain. This difference becomes significant when opamp DC gain drops below 50 dB, as noted in this figure. Fig. 9 illustrates SNR versus all integrators DC gain. Note that traditional MASH structure will not settle even with 70 dB opamp gain.

To verify the stability and dynamic range of the proposed structure, SNR versus input amplitude for both structures are plotted in Fig. 10. In this figure ideal integrator were used for both MASH and S-MASH^2 structures.

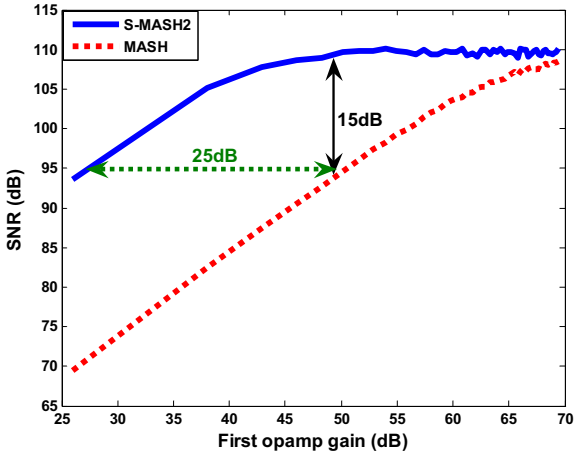

Figure 8. SNR versus first integrator gain.

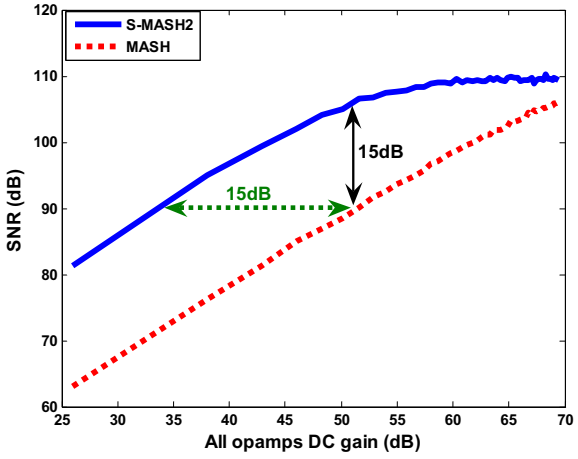

Figure 9. SNR versus all integrators gain.

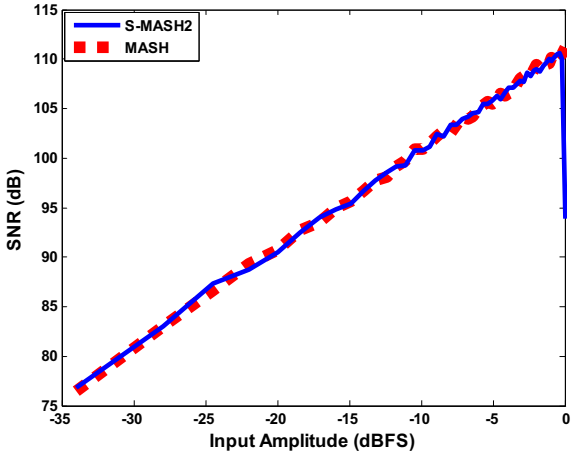

Figure 10. SNR versus input amplitude.

As this figure illustrates, both structures are capable of converting full-scale signal into digital output. This is while the first loop in S-MASH^2 should also process second stage quantization error, i.e. E_2, which will result in slightly increased swing at the output of the first and second integrators compared to that of the MASH structure.

VI. Conclusions

A simple method was proposed in this paper to enhance the performance of the SMASH structure. After reviewing challenges towards multi-loop high order noise shaping, a new multi-loop architecture was proposed. Compared to the traditional MASH structure, the S-MASH^2 modulator is less sensitive to path mismatch between analog transfer functions and digital filters, while the overall performance is comparable with the MASH structure. S-MASH^2 has the potential to be used in multi-loop very high order modulators without stability issues. All these properties make this structure a suitable candidate for wideband low power applications.

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