Reducing the Effects of Component Mismatch by Using Relative Size Information

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***Abstract*—This paper shows how the relative size of components can be used to increase matching performance – saving orders of magnitude in component area. The relative size information can be found by ordering the elements from smallest to largest. A circuit to do this is described. Properties of ordered devices are summarized. Improvements are quantified for simple feedback circuits and matched devices constructed from ordered sub-elements. The INL of a 17-level D/A converter is simulated, and the methods are shown to increase linearity by 5 bits.**

I. INTRODUCTION

Component mismatch is often a performance-limiting factor in analog circuits such as A/D and D/A converters. Component mismatch can be dealt with in various ways including making the devices larger [1], digital calibration [2], error averaging [3], data weighted averaging [4] or self-configured capacitor matching [5]. This work shows how the information contained in the relative sizes of elements (easily obtained by ordering them from smallest to largest) can be used to cancel the mismatches, giving matching performance equivalent to elements orders of magnitude larger.

Section II shows how using the relative size of devices to determine where they are placed improves performance. Whereas most matching schemes are less effective at higher ratios, this method is more effective. Section III highlights some important properties of ordered elements. Section IV shows how grouping the ordered elements and reordering them can improve matching even more. Section V uses the introduced concepts to improve the INL of a 17 level D/A converter from 10 bits to more than 15 bits. Finally, section VI shows how to determine the relative sizes of the elements.

II. STRATEGIC ELEMENT PLACEMENT

A. Average mismatch cancellation

Performance can be increased substantially if the relative sizes of the devices are known. Consider, for example, the simple 1.5-b MDAC in Fig. 1 [9]. We can improve the gain error tolerance by arranging the capacitors so that the mismatch error of the top pair is of the opposite sign of the bottom pair. This is done by picking the top feedback capacitor to be the larger of the two top capacitors, and the bottom feedback capacitor to be the smaller of the two bottom capacitors. As will be shown in section VI, the capacitor relative size can be determined using the op-amp.

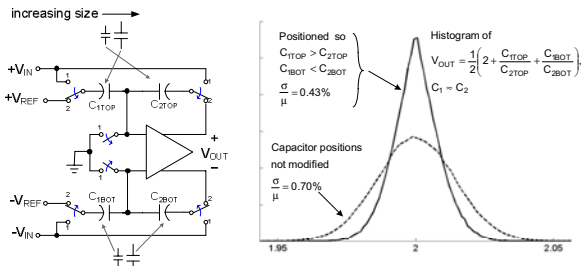

Figure 1. Fully differential gain of two circuit and the reduced spread when the capacitors are arranged based on relative size. The factor of 1.6 improvement in matching means that capacitors can be 2.56x smaller.

As Fig. 1 shows, this simple change in configuration makes the distribution much peakier. At the 98 percentile, the spread is reduced by a factor of 1.6. To get this same spread without sorting one would have to increase the size of the capacitors by a factor of $(1.6)^2 = 2.56$. The power would also have to be increased by at least the same factor to maintain the same speed. The distribution was determined with Monte Carlo simulations, although in this case it could have been derived by convolving two half-Gaussian distributions.

B. Selecting the median device

The procedure works even better when higher ratios are desired. This is very fortunate because achieving accurate high ratios is difficult because the mismatch is largely determined by the smallest element (C_2 in Fig 2). As a result, the other element (C_1) must be must larger than would normally be required based on matching considerations alone. However, if one is able to *choose* which device is used for C_2 the matching performance increases substantially as the number of choices is increased. This makes sense since more choices will increase the odds of finding a well matched

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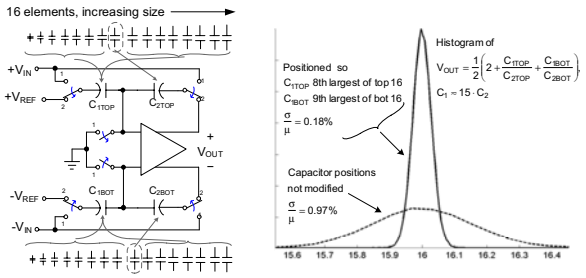

Figure 2. Gain of sixteen circuit and the reduced spread when the feedback device is choosen to be the median element of the ordered devices. Capacitors can be made nearly 30x smaller when this is done.

device. One application of this is shown in Fig. 2, which is a gain of sixteen circuit. As can be seen, the spread is reduced by a factor of 5.3 when the feedback device is chosen based on the relative sizes of devices. This means capacitors 1/30th the size can achieve the same matching performance as unordered devices.

Ideally, the feedback device would be chosen to be the one closest to the mean value of the other devices. This cannot be found if we only know the relative device sizes; however, the *median* device is easily found from an ordered set as it will rank half-way, and using this device gives very good results.

The circuits in Fig.1 and Fig. 2 have an even number of elements so a single median device does not exist. This case is easily handled by choosing the devices as shown in Fig. 2. The top feedback device is the 8th largest of 16, whereas the bottom feedback is the 9th largest of 16. While each choice will give a mean error, the errors are of the opposite sign and cancel.

C. Other applications

The popular op-amp sharing topology (Fig. 3) [5] allows one to take advantage of ordering with little added complexity. To do this, one would rank the four upper capacitors from smallest to largest and choose the first stage devices to be the second and third largest devices (i.e. the middle devices). This will be repeated for the bottom four devices. As in the previous examples, the mismatch of the top pair will be the opposite sign of the mismatch of the bottom pair. Doing this will decrease the spread by a factor of 2.6 for the first stage, and 1.6 for the second stage. The second stage will have greater mismatch than the first stage since it uses the

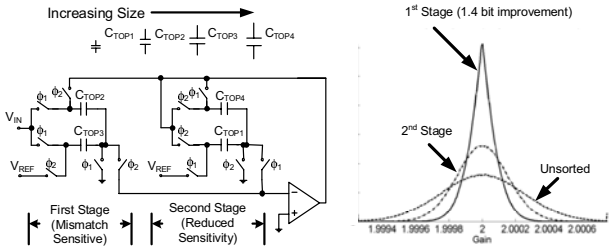

Figure 3. Op-amp sharing topology that allows for reduced spread by choosing the first stage capacitor pair from a group of four devices. No sub-elements are used in this example.

outliers. This is acceptable because the second stage has less stringent matching requirements than the first stage. The net effect is a 1.4 bit improvement in matching with little overhead. The ΔVgs (β multiplier) bias [10] and bandgap references are other applications where it would be desirable to select the median device to decrease spread from mismatch.

III. Order Statistics

A. Properties of ordered elements

For the purposes of this paper, the form of an ordered (i.e. sorted) array of length 2*N will be

$C_{-(N)}, C_{-(N-1)}, \ldots C_{(N-1)}, C_{(N)}$,

where $C_{-(N)}$ is the smallest device, $C_{-(N-1)}$ is the second smallest device, etc. If the length of the array is 2*N+1, the center (median) device will be denoted as C_0. There are three important properties of sorted (ranked) devices chosen from a population of normally distributed devices.

1) Sorting reduces the standard deviation of the devices. That is, one knows the size of the ith element of an array with more certainty if the array is sorted.

2) With respect to C_0, the mean value of the ith largest has the opposite sign of the ith smallest (aka -ith) device. That is, $E(C_{-(i)} + C_{(i)}) = C_0$, where E is the expected value operator.

3) The middle devices have a lower standard deviation than the devices towards the endpoints of the array.

Properties 1-3 are shown graphically in Fig. 4 for a normally distributed random variable with 100,000 Matlab Monte Carlo simulations. Note that the plots are normalized to a mean value of zero and a standard deviation of one.

The practical use of the second property is that we can group the ith device with the -ith device and construct a composite capacitor with much better matching properties than if we had simply doubled the area. It also follows that multiple devices could be constructed. For example, one could create four well matched devices by sorting eight elements and grouping the ith and the -ith devices together. Further improvement could be expected if the four devices were sorted and grouped again, producing a single pair of devices. The sequence to do this is shown in Fig. 5.

The consequence of the third property is that, *if possible*, the critical capacitors should be selected from the middle devices of a sorted array. (In fact, significant reduction in

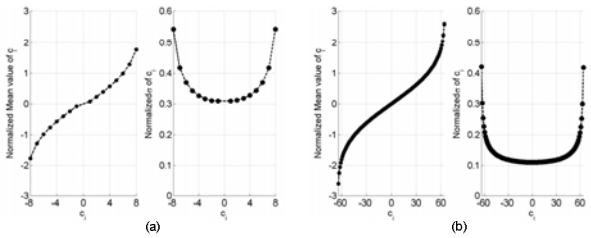

Figure 4. The expected mean and standard deviation of an (a) 16element sorted array, (b) 128 element array.

standard deviation can be achieved by simply *not using* five or so outliers, although this isn't done in this paper.) Using the middle devices for the more critical first stage MDAC was illustrated earlier in Fig. 3. Further improvement can be obtained by sorting and grouping more elements to create the capacitors, before setting their positions. This is explained in the next section.

IV. SORTING AND GROUPING

A. Better matched pairs using subelements

The term sorting and grouping was used by Cong to describe a method to reduce D/A converter integral nonlinearity (INL) [8]. This work improves that methodology significantly by using a simpler sorting routine, and repeated applications of it to eliminate nonlinear gradients.

Sorting and grouping arranges devices so that their mismatches tend to cancel. For example, if four devices are sorted from smallest to largest we can construct an improved matched pair by grouping the smallest and largest together for one capacitor, and make the second capacitor from the two middle capacitors. This improvement can be predicted by the use of order statistics [7]. However, it is much more practical to use Monte Carlo simulations to investigate the properties because order statistics does not generally provide closed form solutions for these problems.

Fig. 5 shows how sorting and grouping can be used to construct two well matched devices from 8 devices. Fig. 6 shows the improvement when sorting and grouping is used to create the matched capacitors for the circuit in Fig. 1. The upper left point corresponds to the factor of 1.6 improvement described in section II-A. As can be seen from Fig.6, the spread is inversely proportional to the number of elements used. This result is NOT from increased area – the total capacitance is kept the same for each case. In other words, matching is significantly improved by breaking a capacitor into many small pieces and using sorting/grouping methods to construct a matched pair.

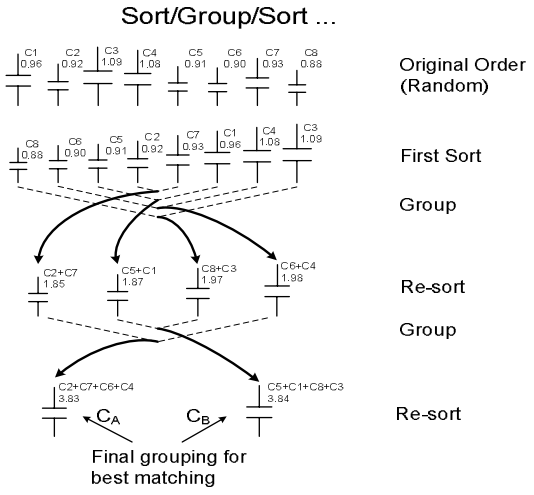

Figure 5. Sort and group operations to create two well matched capacitors from 8 sub-elements.

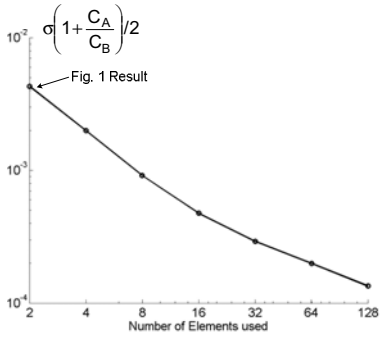

Figure 6. Reduction in σ obtained for the circuit in Fig. 1 when the capacitor is broken into subelements and sorted. Spread is roughly inversly proportional to the number of subelements used, even though total capacitor area stays the same.

B. Improved D/A Converters

The sorting and grouping operation orders elements well for use in very linear thermometer coded D/A converters. Such D/A converters would be valuable for Nyquist-rate or low over-sampling-ratio applications where data weighted averaging [4] does not work well. The final order of capacitors in a nine-level thermometer coded D/A converter is shown in Fig. 7. Different ordering schemes such as switching the direction of the sort after each grouping, or repeated usage of the ordering presented in [8], can offer small improvements in special cases.

V. A HIGHLY LINEAR 17 LEVEL D/A CONVERTER

The principles described in this paper were used to design the highly linear 17 level D/A converter shown in Fig. 8. The results were simulated with MATLAB. The histograms show that the baseline INL performance is about 10 bits when the 32 unit capacitors per side are unordered (i.e. traditional configuration). Ordering these capacitors in addition to using the outliers for the less critical feedback capacitor adds 3 bits of linearity. Another two bits can be obtained by using

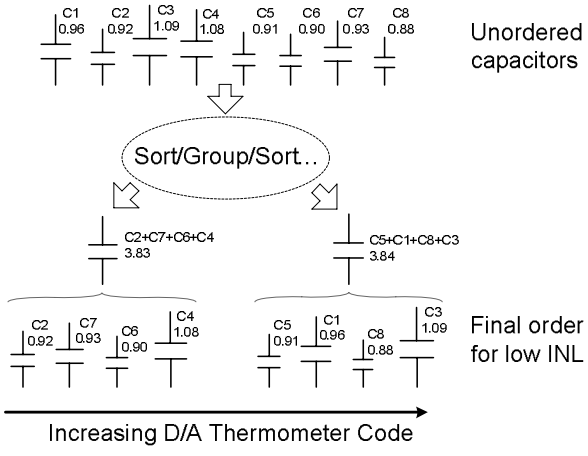

Figure 7. Using the sorting and grouping algorithm to order elements for a highly linear nine level D/A converter.

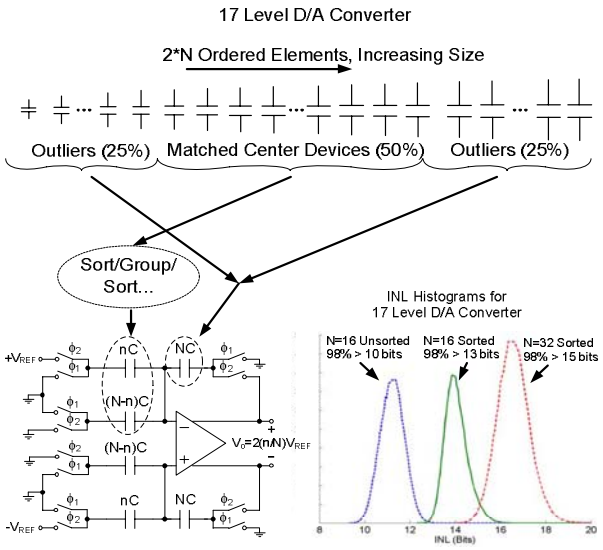

Figure 8. Highly linear 17 level D/A converter and INL histograms. Unordered capacitors limit INL to 10bits (98% yield). Simple ordering (Fig. 6) the same capacitors increases linearity by 3 bits. Further improvement is obtained by creating a 33 level (N=32) D/A converter, and only using the even levels. Total capacitance is the same for all three D/A converters.

64 half-sized unit capacitors instead of 32. To get the same INL performance, capacitance area would need to be increased by a factor of 1024. Further performance increases could be expected using 128 quarter-sized unit capacitors, etc.

VI. Capacitor Sorting Circuit

The operational amplifier can be configured to sort the sub-element capacitors from largest to smallest. This is done by comparing the relative size of each capacitor to the other capacitors. If there are N capacitors, it will take N*(N-1)/2 comparisons to completely characterize the array if all possibilities are checked. Bubble sorts, etc. can be used to sort the array with less comparisons.

A circuit to compare sub-element capacitors C_1 and C_2 is shown in Fig. 9. It has two phases. The first phase autozeros the op-amp offset and pre-charges C_1 and C_2 to $-V_{REF}$ and V_{REF} respectively. Phase two reverses the polarity of the charge, and if C_2 is larger than C_1, the voltage at the inverting node of the op-amp will increase. Accordingly, the op-amp will function as a comparator and output a logic zero. A counter register corresponding to C_2 will then be incremented. This procedure will be repeated to check all permutations of the top-half capacitors. The procedure will be repeated for the bottom-half capacitors. At the end, each counter register will contain the rank of its respective capacitor.

C_3 and C_4 are necessary to negate the effects of charge injection. They are nominally equal to C_1 and C_2. Noise of the operational amplifier will limit the measurement accuracy, but one would expect the noise performance of the amplifier to be

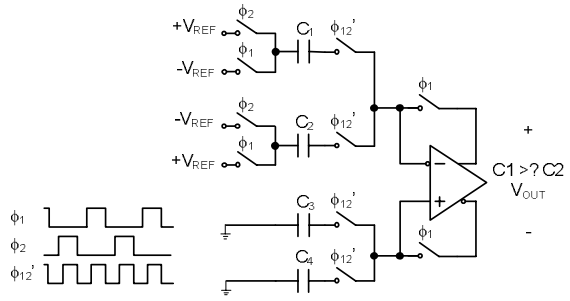

Figure 9. Capacitor ranking circuit created using existing operational amplifier.

at least as good as the desired capacitor matching, or there would be no benefit to increased matching. Slower rate measurements, or multiple measurements could be taken with a majority vote strategy to reduce noise.

VII. Conclusions

The effects of component mismatch can be reduced using relative size information. When done, these components can match as well as components orders of magnitude larger. Sorting can be done by comparing each capacitor to the others in an array. This is possible using the op-amp present, and will take N*(N-1)/2 operations to sort N capacitors.

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