LOW-VOLTAGE SWITCHED-CAPACITOR CIRCUITS

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1. ABSTRACT

Switched-capacitor stages are described which can function with very low (typically 1 V) supply voltages, without using voltage boosting or switched op-amps. Simulations indicate that high performance may be achieved using these circuits in filter or data converter applications.

2. INTRODUCTION

One of the key limitations of state-of-the-art fine linewidth CMOS technologies is the restricted power-supply voltage, limited by the low junction-breakdown voltage of the process and by the thin gate oxide, prone to voltage stress and breakdown. Also, in some applications, the available external power source may limit the supply voltage; for example, this source may be a 1.2 V battery, with an end-of-life voltage of only 0.9 V.

In analog and mixed analog-digital circuits, the circuit technique most often used for analog signal processing is based on switched-capacitor (SC) stages. They can be utilized in many applications, such as data conversion (both in Nyquist-rate and oversampled $\Delta\Sigma$ ADCs), analog filters, sensor interfaces, etc. However, there are fundamental limitations on the operation of switches when the supply voltage becomes less than the sum of the absolute values of the PMOS and NMOS threshold voltages [1]. Specifically, if a switch is connected to a signal voltage, which is about half-way between the rail voltages, and $V_{Tn}+|V_{Tp}| > V_{dd}$, it may not be possible to turn the switch on, even if a CMOS transmission gate is used to realize it.

In the past, two approaches have been commonly used to bypass this problem. One used internal voltage boosting (typically, doubling) to obtain high-swing clock signals [2]. This approach is useful if the supply voltage is restricted by the source, as in the case of battery-operated devices, or by the junction breakdown only. However, it cannot be used if the gate oxide deterioration limits the permissible supply voltage. The other alternative was the use of switched op-amps [3]. This approach also suffers from some shortcomings. Specifically, the transients introduced by the required power-up/power-down of the op-amp slow down the operation, increase the required settling time, and thus reduce the speed of the circuit.

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In this paper, we propose a third approach to realize low-voltage SC circuits. It is based on the use of a novel integrator architecture, illustrated schematically in Fig.1a, which shows two cascade integrators. The clock phases are shown in Fig.1b. Note that the four switches needed for the conventional integrator stage are replaced by the two grounded switches S_A and S_B in this circuit. This architecture was suggested earlier [4] for reducing the offset and 1/f noise in SC filters. In this circuit, the op-amp remains in its high-gain region during reset, and hence recovers rapidly when $\Phi 2 \rightarrow 1$.

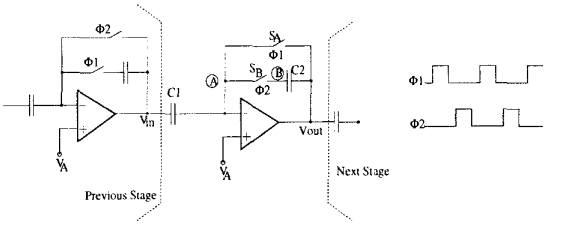

Figure 1: (a) Low-voltage SC integrator (b) Clock phases

A straightforward implementation of the stage of Fig.1a would introduce practical problems due to forward-biased p-n junctions in the S_B switches. The operation of the circuit, and the practical problem mentioned above, will be described in Sec.3. Several techniques for its solution will be discussed in Secs.4-6. The application of the improved integrator stage in a SC filter and a $\Delta\Sigma$ ADC will be discussed in Sec.7.

3. THE OPERATION AND IMPLEMENTATION OF THE LOW-VOLTAGE INTEGRATOR

It is easy to show that when $\Phi 2 = 1$, the circuit of Fig.1 satisfies the appropriate equation for an inverting delay-free integrator. Notice that v_{in} is the output voltage of the preceding stage, which has the same architecture. Hence, if the preceding stage has the same switching sequence as the one analyzed, then $v_{in}(n-1/2) = V_A$, while $v_{in}(n)$ is the output signal voltage of the preceding stage. If the S_A switch of the previous stage is closed during $\Phi 2 = 1$, and its S_B is closed during $\Phi 1 = 1$, then the output voltage of the cascade is inverted and delayed.

Note that (at the cost of two additional switches) the right-hand terminal of *C1* can be disconnected from the virtual ground

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and grounded during the $\Phi 1 = 1$ period. Note also that some discussions in this report refer to single-ended circuit realizations. In reality, the implementations planned will be mostly fully differential (or at least pseudo-differential [5]) structures, to achieve better noise immunity.

As mentioned in the Introduction, the obvious realization of the circuit of Fig.1 leads to some practical difficulties. Assume that the analog ground voltage is $V_A = V_{SS} = 0$, i.e., that the input common-mode voltage is true ground, as may be the case if the op-amps have PMOS input devices. Then the conventional realization of the circuit calls for NMOS switches for both S_A and S_B, since NMOS devices are easy to turn on when they operate at ground bias. Assume also that the output voltage at the end of a $\Phi 2 = 1$ period approaches V_{dd}. Then, at the beginning of the next $\Phi 1 = 1$ phase, V_{out} is pulled down to ground by S_A, and the floating node B (between S_B and $C2$) is pulled down to about $-V_{dd}$ by $C2$. Since node B is connected to the n+ source diffusion of S_B, the source-to-substrate junction of S_B will be forward biased, and $C2$ will lose charge to the substrate.

In what follows, several techniques for avoiding the forward-biased junction problem will be described.

4. INTEGRATOR REALIZATION USING A PMOS SWITCH AND LEVEL-SHIFTED CLOCK

A possible solution to the junction leakage problem is illustrated in Fig.2.

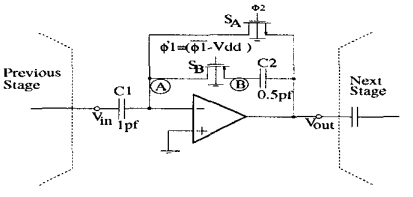

Figure 2: Low-voltage integrator with MOS switches

As before, the circuit uses an NMOS implementation for S_A, but now a PMOS device is used as S_B. Clearly, now the voltage drop from 0 to $-V_{dd}$ at node B will reverse bias, not forward bias, the source-to-well junction. Hence, the charge loss from $C2$ is avoided.

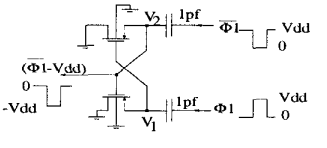

Figure 3: Level-shifted clock generator

The remaining problem is that the grounded PMOS switch device requires a negative clock voltage for conduction. A level-shifting circuit which can realize this is shown Fig.3. It is a variant of the widely-used Nakagome clock-booster stage [6]. It provides a clock signal varying between 0 and $-V_{dd}$. At power-up, the first few samples will be positive, leading to charge pumping into the well from the sources of the PMOS switches. This should not be a problem as long as the well is adequately grounded. After the third or fourth clock periods, the samples of V1 and V2 become negative, and the charge pumping stops. As an illustration of the

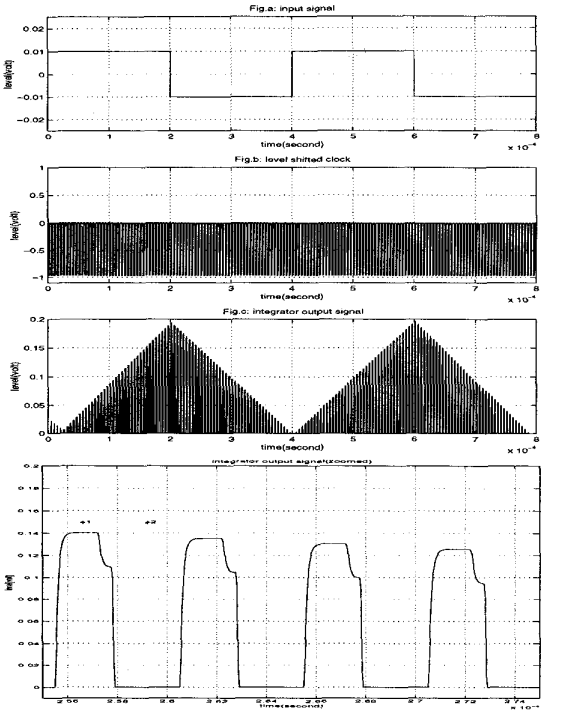

Figure 4: Simulated voltages in the integrator of Fig.3: (a) input; (b) clock; (c) output voltage; (d) output voltage on an expanded time scale

integrator operation, Fig.4 shows the simulated input, clock, and output voltages of the circuits of Figs.2 and 3, under the following test conditions: $C1 = 1$pF, $C2 = 0.5$pF and $V_{dd} = 1$ V.

The input voltage was a 2.5-kHz, 20-mV p-p square wave, and the clock frequency was 200 kHz. A simple macromodel was used for the op-amp. It corresponds to a dc gain of 3000 and a unity-gain bandwidth of about 2 MHz. The models used for the switches were realistic Level 13 HSPICE ones.

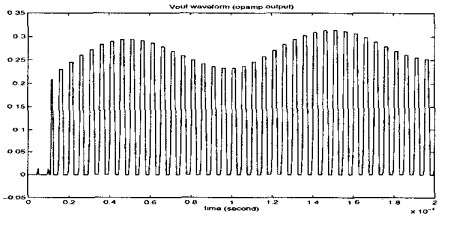

Figure 5: Simulated waveforms for a sine-wave input signal

Fig.5 shows the simulated waveforms for a 10-kHz, 20-mV p-p sine-wave input signal, under the same conditions. The waveform includes the power-up transient around $t = 0$.

5. INTEGRATOR REALIZATION USING A FLOATING VOLTAGE SUPPLY

An alternative realization, which also avoids charge leakage, is shown conceptually in Fig.6. This circuit can be implemented us-

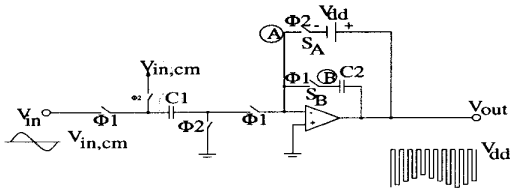

Figure 6: Low-voltage integrator using a floating bias supply

ing only NMOS switches, since when S_A closes the output voltage rises to the reset voltage V_{dd} (rather than drop to 0 as in the previous realization), and hence the voltage at node B cannot fall below 0 V. Thus, the source-to-substrate junction of S_B remains reverse-biased under all conditions. A more detailed circuit diagram, showing also the implementation of the floating V_{dd} source in the form of the switched capacitor $C3$, is illustrated in Fig.7. It is also possible to implement a floating voltage source $V_{dd} - V_{DSAT}$, which allows the op-amp to retain a high gain during reset. This results in faster recovery.

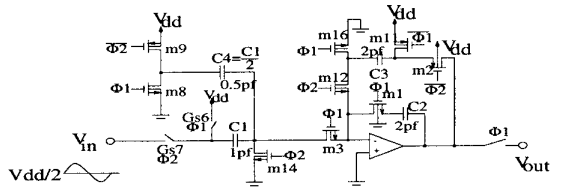

Figure 7: A possible implementation of the floating-supply integrator

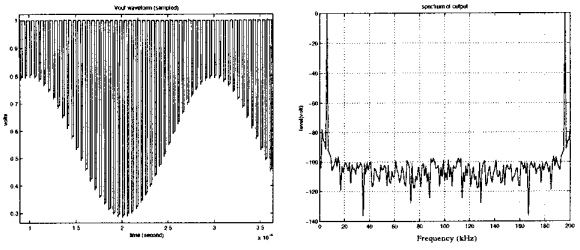

Figure 8: Simulated output in the time- and frequency-domain for the floating-supply integrator

Note that the dc bias of the input signal is assumed in Fig.7 to be $V_{dd}/2$, and hence a compensating branch, realized by the SC branch containing $C4$, is needed to prevent the output from ramping down due to the accumulation of this input bias. Fig.8 shows the simulated time- and frequency-domain representations of the output voltage of the integrator stage of Fig.7 for a 5-kHz, 0.2-V p-p sine-wave input voltage, under the following conditions. The capacitances were $C1$ = 1pF and $C2$ = 2pF, and V_{dd} was 1V. The op-amp model was as before, and the switch models were HSPICE Level 13.

6. INTEGRATOR REALIZATION USING MASTER/SLAVE INTEGRATORS

Yet another technique for avoiding charge leakage in the low-voltage integrator of Fig.1 is to use an extra op-amp stage (slave integrator) for storing the charge during the reset phase when the integrating capacitor is floating. Fig.9a shows the schematic diagram of the circuit; Fig.9b illustrates the clock phases. When Φ2 and Φ2' rise, the signal charge stored in the master storage element $C_{integrator}$ is transferred into the slave storage capacitor C_{slave}; when clock phases Φ1 and Φ1' rise, the charge is returned into $C_{integrator}$. The sensitive nodes A and B are kept at or near the analog ground, and charge leakage is thereby prevented. This

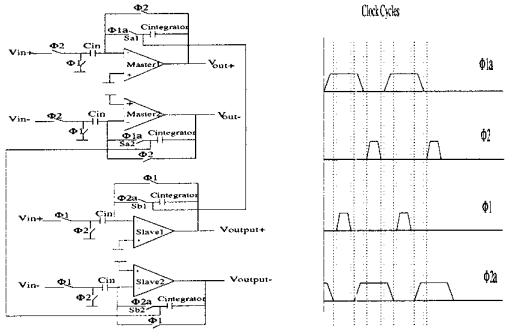

Figure 9: Master/slave integrator scheme (pseudo-differential implementation

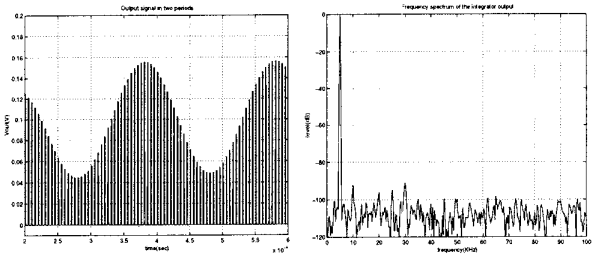

Figure 10: (a) Output voltage (b) Output spectrum

stage can use single-channel (NMOS) switches everywhere, since all switches operate at analog ground potential. A drawback of the master-slave structure is the need for the second integrator stage. However, it is possible to operate the structure in a double-sampling mode, in which both integrators receive input charges in alternating clock periods. For such a "ping-pong" circuit, the sampling rate can be doubled without increasing the op-amp bandwidth. The performance of this integrator was simulated using HSPICE. A macro model, corresponding to a dc gain of 80 dB and a unity-gain frequency of 100 MHz was used for the opamp. All capacitors were chosen as 2 pF. The switches were simulated by the Level 13 model in HSPICE. Their dimensions were L = 0.6 um and W = 10 um. The sampling frequency was 200 kHz. A 20-mV p-p 5-kHz sine wave was used as input signal. Fig.10a shows

the output voltage over two periods; Fig.10b illustrates its spectrum. The low harmonic distortion verifies the absence of charge leakage.

7. EXAMPLES OF LOW-VOLTAGE SC CIRCUIT IMPLEMENTATIONS

Fig.11 illustrates a biquad stage constructed from the low-voltage integrator of Fig.2. (Even though a fully differential configuration is shown, for very low supply voltage a pseudo-differential implementation may be necessary.) It was used to realize the transfer function:

$$H(z) = -\frac{z^{-2} - 1.3672z^{-1} + 1}{z^{-2} - 2.2354z^{-1} + 1.3228} \qquad (1)$$

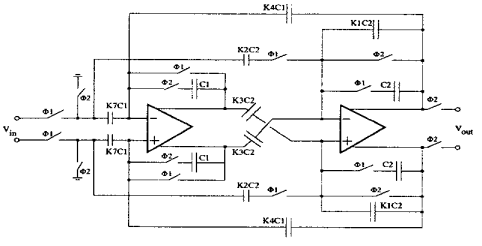

Figure 11: SC biquad using the low-voltage integrator of Fig.3

Note that the input switches cannot be directly implemented for a low voltage technology. A possible solution is to connect the input terminals to virtual grounds via resistors and to use a SC branch like the one with $C4$ in Fig. 7 to have $Vdd/2$ compensation.

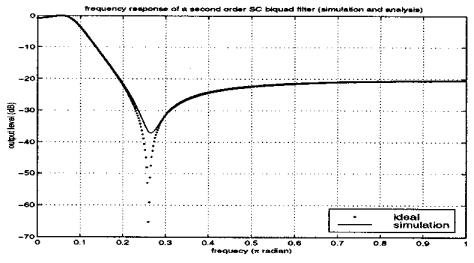

Figure 12: SC biquad filter simulation and analysis results

Figure 12 compares the simulated response of this filter with the ideal one. The clock frequency is 200 kHz.

A complete circuit realization of a differential $\Delta\Sigma$ A/D converter, using the integrator of Fig.2, is shown in Fig.13.

To verify the operation of the delta-sigma circuit, it was simulated using HSPICE under the following conditions: sampling frequency f_s = 200 kHz, sine-wave input signal frequency f_i = 781.25 Hz, and op-amp model the same as before. The simulated output spectrum (Fig.14) is that of a nearly ideal second-order delta-sigma modulator, indicating that the circuit is likely to operate successfully if properly designed and fabricated.

8. CONCLUSIONS

A set of new low-voltage switched-capacitor circuits were presented. The circuit details show that all transistors stay within the specified voltage operations of a given technology (i.e. voltages across junctions and gate oxide never exceed V_{dd}). These techniques apply directly to filters and data converters as briefly shown in Section 6. Even though the discussions were confined to op-amps with $0 \rightarrow V_{dd}$ output swing, the virtual ground potential and supply voltage (V_{dd}) can easily be modified to keep the op-amp output swing limited in order to keep it from saturating.

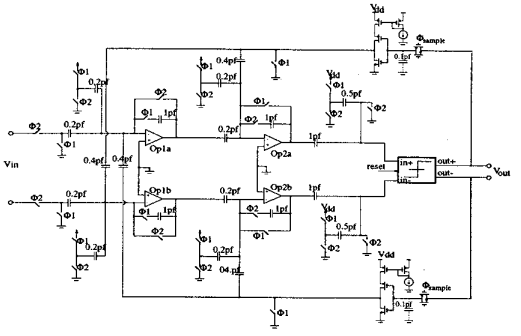

Figure 13: 1-V power supply $\Delta\Sigma$ ADC

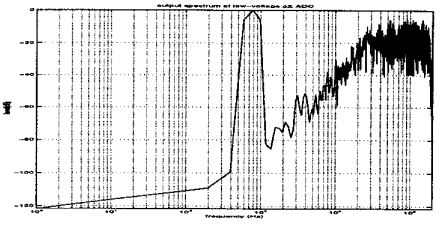

Figure 14: Output spectrum of low-voltage $\Delta\Sigma$ ADC

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