CAPACITOR MISMATCH ERROR CANCELLATION TECHNIQUE FOR A SUCCESSIVE APPROXIMATION A/D CONVERTER

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ABSTRACT

An error cancellation technique is described for suppressing capacitor mismatch in a successive approximation A/D converter. At the cost of a 50% increase in the conversion time, the first-order capacitor mismatch error is cancelled. Methods for achieving top-plate parasitic insensitive operation are described, and the use of a gain- and offset-compensated opamp is explained. SWITCAP simulation results show that the proposed 16-bit SAR ADC can achieve an SNDR of over 91 dB under non-ideal conditions, including 1% 3σ nominal capacitor mismatch, 10-20% randomized parasitic capacitors, 66 dB opamp gain, and 30 mV opamp offset.

1. INTRODUCTION

Switched-capacitor data converters commonly suffer from the finite matching accuracy of capacitors. A variety of techniques have been proposed to minimize this problem, such as mismatch-shaping [1]-[4] and first- order mismatch error cancellation [5].

In this paper, another capacitor mismatch error cancellation technique is proposed in the context of a successive-approximation ADC. In the proposed technique, the first-order error is cancelled at the cost of 50% increase in the conversion time, instead of the two-fold increased described in [5]. In the context of a SAR ADC, the N clock cycles nominally required for an N-bit converter are increased to 1.5 N clock cycles. In the example to be presented, 24 cycles are required for a 16-bit SAR ADC.

One of the novel aspects of the proposed technique is that while the error cancellation is carried out, opamp gain boosting as well as opamp offset cancellation also occurs. This allows the usage of a lower-gain wider-bandwidth opamps, while ensuring high-accuracy data conversion. The error cancellation technique also absorbs any small error that may ordinarily be caused by top-plate parasitic capacitors.

2. SUCCESSIVE-APPROXIMATION ADC AND DAC ARCHITECTURES

A general block diagram of a SAR ADC is shown in Fig. 1a. In operation, the sampled input voltage is continually compared to the output of the internal DAC. For a given input sample, V_{in} is only acquired once in a conversion period, and the conversion takes place in N cycles (for an N-bit converter). According to the digital output (high or low) of the comparator, the successive-approximation register(SAR) selects the DAC's input data/bits. Operation starts with finding the MSB in the first clock cycle, then progresses down to the LSB at the last (N-th) clock cycle. Fig. 1b illustrates a possible scenario for an input sample.

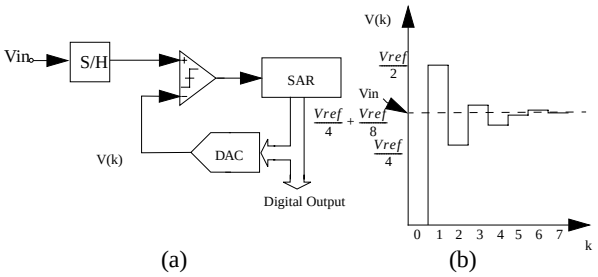

Figure 1: General successive-approximation ADC

In a SAR ADC, the internal DAC plays a critical role, as the accuracy of the converter is mainly defined by the DAC's accuracy. Therefore, it is essential that any error that may originate from the DAC be avoided. The proposed DAC is shown in Fig. 2. The nominal value of all capacitors are the same. The operation is as follows. (Assume, for now, that the opamp gain is very high and the offset is zero.) At the beginning of the conversion cycle, the capacitor C_1 is initially precharged to $-Vref$, and C_f and C_2 are discharged. In the first clock cycle after the initial reset, capacitors C_1 and C_2 share the charge that was stored on C_1, while dumping an equal and opposite charge into integrating capacitor C_f. This occurs if the data is *high* (MSB=1 as controlled by the SAR), and $\phi_x = \phi_1$. If the data is *low* (MSB=0), the ϕ_x switch stays open and the ϕ_y one closes instead. During the second phase ϕ_2, C_2 is discharged and the charge on C_1 (which is now half of what it had previously) is preserved. The following data bits con-

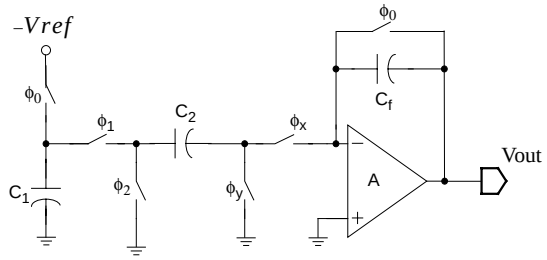

Figure 2: Two-capacitor charge-redistribution DAC

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trol the same set of operations. For an N-bit converter, the final DAC output is reached after N clock cycles (2N phases). For this simplified single-ended example, the output range of the structure is 0 to $Vref$.

3. CAPACITOR MISMATCH ERROR

For the DAC's operation described in the above, the capacitor mismatch between C_1 and C_2 has a direct impact on the linearity of the overall converter. If the mismatch between the two capacitors is described by $\alpha = (C_2 - C_1)/(C_2 + C_1)$, the errors occurring in the DAC may be fully described in terms of α. (The polarity of α is unimportant as long as it is fixed.) First consider the operation outlined in Fig. 3a. Given that the charge initially stored on C_1 in ϕ_1 is q, the amount of charge transferred to C_{int} during next ϕ_2 is $-q/2(1+\alpha)$, equal and opposite to the charge on C_2. The charge remaining on C_1, on the other hand, is $q/2(1-\alpha)$. Thus, in the next cycle, the charge transferred to C_{int} during ϕ_2 is $\frac{q}{4}(1-\alpha)(1+\alpha) \cong \frac{q}{4}$. Next, we shall show how to manipulate the error contributions so that the total net error in a conversion period is suppressed.

4. ERROR CANCELLATION

The accumulation error given in the previous section relates to a specific operation, where the initial charge is always stored on C_1, and either C_1 or C_2 is connected to the virtual ground in the next phase, as the charge is shared between C_1 and C_2. The available choice of which capacitor retains the charge and which capacitor connects to the virtual ground provides additional degrees of freedom for how much error charge is injected into the integrating capacitor C_{int}. In the differential configuration, another degree of freedom exists, since the capacitors may be cross-coupled for changing the polarity of the charge transfer to C_{int}.

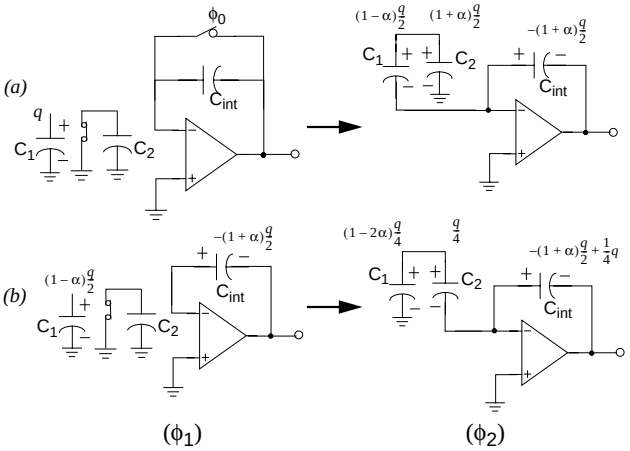

Figure 3: Capacitor mismatch error occurring in the DAC

From all capacitor switching possibilities for processing 2 bits, four optimal sequences are illustrated in Fig.4. The proposed capacitor mismatch error cancellation algorithm completes the desired task with each pair of data bits. After two bits of data (equivalent to three clock cycles due to 50% increase), the accu-

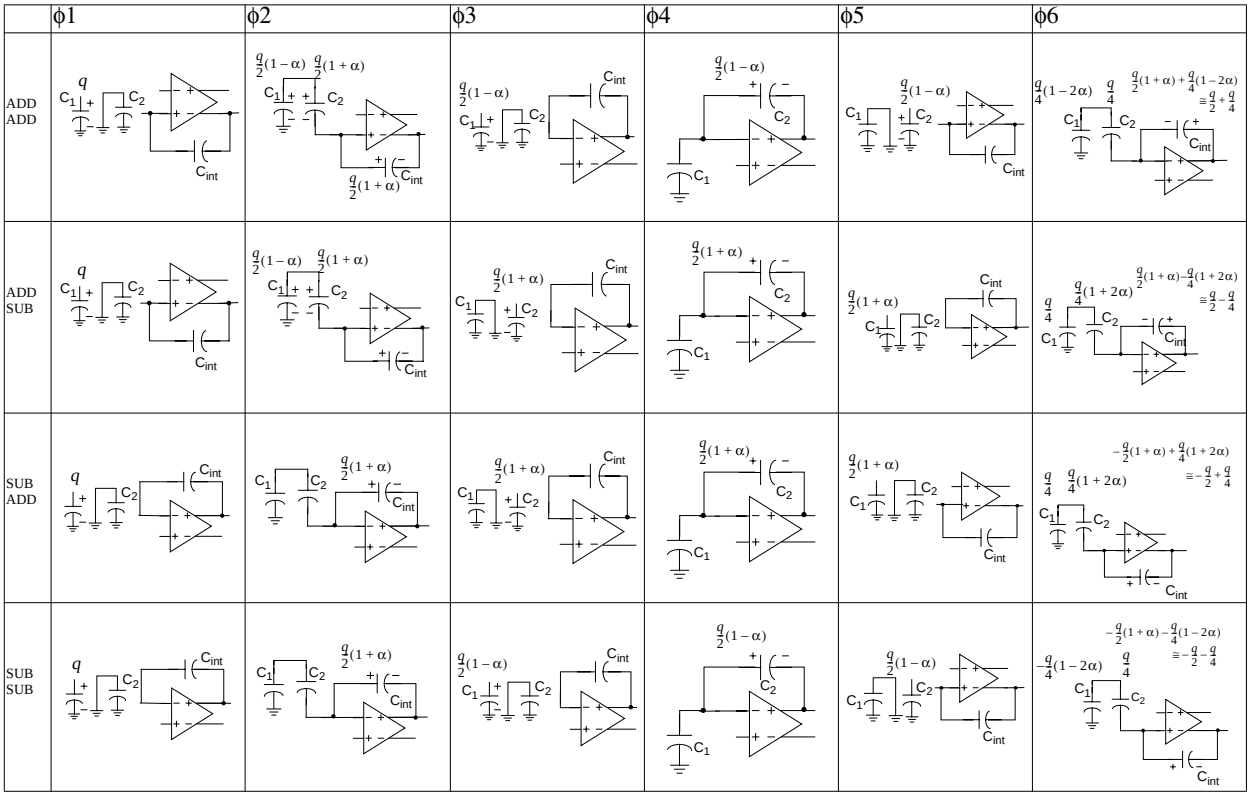

Figure 4: Switching sequences for proper cancellation

mulated error injected into C_{int} is to a first-order approximation equal to zero.

One important aspect of the steps specified in the four columns of Fig.4 is that the capacitor which connects to the opamp virtual grounds is always the same one throughout all three cycles. The appropriate polarity is controlled by either cross-coupling the capacitor connection to the opamp or making the connection in line. The reason for maintaining the use of the same capacitor is to avoid any error that may result from the top-plate parasitic capacitors. This is illustrated in Fig.5. Two examples of ADD and SUB operation are shown in the Figure. If the capacitors that connect to the opamp are interchanged, as shown in the upper portion of the figure, the charges transferred to C_{int} in the two cases (ADD and SUB) are

$$q\frac{c_2+c_{2p}}{c_1+c_{1p}+c_2+c_{2p}}\bullet\frac{c_1}{c_1+c_{1p}} = \frac{q}{2}(1+\alpha)\bullet\frac{c_1}{c_1+c_{1p}} \quad \text{(ADD)}$$

$$q\frac{c_2+c_{2p}}{c_1+c_{1p}+c_2+c_{2p}}\bullet\frac{c_2}{c_2+c_{2p}} = \frac{q}{2}(1+\alpha)\bullet\frac{c_2}{c_2+c_{2p}} \quad \text{(SUB)}$$

The additional terms resulting from the top-plate parasitic capacitors (C_{1p} and C_{2p}) will produce charge error when applied to the first-order cancellation algorithm. Even though the effect of the top-plate parasitic mismatch (more specifically, the mismatch of the ratios) may be small, any amount of mismatch of the order of the nominal capacitor mismatch (α) or greater can significantly degrade the error cancellation.

Shown in the lower portion of Fig.5 is the proposed scheme, following the rules specified in Fig. 4. Due to allowing only C_2 to connect to the opamp, the absolute value of the charge transferred to C_{int} in the two cases (ADD and SUB) are

$$q\frac{c_2+c_{2p}}{c_1+c_{1p}+c_2+c_{2p}}\bullet\frac{c_2}{c_2+c_{2p}} = \frac{q}{2}(1+\alpha)\bullet\frac{c_2}{c_2+c_{2p}} \quad \text{(ADD)}$$

$$q\frac{c_2+c_{2p}}{c_1+c_{1p}+c_2+c_{2p}}\bullet\frac{c_2}{c_2+c_{2p}} = \frac{q}{2}(1+\alpha)\bullet\frac{c_2}{c_2+c_{2p}} \quad \text{(SUB)}$$

The appropriate polarity of the charge transferred to C_{int} differentially is ensured by the cross-coupling option. The top-plate parasitic mismatch issue no longer exists with the proposed scheme. It can be shown that the term $C_2/(C_2+C_{2p})$ only contributes as an overall gain error of the ADC and does not degrade the converter's linearity.

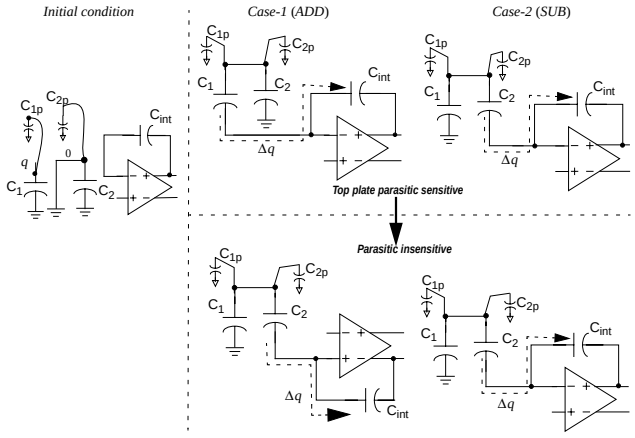

Figure 5: Top-plate parasitic insensitive technique

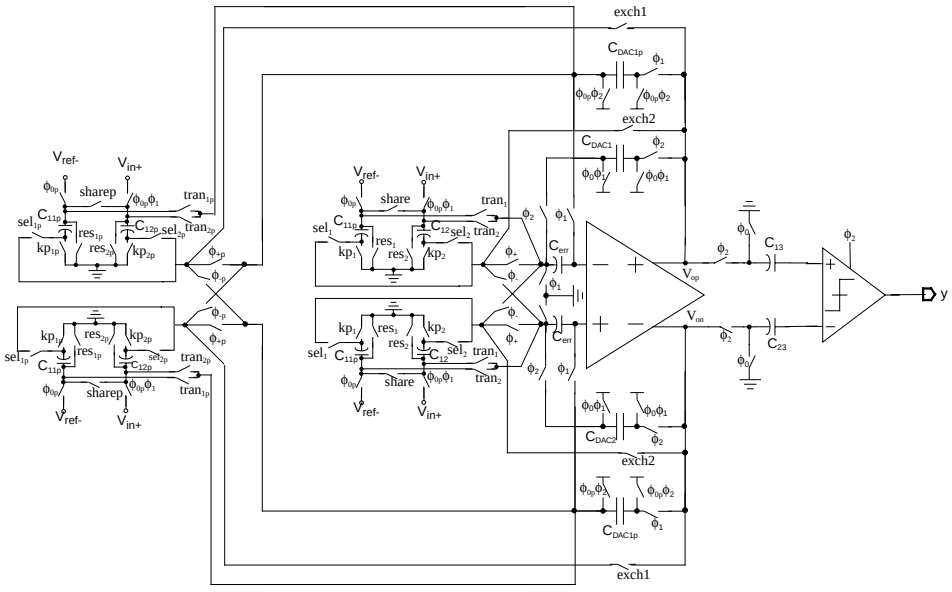

Figure 6: Differential GOC implementation

5. SIMULATION RESULTS

A 16-bit successive-approximation A/D converter was simulated using SWITCAP. Opamp gain and offset compensation utilizing predictive correlated double sampling (CDS) technique [6][7] was adapted for this ADC. As illustrated in Fig. 4, the opamp is not in use when ϕ_1 = 1. A set of nominally equal capacitors is used when ϕ_1 = 1 to predictively compensate for the opamp gain and offset before the real operations take place during ϕ_2 = 1. The fully differential implementation incorporating all techniques discussed is shown in Fig. 6. The digital circuitry including SAR and the algorithm- related control logic is omitted in this figure. Note that the input sample-and-hold (S/H) is incorporated into the DAC itself.

The following simulation results included a 1% 3σ RMS capacitor mismatch, 20% randomized bottom parasitic capacitors, 10% randomized top parasitic capacitors, opamp dc gain of 66 dB, and 30 mV opamp offset. A realistic clock feed-through model associated with the switches was also incorporated into the SWITCAP simulation. The results before and after the capacitor mismatch error compensation technique applied are shown in Fig. 7. The SNDR of 55.1 dB has improved to an SNDR of 91.1 dB.

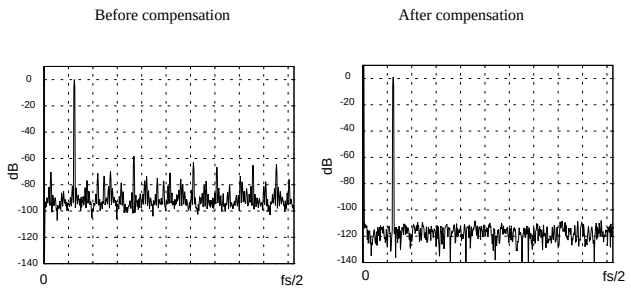

Figure 7: Output spectrum of SWITCAP simulation

6. CONCLUSION

A novel technique was proposed for algorithmically cancelling the capacitor mismatch error. The technique has been shown effective via SWITCAP simulation. This paper has addressed only one specific DAC structure for illustration, but other DAC structures may also achieve the same end goal. The proposed technique has been shown to suppress all capacitor mismatch errors to a first-order accuracy (virtually error-free for all practical purposes), and accounts even for the small top-plate parasitic capacitances. The implementation utilizes a predictive correlated double sampling technique to overcome errors resulting from finite opamp gain and opamp offset. Further study will address the issue of the charge injection occurring in the proposed structure, and will explore other structures such as pipeline ADCs.

7. ACKNOWLEDGEMENTS

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8. REFERENCES

[1] T. Brooks, D. Robertson, D. Kelly, A. Del Muro, and Sharston, "A 16b ΣΔ pipeline ADC with 2.5MHz output data-rate," *Dig. ISSCC*, pp. 208-209, Feb. 1997.

[2] R. Adams, K. Nguyen, and K. Sweetland, "A 113dB SNR oversampling DAC with segmented noise-shaped scrambling," *Dig. ISSCC*, pp.62-63, Feb. 1998.

[3] R. Schreier and B. Zhang, "Noise-shaped multibit D/A converter employing unit elements," *Electron, Lett.*, vol. 31, no. 20, pp. 1712-1713, Sep. 28. 1995.

[4] L. Hernandez, "Digital implementation of mismatch shaping in oversampled pipeline A/D converters," *Electron. Lett.*, vol. 34, no. 7, pp. 616-617, Apr. 2, 1998.

[5] P. Rombouts and L. Weyten, "A digital error-averaging technique for pipelined A/D conversion," *IEEE Trans. Circuits and Systems-II*, vol. 45, no. 9, pp. 1321-1323, Sep. 1998.

[6] G. Temes, Y. Huang, and P. Ferguson, Jr., "A high-frequency track-and-hold stage with offset and gain compensation," *IEEE Trans. Circuits and Systems-II*, vol. 42, no.8, pp. 559-561, Aug. 1995.

[7] Y. Huang, G.C.Temes and P. Ferguson, Jr., "Experimental results on reduced harmonic distortion with correlated double sampling," *Dig. of Symp. VLSI Circuits*, June 1998.