9.1 A 0.6V 82dB ΔΣ Audio ADC Using Switched-RC Integrators

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Low-voltage, low-power and medium-accuracy analog-to-digital converters (ADCs) are essential components in portable devices. Low-voltage operation of these ADCs poses three major challenges. First, the floating switches required in conventional switched-capacitor implementations are not operational for very low supply voltages. Second, reduced supply voltage translates to reduced signal power, mandating lower noise circuits. Third, the rail-to-rail input required to maximize signal power introduces added distortion in both the switches (due to signal-dependent ON resistance and charge injection) and amplifiers (due to limited output swing). Hence, low-voltage operation generally results in excessive power dissipation, and often requires voltage boosting [1] and/or bootstrapping [2]. In this paper, architectural and circuit techniques are proposed to overcome these problems, and a 0.6V 1mW delta-sigma audio ADC employing these techniques is presented.

The block diagram of the converter is shown in Fig. 9.1.1. A 2-2 MASH structure was adopted as it allows a low oversampling ratio (OSR = 64), thus reducing the power dissipation compared to lower-order systems operating at higher OSR. The first stage contains a low-distortion second-order loop [3], in which the loop filter ideally only processes quantization error, and therefore the amplifiers have relaxed distortion requirements. As opposed to a conventional MASH structure, no additional subtraction is required in the coupling between stages, since the second integrator output, V1, does not contain the signal. In order to maximize the input signal range without overloading the integrators, 1.5b local feedback was used [4], resulting in higher peak SNDR. Single-bit global DAC feedback was used for its inherent linearity.

Figure 9.1.2 shows the circuit diagram of the integrator of the first MASH stage. An example timing diagram illustrating the relationship between the DAC control signals (D1, D2) and the first-stage quantizer output (Y1) is also shown. As mentioned earlier, one of the major bottlenecks in low-voltage switched-capacitor (SC) circuit design is turning ON and OFF the floating switches. To circumvent this problem, the input SC branch of the conventional structure was replaced by a switched-RC (SRC) branch. The input floating switch in the conventional integrator was replaced by a resistor. This modification results in two major advantages. First, it obviates the need for the floating switch, and second, the input sampling linearity can be improved by making the linear resistor R1 much larger than the variable ON resistance of the reset switch (MSP, MSN). However, R1 should be small enough to satisfy the settling requirement during the sampling phase $\phi 1$.

In a conventional SC input sampling circuit, it is hard to maintain constant input common-mode bias during the sampling and resetting phases due to the limited signal range of the switches. The varying common-mode bias results in common-mode charge injection during each $\phi 2$ clock phase. In order to cancel this common-mode charge, an equal and opposite charge should be injected onto the integrating capacitors CI1 [5]. However, this requires additional SC branches, adding to the thermal noise from the switches. In the proposed architecture, split SRC branches were employed to suppress the input common-mode injection. This technique does not result in any noise penalty. During the $\phi 1$ phase, the input signal is sampled onto capacitors CS1 through resistors R1. The sampled charge is transferred to the integrating capacitors CI1 during the $\phi 2$ phase by connecting the bottom plate of each capacitor to VDD or VSS. A pseudo-differential architecture was used to circumvent the difficulty of realizing the common-mode feedback required in a fully differential amplifier operating at such a low supply voltage. Common-mode feedback using capacitors CM1 was used to maintain well-controlled output common-mode bias conditions. The output common mode is detected by utilizing the SRC input branches of the following stage.

Figure 9.1.3 illustrates the circuit diagram of the first stage of the delta-sigma ADC. A two-stage internally-compensated amplifier employing a folded-cascode first stage and a common-source second stage was used to achieve high gain and rail-to-rail operation. The input devices and the compensation capacitor were optimized for low-noise performance. SRC input sampling branches, similar to those in the integrators, were also used to realize the low-voltage comparator. An output offset cancellation technique was used to prevent overloading the integrator in the loop. The gain coefficients for the comparator inputs were implemented by scaling its input sampling capacitors. Output voltages from the second integrator drive the second stage directly. The second stage is similar to the first one, but does not require local feedback. Capacitor sizes and power consumption were scaled down in stages with lower noise and accuracy requirements.

The prototype ADC was fabricated in Asahi Kasei Microsystems 0.35μm CMOS technology, and occupies 1.8×1.6mm^2 active die area. Figure 9.1.4 shows the measured power spectrum of the output for a 1kHz, 0.57V peak-to-peak differential input sine wave, with a 0.6V power supply. Thanks to the low-distortion loop, 103dB SFDR was measured over the audio band. The SNDR versus input amplitude curve is illustrated in Fig. 9.1.5. In the 20kHz A-weighted band, the prototype achieved 81dB peak SNDR and 82dB dynamic range with a 0.6V supply voltage and 1mW power consumption. Similar performance (scaled up with the supply voltage) was achieved with supply voltages ranging from 0.6V to 1.8V. The performance is summarized in Fig. 9.1.6.

The die photograph of the prototype IC is shown in Fig. 9.1.7.

Acknowledgements:
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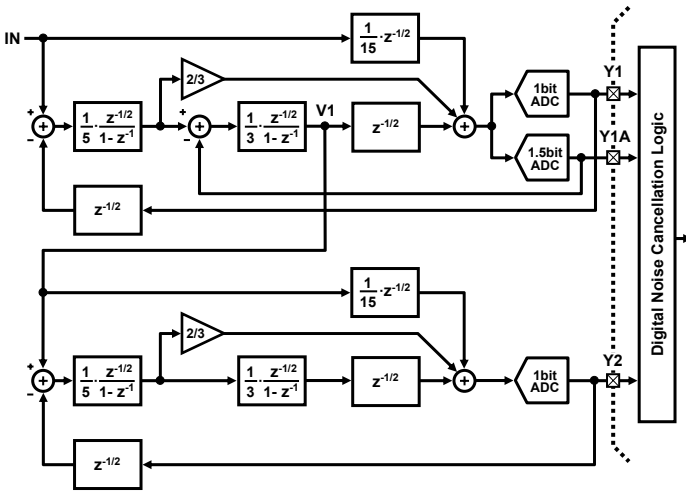

Figure 9.1.1: Block diagram of two-stage cascaded delta-sigma modulator.

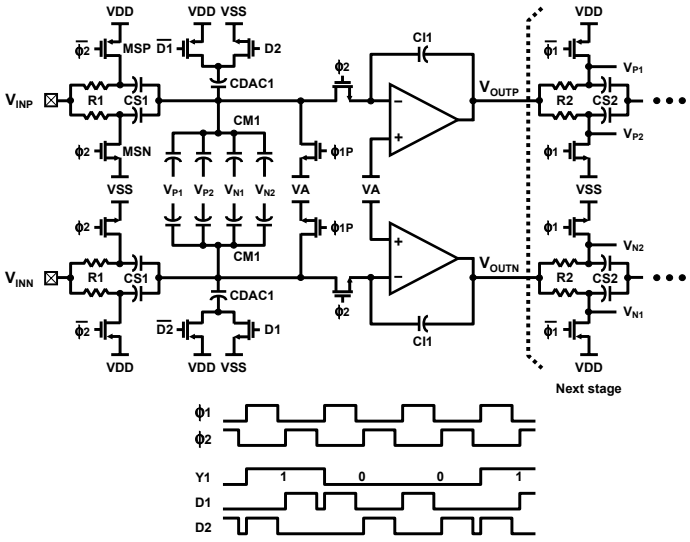

Figure 9.1.2: Low-voltage integrator with switched-RC technique.

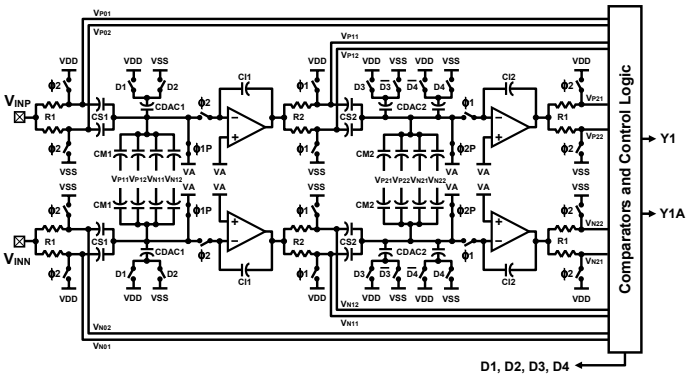

Figure 9.1.3: First stage delta-sigma modulator.

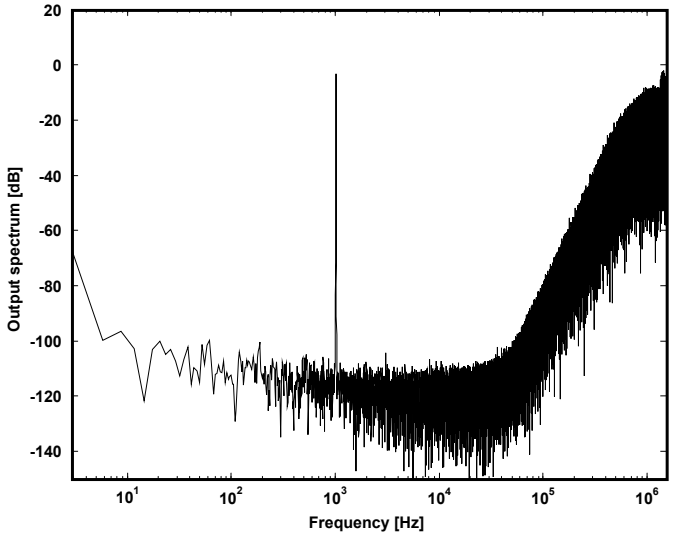

Figure 9.1.4: Measured output spectrum.

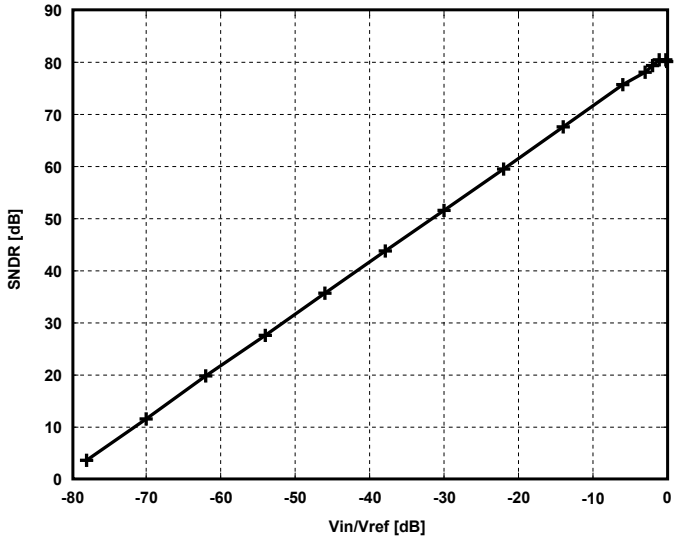

Figure 9.1.5: Measured SNDR.

Power supply voltage	0.6V
Signal bandwidth	24kHz
Clock frequency	3.072MHz
Oversampling ratio	64
Total power consumption	1mW
Input range	0.8Vpp (differential)
Peak SNR	77dB @ BW = 24kHz 78dB @ BW = 20kHz 81dB @ BW = 20kHz, A-weighted
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Dynamic range	78dB @ BW = 24kHz 79dB @ BW = 20kHz 82dB @ BW = 20kHz, A-weighted
Active die area	1.8 X 1.6 mm^2
Technology	0.35µm CMOS

Figure 9.1.6: Performance summary.

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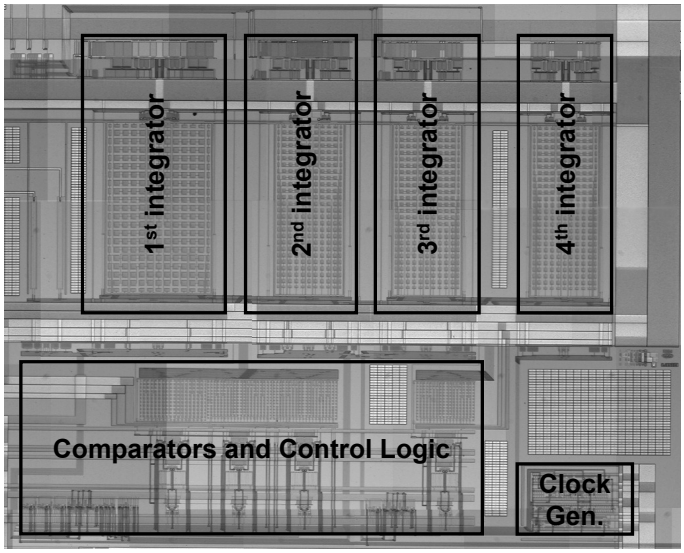

Figure 9.1.7: Die photograph.

