30.1 An Over-60dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp with 30dB Loop Gain

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Finite opamp gain and output swing are two limitations for precision analog circuits. These limitations are especially serious at lower supply voltages where limited headroom prevents the use of cascode devices to improve gain. The magnitude of the problem is illustrated in Fig. 30.1.1 for a 2-stage opamp in a 0.18µm process. When each leg is biased at 1mA, the gain of the opamp is ~18dB per stage, therefore, when configured for a gain of 2, the overall loop gain is ~30dB. This gain decreases dramatically when the output is near the rails as the driven second-stage device enters the linear region. Note that with a loop gain of 30dB, the closed-loop gain is only 1.95V/V, and this poor gain is only maintained with more than 150mV of headroom. At best, one could expect about 5b performance with a useful swing of 0.6V in a traditional configuration.

Technology scaling will not improve the situation. First, intrinsic gain will get smaller as channel lengths decrease. Second, to be in saturation, the minimum V_{DS} is the lesser of V_{GS}-V_T or a few kT/q. These obviously do not change with process.

This work introduces correlated level shifting (CLS) that simultaneously decreases the error due to finite opamp gain and allows true rail-to-rail operation. An extra phase is needed, but, surprisingly, there is no speed penalty when compared to a high-gain opamp solution because CLS does not require full settling during the next-to-last phase. In fact, the increased signal swing means that the same SNR can be achieved using smaller sampling capacitors. Thus, it could be argued that CLS can provide accurate results at a higher speed than using a traditional 2-phase operation with a high-gain opamp. For example, with CLS, the performance is maintained over the whole 0.9V supply, whereas a standard configuration has only a 0.6V swing. Thus, the standard configuration requires 2.25× larger sampling capacitors to achieve the same signal to kT/C noise ratio.

Figure 30.1.1 shows the simulated improvement provided by CLS to a 2-stage opamp used in a 1.5b-per-stage MDAC [1] operating with a 0.9V supply. The reason the boosting is so effective is explained shortly, but for now note how the CLS-configured MDAC provides a more accurate gain of 2 over the entire output range; i.e., true rail-to-rail operation. Also note how the effective loop gain is increased by a constant amount (36dB) across the output range.

Figure 30.1.2 shows the steps involved in the CLS operation. The actual implementation is fully differential, but single-ended is shown for simplicity. Three phases can be used, but for the pipelined ADC application, it is more convenient to use a 4-phase clock and lump ϕ_1 and ϕ_2 into a single phase. The sample and estimate phases are almost identical to the operation of the standard flip-around MDAC [1], which produces a first estimate of the output. The error in this estimate depends on the loop gain product Aβ. The key difference from a traditional flip-around operation is that this estimated output is sampled onto C_{LS} so it can be used to level shift the opamp output towards mid-supply during the final phase.

CLS increases the effective loop gain because the switched capacitor C_{LS} tends to return the opamp output to mid supply, regardless of the input. This action has the same effect as an additional gain stage, because the voltage stored across the capacitor is equal to what would have been across the gain stage. Thus, during the level shift phase, the *effective loop gain* (which determines final output voltage error) is approximately equal to the loop gain in the estimation phase multiplied by the loop gain in the level shift phase. Since the opamp has been returned to mid supply during the level-shift phase, the gain increase is a constant value, regardless of the output level. This significantly improves the performance near the supply rails. CLS action is different than that of correlated double sampling (CDS), which stores the error and subtracts it from the original output [2, 3]. Unlike CDS, CLS does not cancel offset or 1/f noise. Also, a CLS output stage cannot drive DC loads because the output is taken at a high impedance node; however, these shortcomings are not important for many switched-capacitor applications such as ΔΣ and pipelined ADCs. A significant advantage of CLS over CDS is that it does not add kT/C noise.

The configuration in Fig. 30.1.2 has the CLS network is inside the Miller loop. This keeps the bandwidth the same during ϕ_3 and ϕ_4 Additionally, charge transfer from the compensation cap during ϕ_4 can be used to robustly increase the effective gain by 10dB or more.

A 12b pipelined ADC is implemented in a 0.18µm process. The topology is similar to [1]. Each of the ten 1.5b-per-stage MDACs use the fully differential opamp in Fig 30.1.3, which has a loop gain of ~30dB in the MDAC configuration. The first 2 stages use 1.6pF sampling capacitors, while the remaining 8 stages use 0.4pF. Bias currents are scaled accordingly. The analog section use 0.9V for the supply and reference. The digital supply is kept at 1.8V instead of using bootstrapped switches. Sampling speed is expected to be ~100MHz, but a glitch on a bias line limited the speed to 20MHz with the analog components consuming 8.7mW @0.9V (including the reference current).

The 30dB loop gain of the MDAC would normally limit performance to ~5b. Furthermore, the performance drops off rapidly as the input approaches -3dBFS (150mV from the rail). With CLS, a better than 60dB performance (i.e., 10b), very close to 0dBFS, is expected. This is confirmed with measurements shown in Fig. 30.1.4, showing better than 10b performance right up to the rail (0dBFS). Actually, since the ADC reference is the power supply, at 0dBFS the opamp outputs are likely operating slightly beyond the rails due to opamp offsets.

The results in Fig. 30.1.4 are obtained with a C_{LS} value of ~3.2pF for the first 2 stages and 0.8pF for the remaining stages. C_{LS} is realized with a capacitive DAC (Fig 30.1.5), and performance is measured versus C_{LS} of the first 2 stages. The first concern is that small C_{LS} does not increase noise. The constant 11dB SNR with -60dBFS input (Fig. 30.1.6) suggests the noise floor is ~71dB for C_{LS} >100fF. The zero crossing of SNR in Fig. 30.1.4 corroborates this noise floor. Distortion is also measured with V_{in}=-1dBFS (~50mV from rails). Distortion characteristics are maintained for C_{LS} > 1.6pF, which is about 1/3 of the overall load. Higher opamp loop gain during ϕ_4 would allow performance to be maintained at the rails with smaller C_{LS}.

Acknowledgements:
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[1] A. M. Abo, P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE J. Solid-State Circuits,* vol.34, no.5, pp.599-606, May 1999.
[2] C. C. Enz, G. C. Temes, "Circuit techniques for Reducing the Effects of Opamp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilization," *Proceedings of the IEEE*, vol.84, no.11, pp.1584-1614, Nov 1996.
[3] J. Li; U.-K. Moon, "A 1.8-V 67-mW 10-bit 100-MS/s Pipelined ADC Using Time-Shifted CDS Technique," *IEEE J. Solid-State Circuits,* vol.39, no.9, pp. 1468-1476, Sept. 2004.

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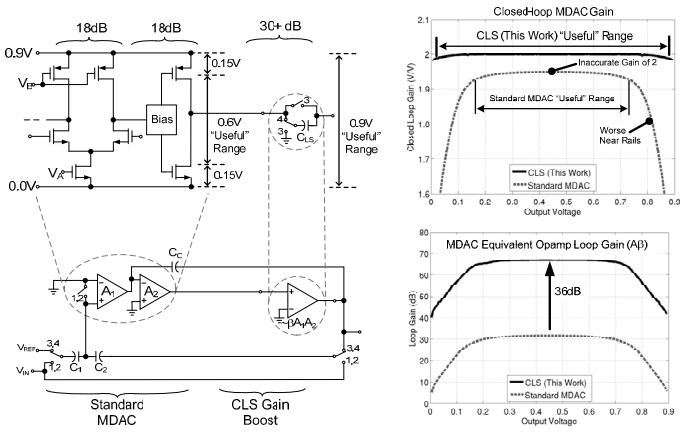

Figure 30.1.1: Simulated performance of 36dB opamp with and without CLS.

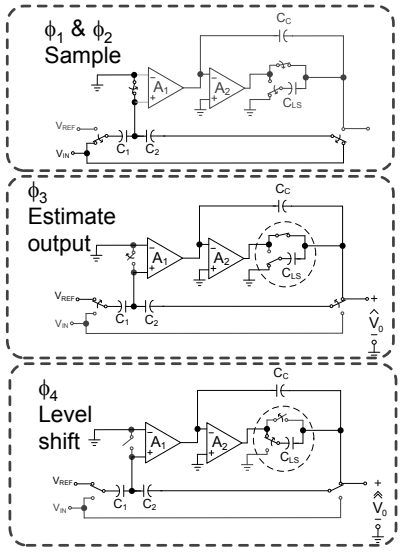

Figure 30.1.2: CLS operation.

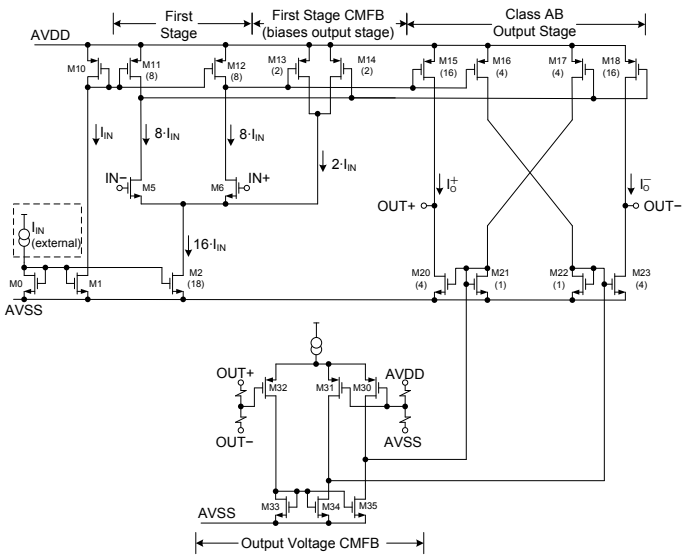

Figure 30.1.3: Schematic of the 2-stage opamp used for MDAC.

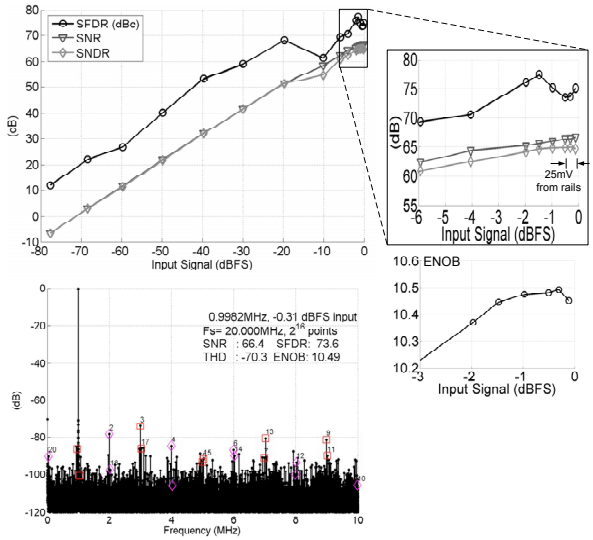

Figure 30.1.4: SFDR, SNR, SNDR and ENOB versus input amplitude and spectrum when driven 16mV from rails.

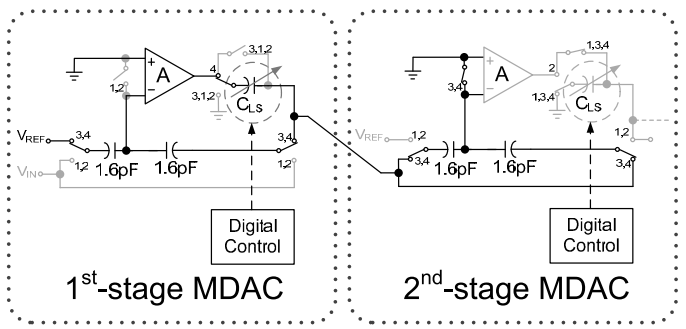

Figure 30.1.5: 1st-and 2nd-stage MDACs with internal digital control for C_{LS}.

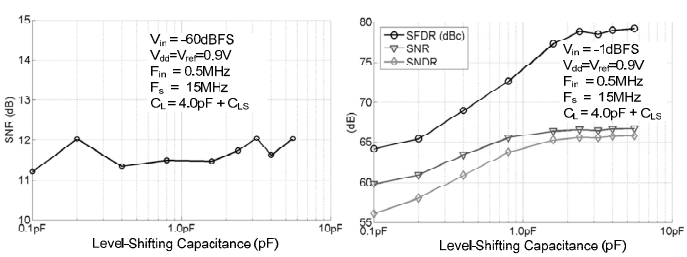

Figure 30.1.6: Performance as a function of C_{LS}.

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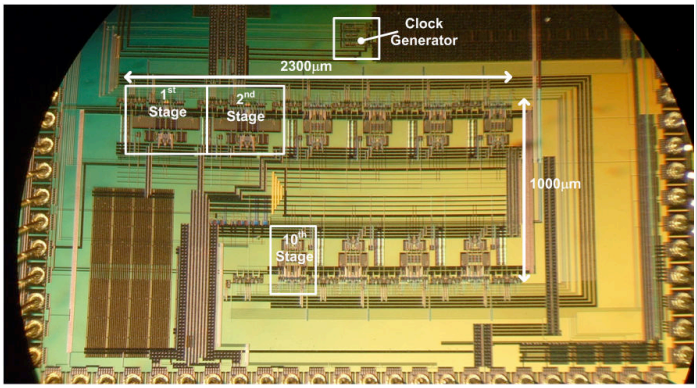

Figure 30.1.7: Micrograph of the chip fabricated in 0.18μm CMOS process.

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