TA 7.1: A Low-Distortion 22kHz 5th-Order Bessel Filter*

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A well-known design among the class of tunable continuous-time filters is the MOSFET-C filter. This design uses the linearized model behavior of a MOS transistor operating in the triode region in place of a passive resistor [1]. Due to mismatch and the inherent nonlinear behavior of a MOSFET operating in the triode region, THD has been limited to 40-60dB level with a volt-level signal swing in a single-5V system. The technique proposed herein relies on the linearity of the passive resistors and the tunability of current-steering MOS transistors operating in the triode region. Placing the nonlinear elements inside the feedback loops, and degenerating the MOSFETs by passive resistors, the distortion resulting from the nonlinear devices is greatly reduced. A prototype 22kHz Bessel filter automatically tuned to a switched-capacitor reference resistor has control voltage feedthrough below -100dB, and measured linearity better than -90dB THD, with a 2kHz, $4V_{pp}$ voltage swing. Measured THD demonstrates an improvement of at least 30dB over a conventional MOSFET-C filter. The chip consumes 40mW with a 5V supply, and the active die area is $7mm^2$ in 2μm double-poly CMOS.

The integrator with improved variable-resistance stage shown in Figure 1 (without R_f) is an extension of a MOSFET-C integrator based on a differentially-balanced variable resistor [2]. The variable resistor operates with a reduced voltage across the nonlinear MOSFETs and therefore exhibits lower distortion. The voltage scale factor, $F=V_i/V_x$ is equal to $1 + 2\bar{G}R$, where $\bar{G}$ is the average conductance of the four MOSFETs. This effect is identical to local feedback of an emitter degeneration. Note that these current-steering stages also face some reduction of the effective dc gain and bandwidth of the operational amplifier. Performance degradation due to these effects should be taken into account. Low distortion is also feasible using passive RCs and digitally trimming C, but the proposed linearity improvement technique achieves equivalent performance without switching the energy storing element [3].

Placing the nonlinear MOSFETs inside the feedback loops uniquely applies the feedback configuration of active filters, to further reduce the nonlinearity in addition to the passive resistor degeneration previously mentioned. Consider the first-order filter example shown in Figure 1. The resistor R_f is fed back from the output to the current-steering element. (Loading effects need to be considered.) Consequently, the nonlinear current steering element is placed inside the feedback loop. The feedback loop gain, that proportionally reduces the distortion of the MOSFETs inside the loop, decreases as the input frequency passes the dominant pole of the MOSFET-C integrator. Distortion reduction by the feedback approaches its minimum at the filter passband edge. The improvement resulting from the voltage scaling factor, F, however, remains constant at all frequencies.

Circuit noise increases as a function of the voltage scale factor, F, due to the bypassing of the integrating current in the current-steering element. Noise-versus-linearity optimization is therefore necessary to minimize the noise contributed by the current-steering element. It is found that distortion is reduced by 14dB (F=5) with less than 3dB increase in the noise power for the first-order filter example without the additional improvement by the feedback. Taking into account a significant linearity improvement by the feedback loop, a much larger signal swing without distortion justifies the marginal increase in the noise floor.

The automatic tuning takes advantage of switched-capacitor accuracy in achieving the desired corner frequency [4]. This switched-capacitor tuning method, merely a time-constant matching circuit, greatly simplifies automatic tuning. Figure 2 shows the time-constant matching integrator of the linearity-improved continuous-time path and the switched-capacitor path. The mismatch of the two time constants, that simplifies to the mismatch of R_{eq} and $1/f_{clk}C_1$, appears at the output of the integrator. That voltage is then translated to the control voltage V_C of the current steering MOSFETs. The lower portion of the schematic is the tuning circuitry for the common-mode control voltage V_{CM} that maintains the designed voltage scale factor F. By choosing the product $R_{LP}C_{LP}$ very large, open-loop control is established.

An audio-band (22kHz) fifth-order Bessel filter with a voltage scaling factor F varied between 2.5 to 5 is fabricated using a 2μm CMOS technology. Figure 3 is a fifth-order Bessel filter using this linearity improvement technique. The filter is node-voltage scaled and the capacitor sizes are optimized for dynamic range with a fixed total-capacitance constraint. The box with the crossing arrows indicates the current-steering portion of the variable-resistor stage. The tuning capability is demonstrated in Figure 4. Figure 5 is a plot of THD versus input frequency where the input signal is fixed at $4V_{pp}$ differential. This plot captures the effect of the feedback loop on distortion. Each of the two lines represents a different control voltage set to place the f_{-3dB} at 22kHz and 32kHz. Even though the THD is partially dependent on the control voltage itself, the THD improvement resulting from the widening of the filter bandwidth is observed in this plot. This in turn implies that as an anti-alias/smoothing filter for oversampling converters, the placement of a higher f_{-3dB} would permit better linearity for the audio-band. The dynamic range measured in reference to the $4V_{pp}$ signal is 83dB. Only a $10\mu V_{rms}$ control voltage feedthrough was observed at the clock frequency since a MHz range clock is used and a lowpass filter eliminates the clock noise. Table 1 summarizes the measured performance of the prototype, and Figure 6 is the chip micrograph.

Acknowledgments

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References

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[4] Viswanathan, T. R., et al., "Switched-capacitor frequency control loop", IEEE J. Solid-State Circuits, vol. SC-17, no. 4, pp. 775-778, Aug. 1982.

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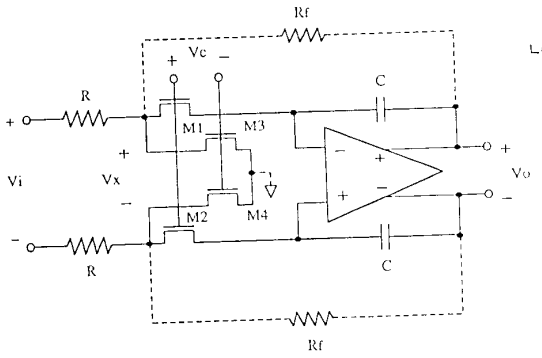

Figure 1: Linearity-improved integrator/1st-order filter.

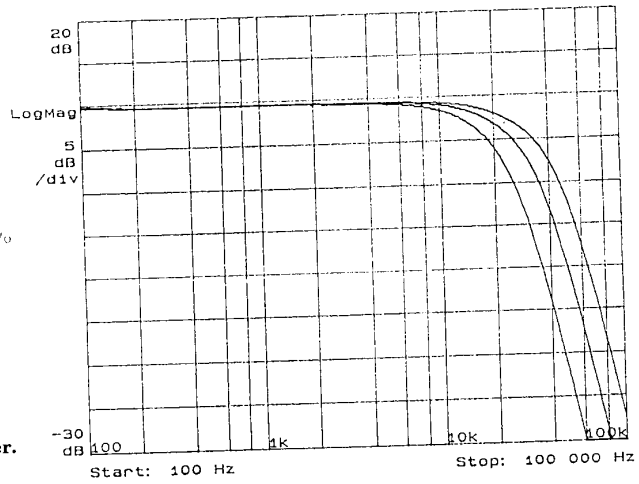

Figure 4: Tunable frequency response.

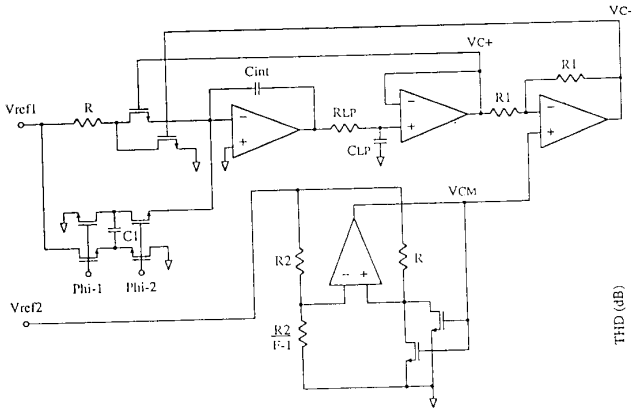

Figure 2: Automatic tuning circuitry.

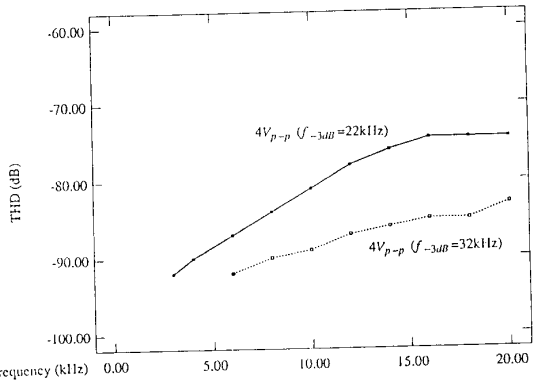

Figure 5: THD vs. input frequency.

Figure 6: See page 271.

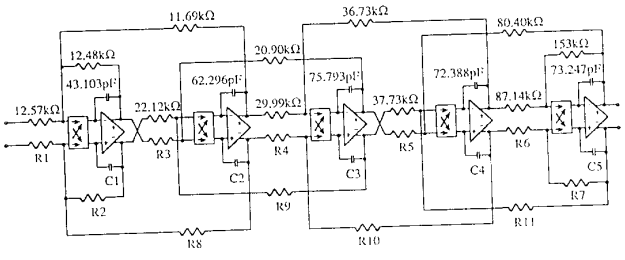

Figure 3: 22kHz 5th-order Bessel filter.

Filter type	5th-order Bessel
Cutoff frequency	22kHz
Tunable range	2k to 35kHz
Passband f_{-3dB} accuracy	±1%
Passband deviation	0.1dB
Group delay	19±0.5μs
Control voltage feedthrough	$10\mu V_{rms}$
THD ($4V_{pp}$, 2kHz input)	-90dB
SNR	83dB
CMRR (flat across spectrum)	58dB
PSRR+ (worst at 10kHz)	58dB
PSRR- (worst at low freq.)	47dB

Table 1: Summary of performance.

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Name	Function	Transistors	Technology	Power	Speed	Area
TMCIN	Conversion of ATM cells into MSC	230k	0.7μm CMOS	3.0W	155.5MHz	86mm²
TMCOUT	Conversion of MSC into ATM cells	960k	0.7μm CMOS	4.0W	155.5MHz	180mm²
POL	Coprocessor for bandwidth allocation	56k	0.7μm CMOS	2.0W	77.7MHz	65mm²
ETT/4STM1	Ext. transfer mode termination; ATM-cell packing	620k	0.7μm CMOS	3.5W	77.7MHz	170mm²
ICC	Physical medium termination	15k	0.8μm BiCMOS	6.0W	622.0MHz	30mm²
SRT RAM	The self-routing tag (SRT) is the header of the MSC and is used to route the MSC through the switch					
TRANSRAM	Translation table: the ATM header is translated into an internal reference number					
LABELRAM	Translation table: the internal reference number is translated into a new ATM header					
POLRAM	Contains the bandwidth allocated by each connection					

Table 1: ALT chip set overview.

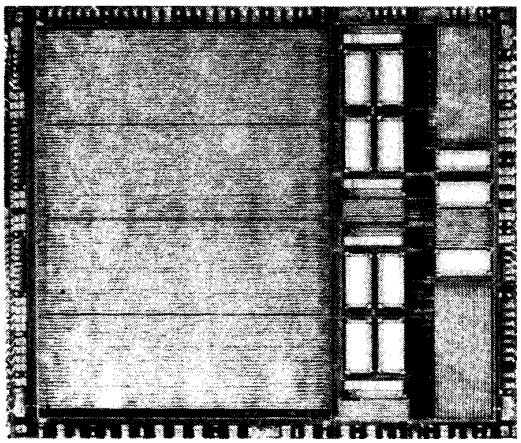

Figure 6: Micrograph of 4STM1 circuit.

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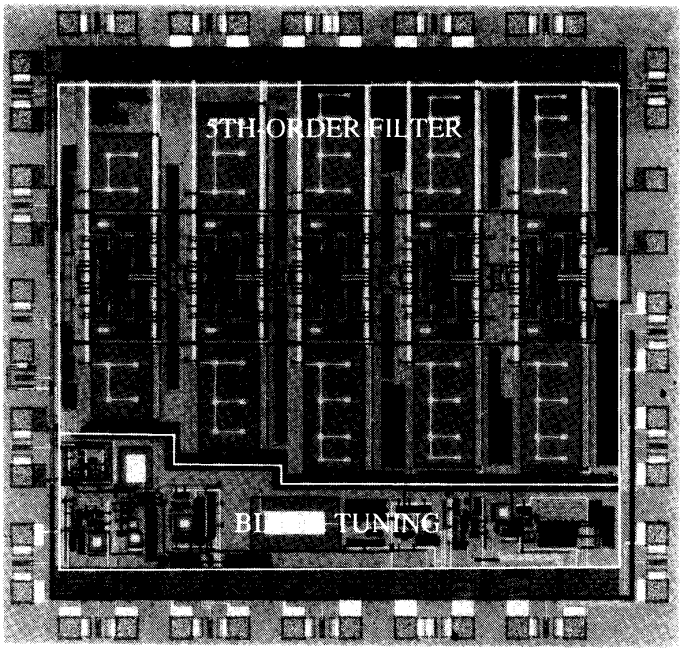

Figure 6: Chip micrograph.