An On-chip Calibration Technique for Reducing Supply Voltage Sensitivity in Ring Oscillators

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***Abstract*—A technique for reducing the supply voltage sensitivity of a ring oscillator using on-chip calibration is described. A 1-V 0.13-μm CMOS PLL demonstrates robust performance against VCO supply noise over operating frequencies of 0.5 to 2 GHz. In the presence of a 10-mV 1-MHz VCO supply noise, the measured rms jitter of the proposed PLL with on-chip calibration is 3.95 ps at a 1.4-GHz operating frequency, while a conventional design measures 8.22 ps rms jitter. For 10-MHz VCO supply noise, the measured rms jitter is improved from 16.8 ps to 3.97 ps. The total power consumption of the PLL is 9.6 mW at 1.4 GHz, and the combined core die area of the PLL and the calibration circuitry is 0.064 mm^2.**

***Index Terms*—Digital calibration, phase-locked loop, supply voltage sensitivity, voltage controlled oscillator.**

I. Introduction

PHASE-LOCKED loops (PLLs) are one of the key building blocks in mixed-signal integrated circuits, and are widely used in applications ranging from clock generation to clock recovery and frequency synthesis. In such applications, there often exist stringent requirements in timing jitter or phase noise. As the continued scaling of deep-submicron CMOS process enhances the level of integration, more noise is coupled from switching digital circuits. Consequently, the design of PLLs that are tolerant to noise variations is increasingly important and necessary.

To benefit from the process scaling and to improve noise immunity, noise-sensitive analog circuits can be replaced with inherently noise-insensitive digital counterparts. For example, digital PLLs (DPLLs) have received increased attention due to their promising advantages over traditional analog PLLs. These include the inherent tolerance to noise and process variations and the ease of scaling with process. Although DPLLs have been designed for a wide variety of applications in the multi-GHz frequency range [1]–[3], the voltage-controlled oscillators (VCOs) continue to be analog blocks. VCOs are critical components in PLLs, and are becoming the bottleneck in the design of high-performance PLLs. In particular, for ring VCOs, supply noise is a major design concern as the oscillation frequency of a ring VCO is highly dependent on the supply voltage.

To suppress the change in frequency of a ring VCO with supply noise, traditional methods employ voltage regulators [4]–[6] at the cost of reduced voltage headroom. However, with the scaling down of supply voltages, the lowered voltage swings make supply-regulated ring-oscillator-based PLL designs difficult. For the design of ring VCOs and PLLs at 1-V supply, alternative techniques should be considered.

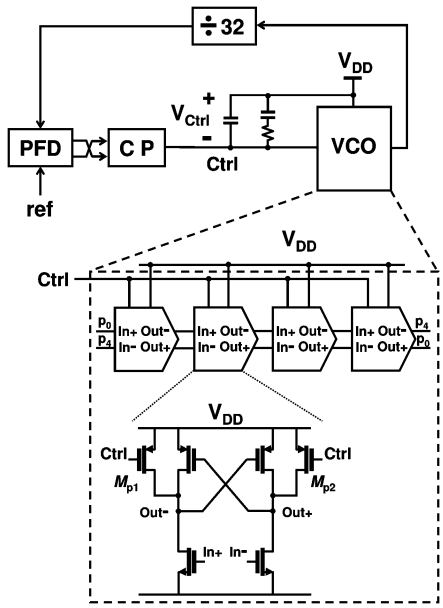

Fig. 1. Conventional ring-oscillator-based PLL.

One of these alternative techniques employs compensation [7]. However, due to process variations and the dependence of the compensation on the oscillation frequency, it is practically impossible to achieve accurate compensation. Since process variations continue to increase as CMOS technology scales down, adaptive compensation techniques are required.

This paper describes one such technique [8] for reducing the supply voltage sensitivity in ring oscillators. The paper is organized as follows. An adaptive supply compensation technique using on-chip calibration is described in Section II. Section III presents the proposed on-chip calibration technique, followed by measurement results in Section IV. Section V discusses the impact of temperature variations on the new calibration technique and presents an enhanced scheme for making the design tolerant to temperature variations. Finally, conclusions are drawn in Section VI.

II. Supply Compensation Technique

A. Conventional Ring VCO

Consider a conventional ring-oscillator-based PLL with a four-stage ring VCO, as shown in Fig. 1. The commonly used Lee–Kim delay cell [9] is employed in this VCO. Like most

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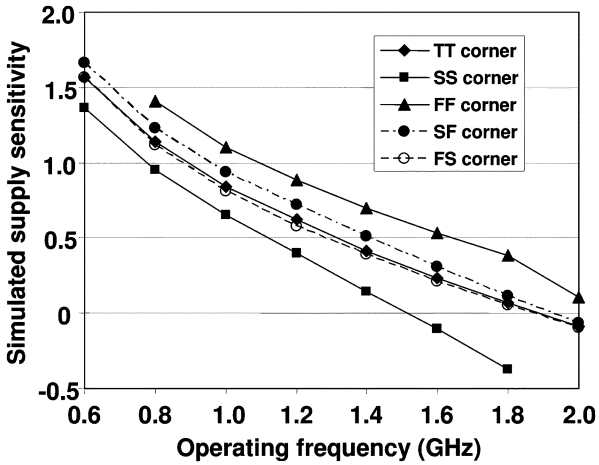

Fig. 2. Simulated VCO supply sensitivity for different process corners.

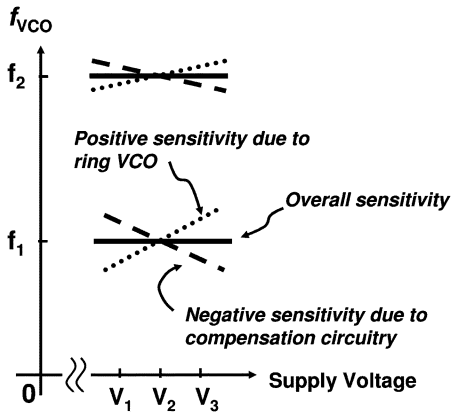

Fig. 3. Concept of supply sensitivity compensation. V_1, V_2, and V_3 are three different supply voltages; the VCO supply is V_2 under typical operating conditions. The VCO has a larger sensitivity at a lower frequency f_1 compared with f_2. To provide an optimum compensation at each operating frequency, the negative sensitivity due to compensation circuitry needs to be controlled.

ring VCOs, the frequency is tuned by controlling the pMOS transistors. In particular, the gates of the two pMOS transistors M_{p1} and M_{p2} are controlled. To minimize supply noise coupling, the PLL loop filter is connected to $V_{\rm DD}$ instead of ground, thus the $V_{\rm GS}$ of the pMOS transistors is fixed. However, the $V_{\rm DS}$ of the pMOS transistors varies with a variation in the supply voltage, causing the current in the delay cell to change. An increase in the supply voltage leads to an increase in the current, hence, an increase in the oscillation frequency. On the other hand, since the VCO outputs swing from rail to rail, an increase in the supply voltage results in an increased swing, hence, a lowered speed. As a result, while the first is dominant, the VCO suffers from supply noise due to these two opposing effects.

To evaluate the supply noise immunity, supply voltage sensitivity is commonly used [7]. This sensitivity is defined by a percentage change in the oscillation frequency to a percentage change in the supply voltage, i.e., $\partial f_{\rm VCO}(\%)/\partial V_{\rm DD}(\%)$. Fig. 2 shows the simulated supply voltage sensitivity of the ring VCO in Fig. 1 for operating frequencies from 600 MHz to 2 GHz. The simulations have been performed at different process corners. As shown in the figure, the supply sensitivity decreases with an increase in the operating frequency. Moreover, at the highest operating frequency, the supply sensitivity even falls below zero to a negative value.

B. Supply Compensation Technique

Since the VCO has a positive supply voltage sensitivity for most operating frequencies, adding a compensation circuitry with a negative supply voltage sensitivity can reduce the total sensitivity. The concept of supply compensation is illustrated in Fig. 3, where V_1, V_2, and V_3 are three different supply voltages. The VCO supply is V_2 under typical operating conditions. The dotted and dashed lines correspond to the positive sensitivity due to the ring VCO and a negative sensitivity due to the compensation circuitry, respectively. If both are properly combined, the dependence of the oscillation frequency $f_{\rm VCO}$ on the supply voltage would be cancelled, leading to a reduced supply voltage sensitivity.

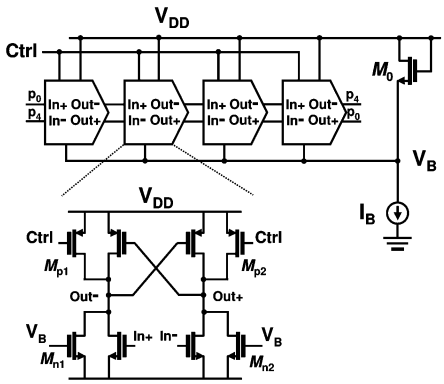

Fig. 4. VCO with the proposed compensation circuitry. The nMOS transistors M_{n1} and M_{n2} compensate for the changes in oscillation frequency due to supply variations. The magnitude of the compensation is controlled by the current I_B.

At a given operating frequency, the goal of the compensation scheme is to make the oscillation frequency insensitive to supply voltage for voltages V_1 to V_3. As indicated in Fig. 2, due to the dependence of the VCO supply sensitivity on the operating frequency, the negative sensitivity due to the compensation scheme should be adjusted for different frequencies. Specifically, since the VCO has a larger sensitivity at a lower frequency f_1 compared with f_2 (Fig. 3), the added negative sensitivity at f_2 should be smaller. To provide an optimum compensation for the supply voltage sensitivity at each operating frequency, the compensation circuitry needs to be appropriately adjusted.

The compensation circuitry proposed in this paper is shown in Fig. 4. Based on the Lee–Kim delay cell, transistors M_{n1} and M_{n2} have been added between the output nodes and ground. The gates of M_{n1} and M_{n2} are connected to the diode-connected nMOS transistor M_0 (node V_B), which is biased by a programmable current I_B. When the supply voltage increases, the current in the pMOS transistors increases. The voltage V_B also increases due to M_0, causing M_{n1} and M_{n2} to sink more current to ground. This mechanism slows the oscillator and thus compensates for the increase in the oscillation frequency due to

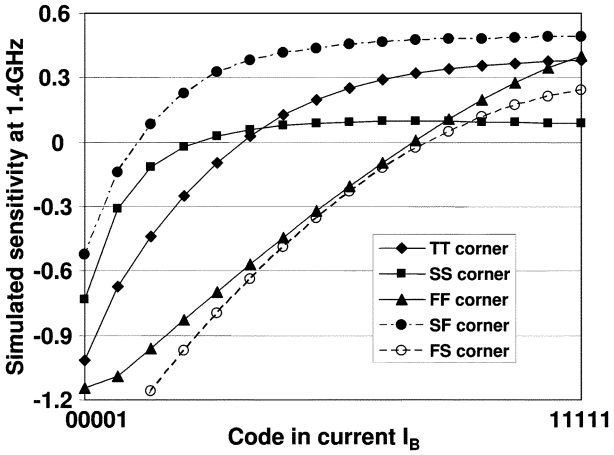

Fig. 5. Simulated VCO supply sensitivity with proposed compensation circuitry for different process corners.

an increase in the VCO supply voltage. If the increase in the currents of M_{n1} and M_{n2} is the same as the increase in the currents of the pMOS transistors, the VCO would maintain the same oscillation frequency. The VCO supply sensitivity would be effectively reduced to zero.

The magnitude of the negative sensitivity is controlled by the bias current I_B. For each operating frequency, a corresponding current I_B needs to be determined to achieve the optimum compensation.

As an example, consider the VCO operating at 1.4 GHz. The simulated overall sensitivity of the VCO with the compensation circuitry is shown in Fig. 5. The current I_B is digitally controlled by a 5-bit word. The code "11111" corresponds to a conventional VCO without the compensation circuitry. As expected, the sensitivity increases with an increase in the bias current I_B. The optimum code for I_B is obtained when the sensitivity is reduced to zero. As shown in Fig. 5, the optimum code varies with process variations and cannot be determined *a priori*. Therefore, an on-chip calibration is needed to ensure optimum compensation under process variations.

III. On-Chip Calibration Technique

To effectively reduce the supply voltage sensitivity to zero, the current I_B has to be calibrated. We propose a new on-chip calibration technique that ensures optimum compensation. Unlike a technique that uses on-chip jitter measurement [10], this technique is based only on measuring the polarity of the supply voltage sensitivity.

A. Calibration Algorithm

The simulation results of Fig. 5 are simplified for illustration purposes in Fig. 6. The relationship between the overall supply voltage sensitivity and the current I_B is shown in the figure. Our calibration algorithm uses a binary search based on this relationship. The flowchart of the algorithm is given in Fig. 7. The procedure starts by "10000" reset, and the algorithm determines all five bits in I_B in five calibration cycles. In each calibration cycle, the polarity of the supply voltage sensitivity is measured. This is performed by comparing the oscillation frequencies for two different supply voltages V_1 and V_3 (Fig. 3).

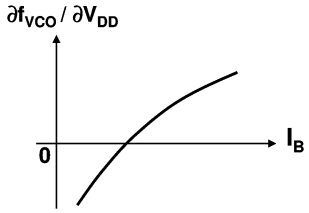

Fig. 6. Relationship between the supply voltage sensitivity and I_B.

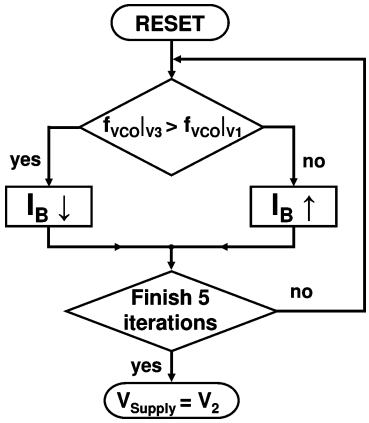

Fig. 7. Flowchart of the proposed calibration algorithm.

If the VCO runs faster for the higher supply voltage V_3 than at V_1 ($f_{\rm OSC}|_{V3} > f_{\rm OSC}|_{V1}$), the supply sensitivity measured is positive, hence, the current I_B should be decreased. Conversely, when $f_{\rm OSC}|_{V3} < f_{\rm OSC}|_{V1}$, I_B should be increased. This trimming procedure is continued from the MSB to the LSB until all five calibration cycles are completed, and thus the equilibrium ($f_{\rm OSC}|_{V3} \approx f_{\rm OSC}|_{V1}$) is reached to the LSB precision. Next, the supply voltage V_2 is used for the VCO. Since V_2 is in between V_1 and V_3, this provides a VCO supply voltage sensitivity that is closer to zero.

B. Circuits

To implement the above algorithm, a variable supply voltage is needed to measure the supply sensitivity. As shown in Fig. 8(a), three pMOS transistors with different sizes have been inserted in series between $V_{\rm DD}$ and the supply node of the VCO. The three pMOS transistors operating in the triode region have nominal series resistance values of 18, 12, and 6 ohms. By turning on one of the transistors M_1, M_2, and M_3, different supply voltages V_1, V_2, and V_3 can be provided to the oscillator. Fig. 8(b) summarizes the simulated voltage drops between $V_{\rm DD}$ and the three possible supply voltages. The reductions in the voltage headroom are small. Furthermore, the series resistance provides a small amount of supply isolation.

The simplified schematic of the resulting VCO is shown in Fig. 9. It incorporates dual-delay paths [11] to extend the frequency range for low supply voltage operation. For a typical supply voltage V_2, since the transistor M_2 operates in the triode region, the reduction in voltage headroom (from $V_{\rm DD}$ to V_{Supply}) is about 50 mV. Further reduction is also feasible.

Next we need to address how the VCO oscillation frequencies are compared for different supply voltages. In a PLL, the VCO output frequency is corrected by the feedback loop to lock

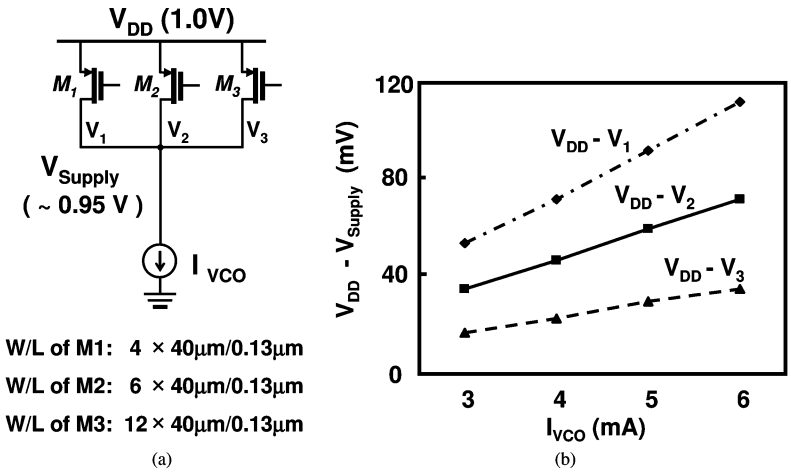

Fig. 8. (a) pMOS transistors in series with $V_{\rm DD}$ are used to vary the supply voltage. (b) Comparison of the simulated voltage drops with different settings of the VCO supply voltages.

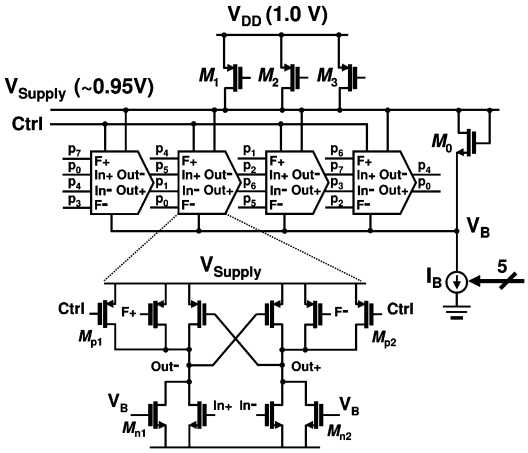

Fig. 9. Final VCO schematic.

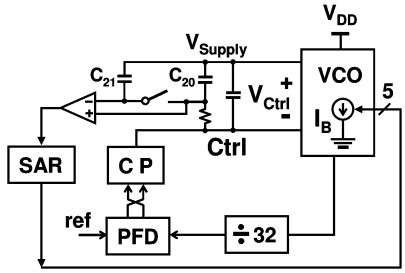

Fig. 10. Schematic of PLL with calibration.

to the reference frequency. When the supply voltage changes from V_3 to V_1, the VCO output frequency does not settle to a new value but the control voltage $V_{\rm Ctrl}$ does. Conceptually, it is possible that the previous value of $V_{\rm Ctrl}$ can be stored on a capacitor and the change of $V_{\rm Ctrl}$ can be detected by using a high-precision comparator. Based on this change (either an increase or a decrease), the code in I_B can be determined via a successive approximation register (SAR). This is illustrated in Fig. 10. This scheme can be easily implemented in a digital PLL, since the control word (voltage for an analog PLL) is digital and is easily compared. In an analog PLL, however, it requires a very high-precision comparator because the VCO has a large gain which is typically about 4 GHz/V. An observed change in the oscillation frequency can lead to a less than 1 mV change in $V_{\rm Ctrl}$. Virtually an offset free comparator would be required.

To eliminate the need for a good comparator, an open-loop scheme is proposed and has been implemented in our prototype chip. The schematic of the PLL including the calibration circuitry is shown in Fig. 11(a). Fig. 11(b) shows the timing diagram. Each calibration cycle consists of lock-in and open-loop phases. To provide an open loop, a CMOS switch has been added between the charge pump (CP) and the loop filter. The charge injection of the switch is negligible, since the capacitance of the switch is much smaller than that of the loop filter. In the lock-in phase, the supply voltage V_3 is used for the VCO. The signal CLK_C is kept "1" for a time period of $2^6/f_{\rm ref}$ to ensure that the PLL settles, where $f_{\rm ref}$ is the reference clock frequency. In the following open-loop phase, the VCO supply voltage is changed to V_1 and CLK_C breaks the loop. Because $V_{\rm Ctrl}$ does not change, the free-running VCO oscillation frequency changes only due to the change in the supply voltage. This frequency change is observed at the output of the CP, causing the output $V_{\rm CPO}$ to significantly increase or decrease. The CP output is fed to two comparators. The voltage $V_{\rm CPO}$ continues to either increase or decrease until it causes one output of the comparators to flip, which triggers an overflow signal to complete the open-loop phase. The open-loop phase also terminates if none of the comparators trigger within the time period of $2^6/f_{\rm ref}$. At the end of the open-loop phase, the current bit of the SAR is determined and the next significant bit is preset to "1". This calibration cycle starts with the MSB and is repeated until all five bits have been determined.

C. Ground Noise

Most supply-regulated PLLs only reduce supply noise. However, ground noise can be equally important in deep-submicron CMOS process. Adding decoupling capacitors between $V_{\rm DD}$ and ground can attenuate ground noise at the cost of die area. A differential supply-regulated design [6] suppresses the ground noise with a reduced headroom in the ground rail.

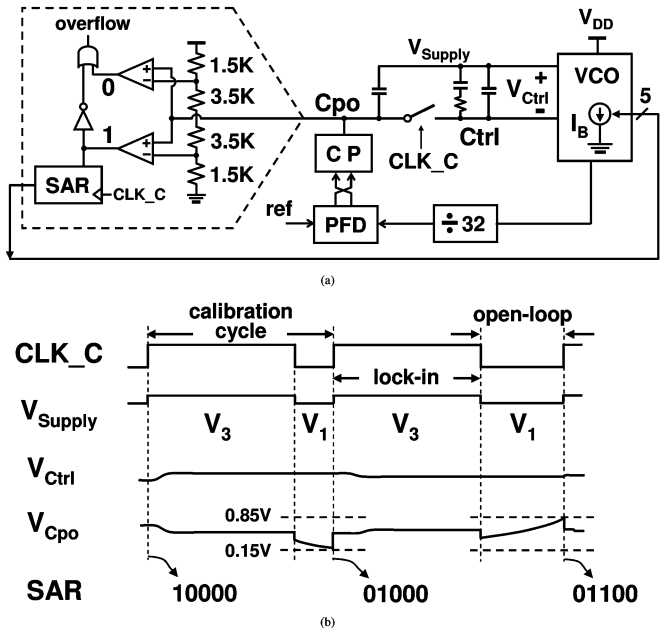

Fig. 11. (a) Schematic of the implemented PLL with calibration. (b) Timing diagram.

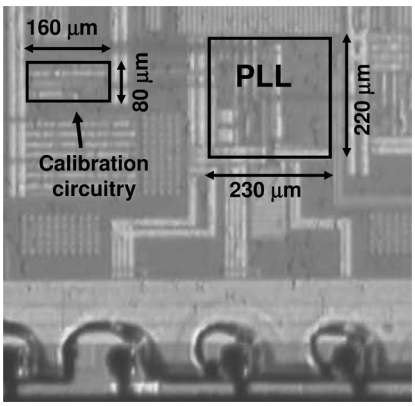

Fig. 12. Die photo.

Although the proposed VCO and the calibration technique have been designed to reduce the supply noise, ground noise is also reduced at no additional cost. In Fig. 9, assume that there is a decrease in the voltage on the ground node. As a result, the common mode of the VCO delay cell outputs also reduces by the same amount. The increase in the currents of the pMOS transistors due to an increase in $V_{\rm DS}$ is the same as the increase in the currents of the nMOS transistors M_{n1} and M_{n2} due to an increase in $V_{\rm GS}$. This condition is exactly the same as when the supply voltage changes, and it is compensated for by the same on-chip calibration. Another way of looking at why the ground noise is also suppressed is because our proposed supply noise compensation is built within the oscillator itself. It does not distinguish between the positive or the negative supplies, unlike supply-regulation-based techniques. This is an important advantage of our technique over the traditional supply-regulated PLL designs.

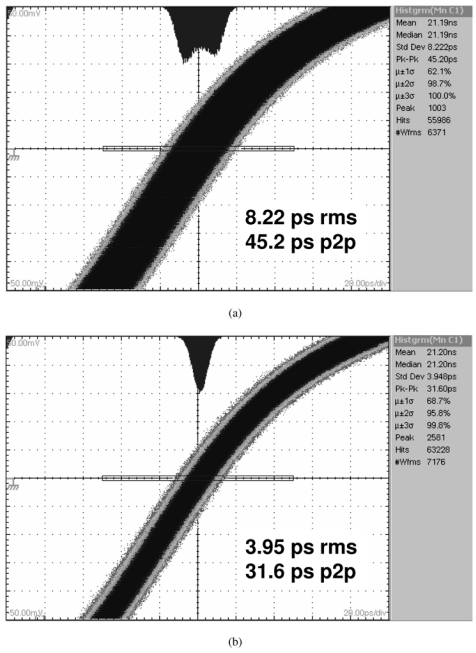

Fig. 13. Measured jitter histogram for a 1-MHz modulation frequency. (a) Conventional VCO. (b) Proposed VCO with calibration.

IV. Measurement Results

The proposed PLL with the calibration circuitry (Fig. 11) has been fabricated in a 0.13-μm CMOS process. The die photo of the prototype chip is shown in Fig. 12.[1] The core areas of the PLL and the calibration circuitry are 0.051 mm^2 (230 μm $\times$ 220 μm) and 0.013 mm^2 (160 μm $\times$ 80 μm), respectively. The pMOS transistors M_1, M_2, and M_3 (Fig. 9) occupy a negligible amount of die area.

To evaluate the supply noise suppression, the PLL performance was measured in the presence of VCO supply noise.[2] A 10-mV noise tone was added to the $V_{\rm DD}$ of the VCO at different modulation frequencies. At an operating frequency of 1.4 GHz, the on-chip auto-calibration circuit converges to the code "01001", whereas the conventional VCO design is equivalent to using the code "11111". Figs. 13(a) and (b) show the measured PLL jitter histograms of the conventional PLL and the proposed PLL with calibration, respectively, at a 1-MHz modulation frequency. The measured rms jitter is improved from 8.22 ps to 3.95 ps, and the peak-to-peak jitter improved from 45.2 ps to 31.6 ps. Figs. 14(a) and (b) compare the jitter histograms of the conventional design and the proposed design at a 10-MHz modulation frequency. The measured rms and peak-to-peak jitter are improved from 16.8 ps to 3.97 ps and from 74.0 ps to 33.2 ps, respectively. The measured performance is shown in Fig. 15 for a range of modulation frequencies. Since the noise tone at the VCO supply is bandpass filtered by the PLL, the conventional design exhibits a bell-shaped curve. The curve is flattened by the VCO, indicating that the proposed VCO with on-chip calibration suppresses the supply noise for any supply

[1]Unlike in the prototype chip, the PLL and calibration circuitry should be laid out close to each other to minimize the length of the control line.

[2]The supply sensitivity cannot be measured since the control node was not brought out in the prototype chip.

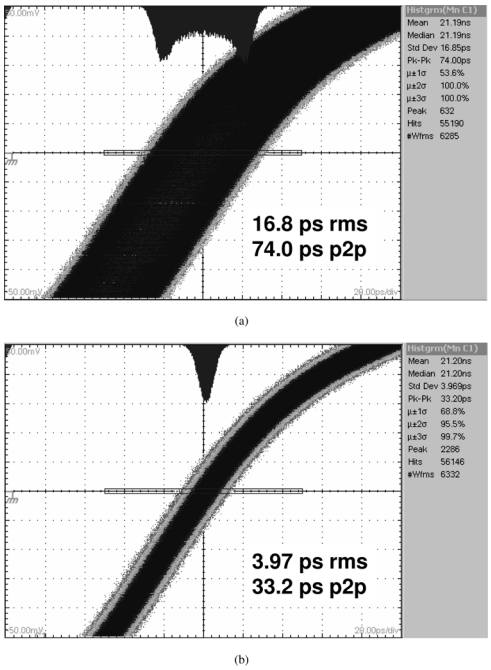

Fig. 14. Measured jitter histogram for a 10-MHz modulation frequency. (a) Conventional VCO. (b) Proposed VCO with calibration.

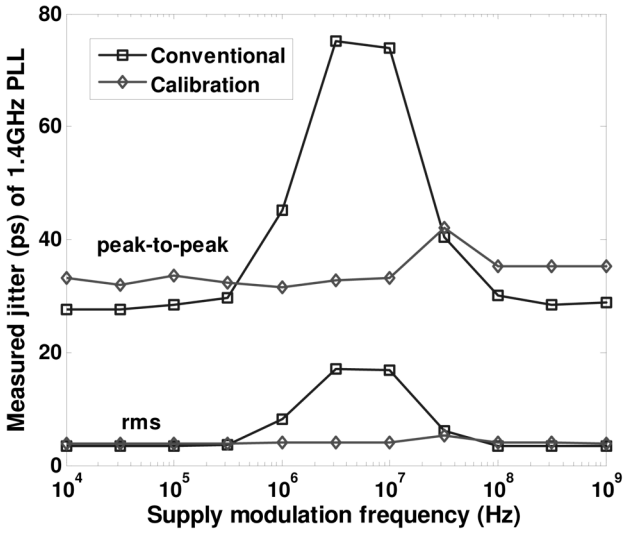

Fig. 15. Measured jitter with supply modulation frequency.

modulation frequency. The VCO consumes 5.4 mA (including I_B), which reflects a 23% overhead compared to the conventional VCO (measured at code "11111" excluding I_B for a fair comparison). Other circuits in the PLL draw 4.2 mA from the 1-V supply.

The SAR can be also controlled manually for evaluation purposes. The measured rms jitter of the PLL versus a 5-bit word control for I_B at 1.4-GHz operation is shown in Fig. 16. The optimum code (i.e., the best performance) that is manually reached at 1-MHz modulation frequency is "01010". The on-chip autocalibration circuit converges to a code with only one bit offset. As seen from Fig. 16, the overall jitter performance could be modestly improved even when the VCO is compensated with a fixed code (e.g., a digital code of "10000"). However, a fixed

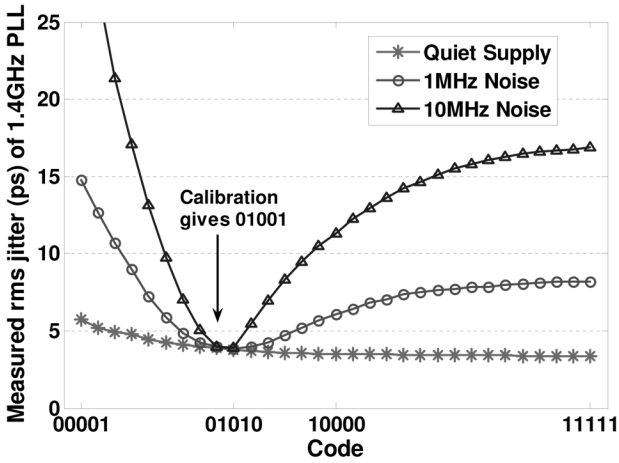

Fig. 16. Measured rms jitter of 1.4-GHz PLL.

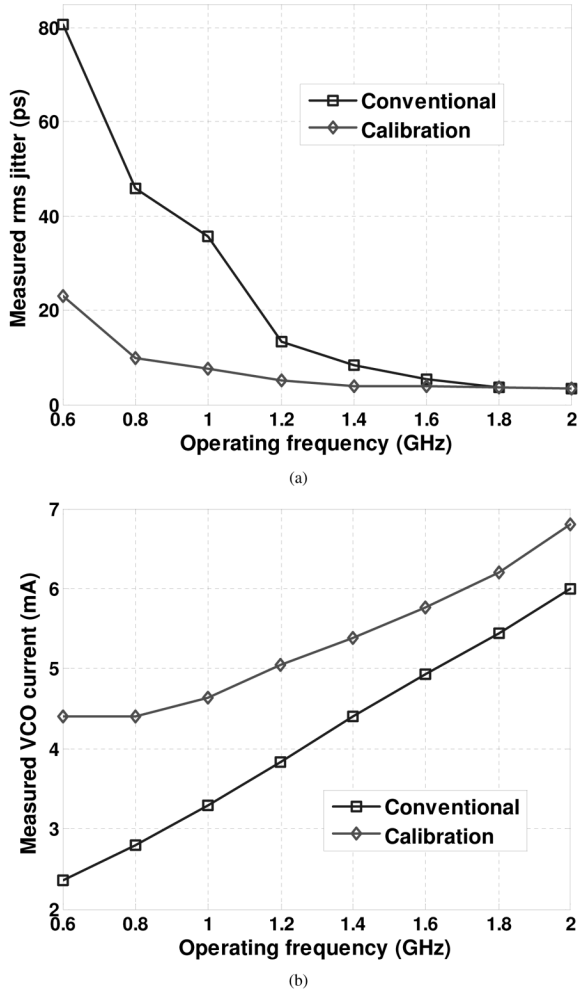

Fig. 17. Comparisons of measured (a) performance, and (b) VCO current consumption.

compensation would be highly susceptible to process variations. Hence, the resulting performance would fall short of the desired optimum that can be reached via an automatic calibration. With a quiet supply, the measured rms jitter increases with a decrease in the code for two reasons. Adding the transistors M_{n1} and M_{n2} in the proposed VCO delay cell (Fig. 9) degrades the phase

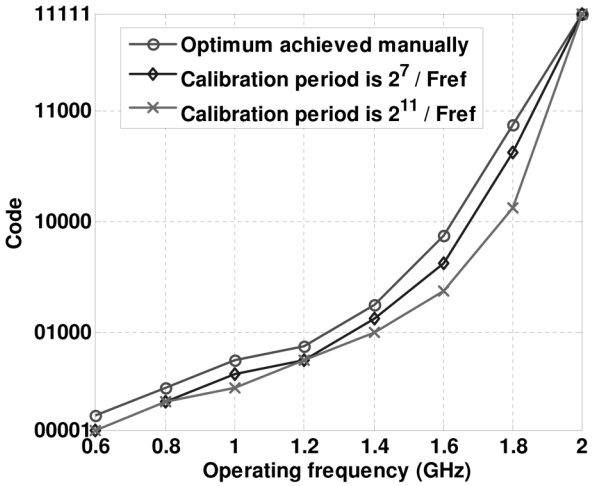

Fig. 18. Comparison between the optimum code and the calibrated code.

TABLE I
PERFORMANCE SUMMARY

Technology	0.13-μm CMOS
Supply voltage	1.0 V
Frequency range	0.5-2.0 GHz
Die area (PLL core)	0.051 mm^2
Die area (calibration circuitry)	0.013 mm^2
Power dissipation @ 1.4 GHz	9.6 mW
Loop bandwidth @ 1.4 GHz	3 MHz
Jitter with clean VCO supply	3.90 ps rms @ 1.4 GHz
Jitter with a 10 mV, 1 MHz supply noise	3.95 ps rms @ 1.4 GHz
Jitter with a 10 mV, 10 MHz supply noise	3.97 ps rms @ 1.4 GHz

noise performance. Simulation results indicate that, depending on the code, the phase noise is worse by up to 3 dB at 1-MHz offset. Secondly, the VCO gain $K_{\rm VCO}$ increases with a decrease in the code, leading to an increased jitter as well. Note that the PLL loop bandwidth is kept roughly the same for each code by changing the CP current in order to evenly maintain the impact on performance due to the PLL loop bandwidth.

The proposed PLL demonstrates robust performance against VCO supply noise over the full operating frequency range from 0.5 GHz to 2 GHz. With a 1-MHz modulation frequency, the measured PLL rms jitter for the conventional design and the proposed design is compared in Fig. 17(a). The proposed VCO with the help of calibration improves the VCO robustness to the supply noise significantly. The overhead in power consumption is indicated in Fig. 17(b). In particular, for a lower operating frequency, the performance improves more significantly, and with a larger power overhead.

Fig. 18 shows the comparison between the code given by the on-chip calibration and the optimum code that is reached

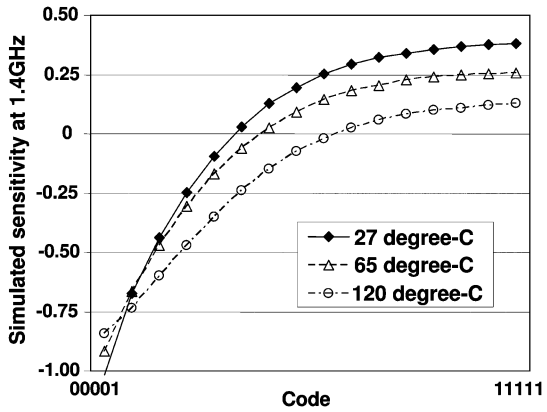

Fig. 19. Simulated sensitivity with temperature variations.

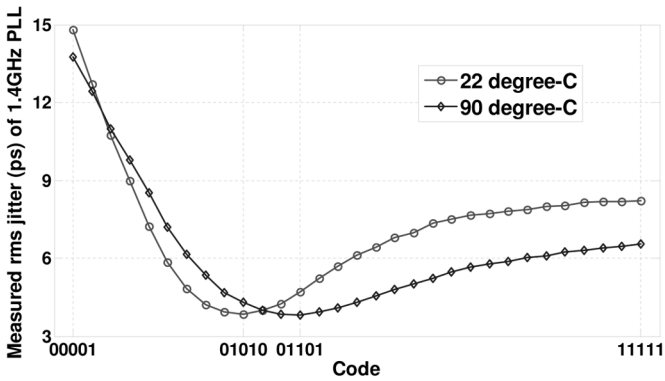

Fig. 20. Measured rms jitter in the presence of a 1-MHz supply noise.

manually. The code increases with an increase in the operating frequency and converges to "11111" at the highest frequency. As suggested in Fig. 2, at a lower frequency a larger compensation is needed, but no compensation is necessary at the highest frequency since the VCO sensitivity is negative. Compared with the optimum code, the on-chip calibration yields a negative offset of 1 or 2 LSBs. The error becomes larger when the calibration period is increased from $2^7/f_{\rm ref}$ to $2^{11}/f_{\rm ref}$. We suspect that this error is mainly due to the leakage in the PLL loop filter. In our implementation, a pMOS capacitor is used for the loop filter in order to reduce die area. To reduce the leakage, a thick-oxide MOS capacitor or a metal capacitor can be employed. Furthermore, the leakage problem can be eliminated if the proposed VCO and calibration technique are integrated in a digital PLL where the loop filter is purely digital.

Table I summarizes the performance of the proposed VCO and PLL with on-chip calibration.

V. DISCUSSION

We now consider the impact of temperature variations on our calibration technique. A large change in temperature affects transistor threshold voltages significantly. An increase in the temperature causes the threshold voltage to reduce. As a consequence, both the voltage V_B and the currents in M_{n1} and M_{n2} increase (Fig. 9), leading to an over compensation. Thus, the relationship between the VCO supply sensitivity and I_B (Fig. 6) is shifted to the right for high temperatures. Fig. 19 shows the simulated VCO sensitivities as the temperature varies from 27 °C

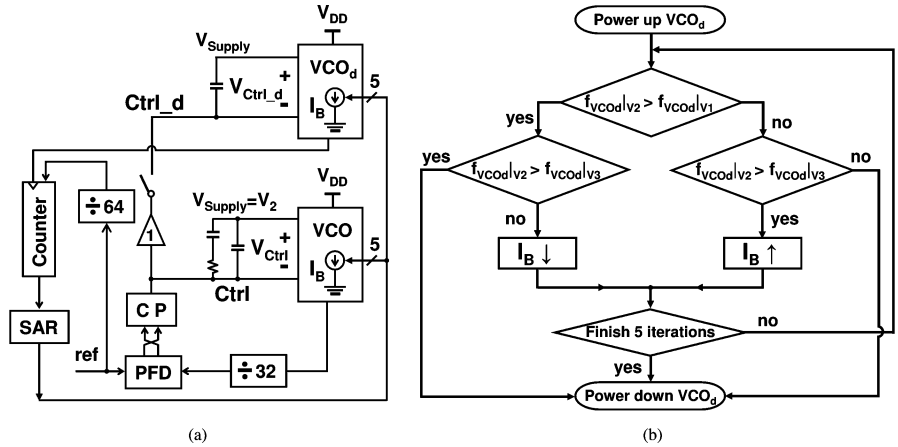

Fig. 21. Enhanced PLL with background calibration. (a) Schematic. (b) Flowchart.

to 120 °C. The optimum code has been changed by 8 LSBs, which can significantly impair the PLL performance. To ensure an optimum compensation over temperature variations, the VCO should be calibrated periodically.

Fig. 20 compares the measured jitter between 22 °C and 90 °C[3] in the presence of a 1-MHz supply noise. As expected, the curve is shifted to the right for a higher temperature. The optimum code changes from "01010" to "01101". A recalibration at 90 °C converges to the code "01011", which is also close to the optimum.

The initial calibration is performed after the system is powered up. As long as the noise in the supply voltage is much less than the difference between V_1 and V_3, a recalibration in a noisy environment has negligible impact on the obtained code. However, the PLL timing jitter may increase significantly during a recalibration, not only due to the break in the loop but also because the supply voltage alternates between V_3 and V_1. One method to tackle the problem is to recalibrate the PLL during system standby. Nevertheless, the system operation has to be interrupted. This is undesirable for many applications. To enhance the calibration technique, a background calibration would be desirable.

One way a background calibration can be implemented is by adding a dummy PLL. This dummy PLL can be periodically powered up to perform a calibration in order to obtain the code in I_B, while the main PLL maintains normal operation. An even simpler method is shown in Fig. 21(a). A dummy VCO has been added in parallel with the main VCO. The main VCO always operates with the supply voltage V_2. Fig. 21(b) shows the calibration algorithm, which is similar to the previous one. One calibration cycle has two phases. In each phase, the supply voltage of the dummy VCO is changed from V_2 to V_1 and from V_2 to V_3, respectively. At the beginning of each calibration phase, the dummy VCO uses a supply voltage V_2, and the switch is closed. Since both the supply voltage and the control voltage are the same for the two VCOs, their oscillation frequencies are also the same, assuming there is good matching between them. Then the switch is opened and the supply voltage of the dummy VCO is changed. The oscillation frequency also changes due to the change in the supply voltage. The dummy VCO output feeds a 12-bit counter to count the divided reference clock. The polarity of the change in the dummy VCO oscillation frequency can be detected by observing the MSB of the counter output. The calibration procedure would continue until either all five cycles are completed or until the polarity of the frequency change in one calibration cycle is the same between the two phases, which suggests that a close-to-zero sensitivity (given sufficient matching) is reached.

[3]A 104A-1 thermo probe was used in the measurement. However, the on-die temperature is unknown.

VI. Conclusion

A ring-oscillator-based PLL with an on-chip calibration technique enables successful integration of a supply noise insensitive PLL. Over a wide operating frequency range, the 1-V 0.13-μm CMOS prototype IC measurement results have confirmed robust operation in the presence of VCO supply noise. The proposed work rejects supply noise while avoiding the use of supply regulation, which makes the proposed technique more desirable in the design of low-voltage high-performance ring VCOs. A feasible implementation of a background calibration technique which would be robust to temperature variations has also been presented. The concepts presented in the context of the prototype analog PLL implementation can be easily migrated to a digital PLL.

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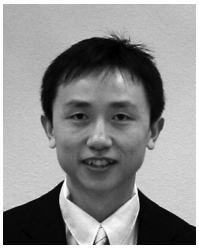

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