Design of Low-Voltage Highly Linear Switched-R-MOSFET-C Filters

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***Abstract*—This paper discusses the design, analysis and performance of a low-voltage, highly linear switched-R-MOSFET-C filter. High linearity, even at a low supply voltage, is achieved through the use of duty-cycle-controlled tuning. Tuning MOSFETs are switched completely on while conducting, such that their nonlinear resistance is much smaller than the linear filter resistors, resulting in low distortion. The MOSFETs are also placed inside the filter feedback loop which further reduces distortion. Because tuning is done in the time domain, rather than in the voltage domain, the tuning range is independent of the supply voltage. The filter achieves −77 dB total harmonic distortion (THD) using a 0.6-V supply, and −90 dB THD using a 0.8-V supply, with a 0.6-Vpp differential 2 kHz sine input. The prototype IC, implemented in a 0.18-μm CMOS process, occupies an area of 0.7 mm^2 and consumes 1 mW of power from a 0.6-V supply.**

***Index Terms*—Duty cycle control, linear, low voltage, master–slave tuning, pulse width modulation, R-MOSFET-C, switched filters, tunable filters.**

I. Introduction

THE continuous downscaling of transistor dimensions in CMOS technology has enabled digital IC systems to achieve increasingly higher speed and integration density. An important aspect of this downscaling trend is that supply voltages must be decreased along with transistor dimensions. While digital circuits benefit from supply voltage scaling with lower power dissipation, the design of low-voltage analog circuits that must co-exist with digital circuits poses many difficult challenges.

Analog filters are key building blocks in many systems. Like many other analog circuits, traditional filters are adversely affected by a low supply voltage. One of the most fundamental low-voltage issues in analog design is the reduction in available signal swing. To achieve the same dynamic range as their high-voltage counterparts, low-voltage circuits must achieve better noise and distortion performance. This is difficult because low-voltage operation exacerbates the nonlinearity, leading to more distortion.

Conventional switched-capacitor (SC) filters have difficulty working at low supply voltages because of the floating switch in the signal path. The fundamental limitation of a complementary floating switch in a SC branch occurs when the supply voltage becomes less than or equal to the sum of the absolute values of the pMOS and nMOS threshold voltages. In modern processes this limit is being reached because the threshold voltages are not scaled as aggressively as the supply voltage to avoid excess leakage current. A bootstrapped clock may be used to solve this problem, but it may lead to reliability issues [1].

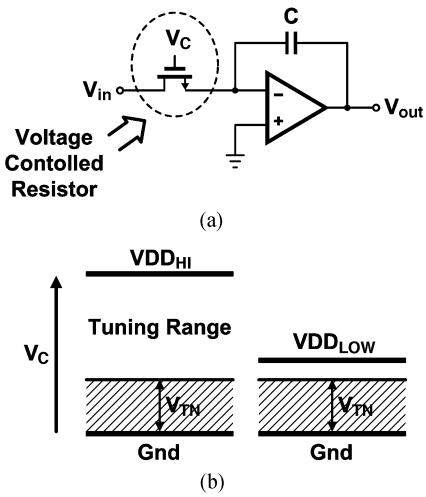

Fig. 1. (a) Simplified MOSFET-C integrator. (b) Tuning range comparison between high and low supply voltages.

Continuous-time (CT) filters are also strongly affected by a low supply voltage. One of the most critical issues in integrated CT filters is the corner frequency deviation caused by variations in process, voltage and temperature (PVT). PVT variations in CT integrated filters can cause a corner frequency variation of up to 50%. To suppress this time-constant variation, voltage-controlled tunable elements such as MOS resistors or MOS capacitors are often used. Fig. 1(a) shows the use of a triode MOSFET as a voltage-controlled resistor in a simplified single-ended MOSFET-C integrator. Problems occur when the supply voltage is lowered, because the tuning range of the voltage-controlled elements is lowered as well. The reduction in tuning range for the MOS resistor is illustrated in Fig. 1(b). A low supply voltage causes the resistance to become highly sensitive to variations in the control voltage and supply voltage. A decrease in supply voltage may also cause a decrease in the linearity of the MOS resistor. If the supply voltage is low enough, the available tuning range may not be enough to compensate for PVT variations.

In order to circumvent these low voltage issues, the switched-R-MOSFET-C (SRMC) filter has been developed. Several previous works have shown the use of variable timing to adjust

Manuscript received December 1, 2006; revised March 1, 2007. This work was supported by the Center for Design of Analog-Digital Integrated Circuits (CDADIC), the National Science Foundation under NSF CAREER CCR-0133530, and Analog Devices, Inc.

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Digital Object Identifier 10.1109/JSSC.2007.900280

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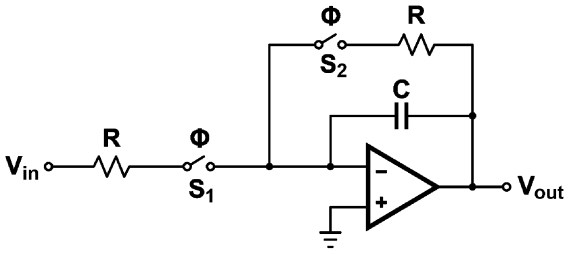


Fig. 2. Ideal first-order SRMC filter.

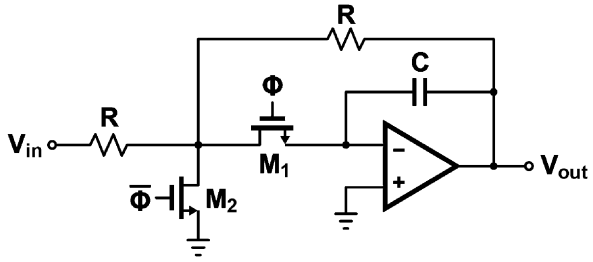


Fig. 3. Complete first-order SRMC filter.

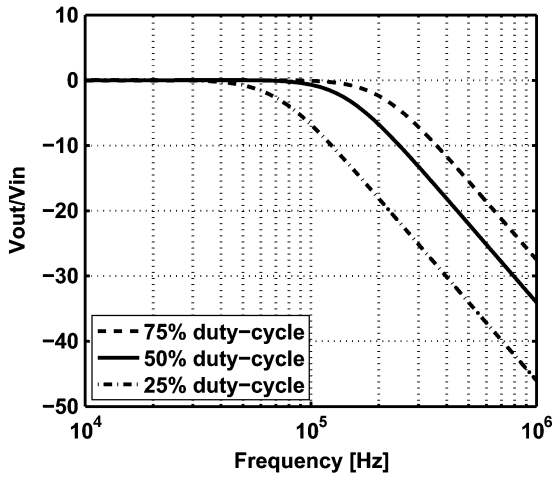


Fig. 4. Ideal first-order SRMC filter corner frequency tuning curves.

circuit time-constants [2]–[4]. The SRMC filter architecture [5] uses duty-cycle-based tuning as a means to achieve accurate time-constants, while maintaining high linearity and large tuning range at low supply voltages. This work describes the IC implementation and measurement results of a SRMC filter. Section II describes the SRMC filter architecture, Section III gives details of the circuit design, Section IV discusses modulation effects, Section V investigates noise folding effects, and finally Section VI presents measurement results of the fabricated IC.

II. System Architecture

The SRMC filter architecture uses the MOSFET as a switch, instead of a voltage controlled resistor as is done in continuous-time filters. This MOSFET switch, with on-resistance $R_{\rm on}$, is put in series with a resistor R to form an R-MOSFET branch (Fig. 2). A duty-cycle controlled clock is applied to the MOSFET gate to control the *average* resistance of the R-MOSFET branch. The average resistance of a duty-cycle controlled R-MOSFET branch is defined as the ratio of applied voltage to the average current which flows through the branch over one clock period. The average resistance is given by

$$R_{\rm ave} = \frac{R + R_{\rm on}}{d} \approx R/d \quad \text{for} \quad R_{\rm on} \ll R \tag{1}$$

where d is the duty-cycle of the applied clock and is defined as the ratio of on-time to clock period. Because tuning is done in time rather than in voltage, the tuning range is not compromised by a low supply.

To obtain an ideal SRMC filter, the resistors in a conventional active *RC* filter are replaced by the switched R-MOSFET branches (Fig. 2). The same duty-cycle controlled clock ϕ is applied to both switches such that the resistances of the R-MOSFET branches are controlled concurrently. By keeping the resistances of the R-MOSFET branches equal, tuning affects only the cutoff frequency of the filter but not the DC gain. The 3-dB cutoff frequency of the first-order SRMC filter is given by

$$\omega_{\rm cutoff} = \frac{1}{R_{\rm eq}C} \approx \frac{d}{RC}. \tag{2}$$

Because switches S_1 and S_2 operate with the same clock and connect to the same node, they can be combined into one switch. The complete first-order SRMC filter structure is shown in Fig. 3, with MOSFET M_1 being the combined switch. An additional switch M_2 is added which is driven with a complementary clock $\bar{\phi}$. The purpose of this switch is to steer current to ground while M_1 is off, such that the current loading through the resistor branches is consistent over both clock phases. This also helps to minimize signal feedthrough while M_1 is off. For M_2 to work properly despite changes in the duty-cycle of ϕ, the complementary clock $\bar{\phi}$ must have a duty-cycle of $1 - d$.

To compensate for process variations, the SRMC filter must have a corner frequency tuning range of at least $\pm 50\%$. By choosing to design the SRMC filter with a nominal 50% duty-cycle, a $\pm 50\%$ tuning range can be achieved with duty-cycles ranging from 25% to 75%. This choice of nominal duty-cycle maximizes the clock edge spacing over the $\pm 50\%$ tuning range. Fig. 4 shows the simulated small signal transfer function of the ideal first-order SRMC filter over the $\pm 50\%$ tuning range.

The component values of the SRMC filter can be obtained from a continuous-time active *RC* filter prototype with the same cutoff frequency. If we choose to keep all capacitor values the same for the active *RC* prototype and the SRMC filter, then (2) can be used to solve for the required resistor values in the SRMC filter. Using a nominal duty-cycle of 50% or $d = 0.5$, the SRMC filter resistors are found to be half that of the continuous-time active *RC* filter prototype resistors.

The SRMC filter shown operates as a filtered track-and-hold stage. By adjusting the ratio of track to hold time using the variable duty-cycle clock, the effective branch resistance and

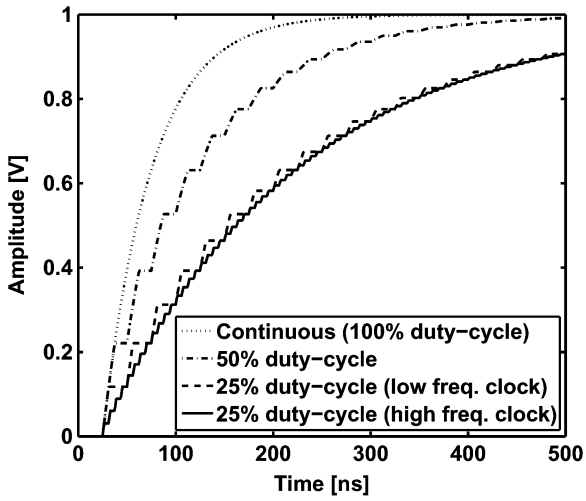


Fig. 5. Ideal first-order SRMC filter step response curves.

therefore the *RC* time-constant of the filter can be changed. The time-constant can be obtained from (2) as

$$\tau = \frac{1}{\omega_{\text{cutoff}}} \approx \frac{RC}{d}. \tag{3}$$

Fig. 5 shows the simulated step response of the ideal first-order SRMC filter with different duty-cycles and clock frequencies. The time-constant variation over duty-cycle predicted by (3) is apparent from the figure. 100% duty-cycle corresponds to the case where the switch M_1 is always conducting. This is the smallest time-constant the filter can achieve over its tuning range. The 25% duty-cycle case has been plotted with both a low-frequency and a high-frequency clock. By observing the two 25% duty-cycle curves, it can be seen that the time-constant is independent of the clock frequency. Though the curves alternate between track and hold at different frequencies, their trajectories are the same. High frequency modulation effects caused by switching will be discussed in Section IV.

The SRMC structure allows the circuit to operate with high linearity. Hold transistor M_1 is switched completely on while it is conducting, such that its nonlinear on-resistance is much smaller than that of the linear branch resistors R. Because the branch resistors are in series with the hold transistor M_1, most of the voltage is dropped across the linear resistors. This keeps the distortion contribution of M_1 low. Including M_1 in the filter feedback loop further reduces its distortion and increases the filter linearity [6]. The opamp gain required to reduce distortion to an acceptable level can be determined using feedback distortion analysis [7].

The SRMC filter is tuned using a master–slave tuning scheme (Fig. 6). The slave is the SRMC filter. The master contains an R-MOSFET resistor/capacitor set similar to those used in the SRMC filter. A feedback loop, created using the duty-cycle controlled clock ϕ, adjusts the resistance of the R-MOSFET branch in the master such that the R-MOSFET resistor/capacitor time-constant is equal to a reference time-period T_{ref}. This reference time-period is the period of an accurate reference clock ϕ_{ref}. Because the duty-cycle controlled clock ϕ is also applied

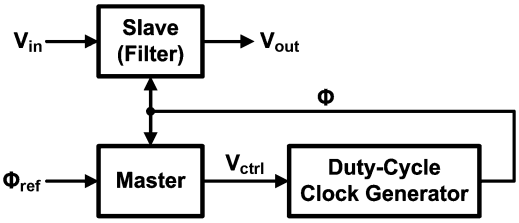


Fig. 6. SRMC master–slave tuning.

to the slave (SRMC filter), the filter will have time-constants proportional to T_{ref}.

III. Circuit Design

A. Biquad

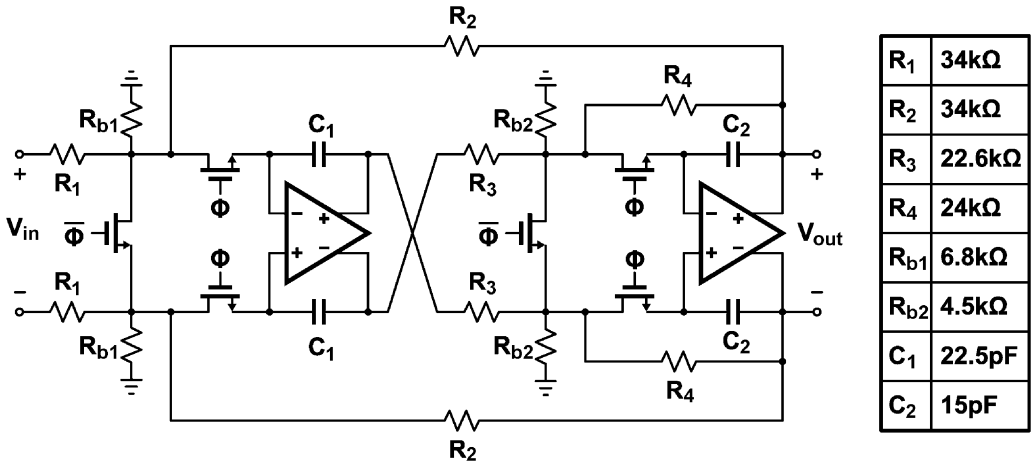
A second-order Butterworth low-pass filter was designed in a 0.18-μm CMOS technology to test the performance of the SRMC structure under low supply voltages. The SRMC filter was implemented in a biquad form shown in Fig. 7. Also shown are the implemented resistor and capacitor values used to achieve a 135-kHz corner frequency. The biquad is developed using the same methodology as described in Section II for the first-order filter. Additional resistors R_{b1} and R_{b2} have been added to bias the inputs of the differential opamps near ground. This allows the opamps with pMOS input pairs to work with a low supply voltage [8]. It also enables the switching MOSFETs to operate with a low-voltage clock. There are no floating switches in the circuit, and all terminal-to-terminal voltages are smaller than the supply voltage at all times.

The choice of bias resistor values presents a tradeoff between noise and distortion. A lower valued resistor lowers the switching MOSFETs drain and source bias voltages. This provides the switching MOSFETs with a higher overdrive voltage and therefore lowers its distortion. At the same time, a lower valued resistor lowers the feedback factor and increases the opamp noise gain to the output.

Common-mode charge injection from switching transistors is absorbed by the opamp CMFB. Even with differential mismatch between switches, charge injection is suppressed for the same reasons that nonlinearity of the switching transistors is suppressed. The filter feedback loop gain helps reduce charge injection errors and because the voltage drop across the switches is small, signal dependent charge injection is low. The SRMC filter architecture is resistant to charge injection errors from switching transistors, therefore these transistors can be sized large to help increase filter linearity.

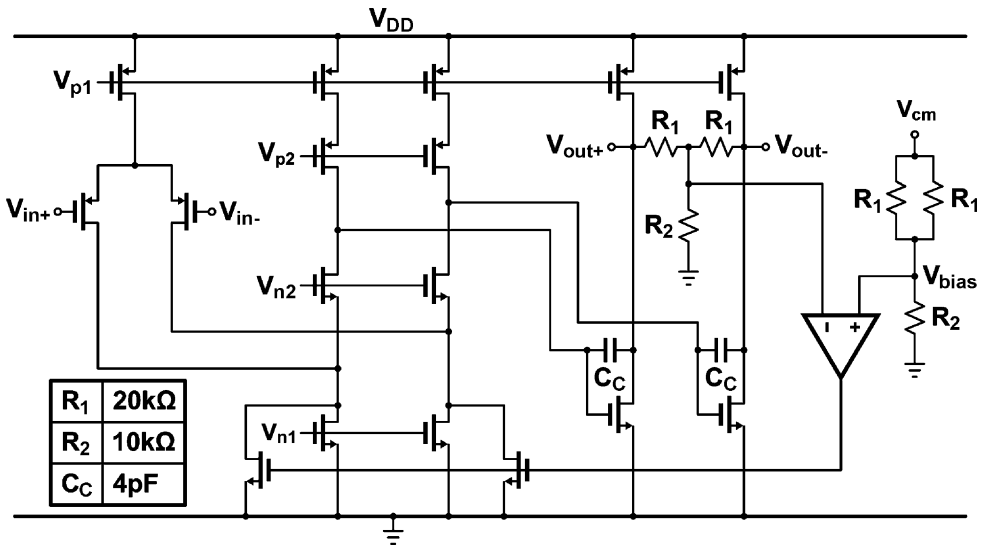
B. Filter Opamp

A low-voltage differential opamp was designed using a two-stage folded cascode structure (Fig. 8). Cascoding in the first stage is possible because the available output signal swing is reduced by the gain of the second stage. The second stage gain is approximately 35 dB. The opamp was designed to operate at supply voltages down to 0.6 V. The 0.6-V supply voltage is distributed over the cascode stack such that there is 100 mV across the top pMOS and bottom nMOS transistors, and 200 mV across the middle pMOS and nMOS transistors under DC conditions.



R_1	34kΩ
R_2	34kΩ
R_3	22.6kΩ
R_4	24kΩ
R_{b1}	6.8kΩ
R_{b2}	4.5kΩ
C_1	22.5pF
C_2	15pF

Fig. 7. SRMC biquad filter.



R_1	20kΩ
R_2	10kΩ
C_C	4pF

Fig. 8. Filter opamp.

Transistors in the cascode first stage have saturation voltages of approximately 80 mV. The nominal threshold voltage in this process is 450 mV. The threshold voltages of the input transistors have been lowered to 300 mV by increasing the transistor channel lengths from their minimum size. This relaxes requirements on the low-voltage biasing of the input common mode. The input transistors and the first-stage cascode top and bottom transistors have been sized for large area to reduce the opamp flicker noise. The opamp has an open loop gain of 70 dB and a bandwidth of 20 MHz.

The common-mode feedback circuit is a single-stage folded cascode opamp with pMOS inputs. The input pair is biased near ground with a resistive voltage divider made up of R_2 and common mode sense resistors R_1. This biasing is similar to that of the main opamp and allows low-voltage operation. The resistors have been chosen such that $R_2 = R_1/2$. For an output common-mode of $V_{\rm DD}/2$, $V_{\rm bias} = V_{\rm DD}/4$. By using resistor ratios to set the output common-mode voltage, the common-mode level is stable over process variations.

C. Master Stage

Fig. 9 shows the master tuning circuit, which is based on time-constant matching [9]. Tuning is performed with a differential structure to suppress charge injection and clock modulation. Considering one side of the differential structure, two branches feed into the input of an integrator. The outer branch is a SC resistor with average resistance $T_{\rm ref}/C_{\rm sc}$, where $T_{\rm ref}$ is the period of clock $\phi_{\rm ref}$. The inner branch is an R-MOSFET resistor with average resistance R/d, where d is the duty-cycle of clock ϕ. Any mismatch between the resistances of these branches causes current to flow into the integrator, which changes the control voltage $V_{\rm ctrl}$. The negative feedback loop controls the duty-cycle of ϕ and adjusts the average resistance of the R-MOSFET branch forcing it to be equal to the average resistance of the SC branch. Once the feedback loop reaches equilibrium, the average resistances of the the branches will be equal. Equating branch average resistances gives

$$T_{\rm ref} = C_{\rm sc}R_{\rm eq} \approx \frac{C_{\rm sc}R}{d}. \tag{4}$$

Equation (4) shows that the time-constant $C_{\rm sc}R_{\rm eq}$ can be set precisely if an accurate reference clock is used for $\phi_{\rm ref}$. R and $C_{\rm sc}$ are made up of the same unit elements as the resistors and capacitors used in the filter, and therefore the time-constants between the master and slave will track with process and temperature variation. The time-constants in the filter can be set as

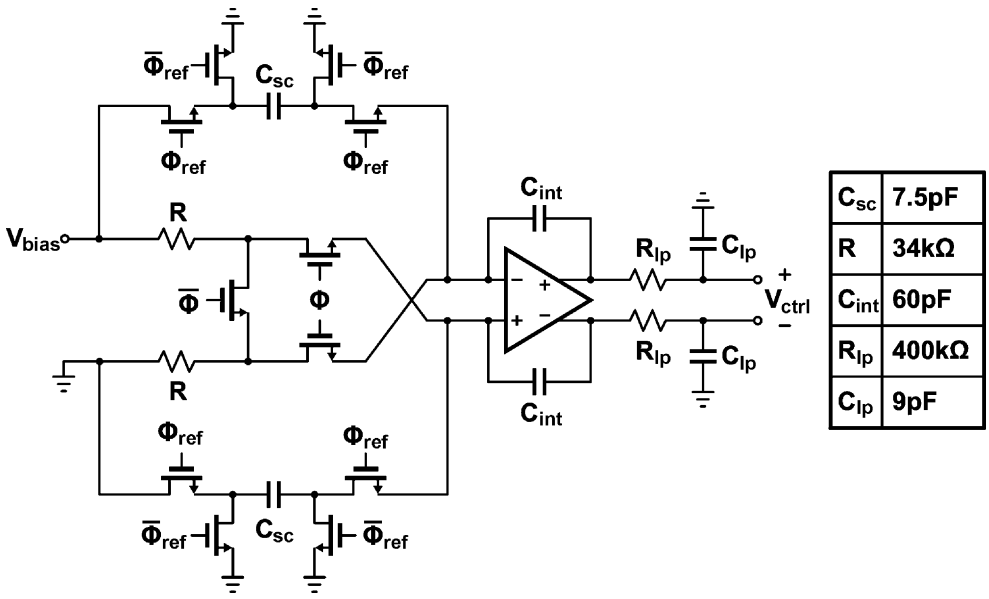


Fig. 9. Master circuit.

accurately as the matching between the master and slave allows. Note that $V_{\rm bias}$ is set to a low voltage ($\sim$100 mV) so there are no floating switches in the circuit.

Offset in the integrator causes cutoff frequency tuning error. The filter time-constant in presence of integrator offset is given by

$$\tau_{\rm off} = \tau_{\rm ideal}\left(\frac{V_{\rm bias} - V_{\rm off}}{V_{\rm bias} + V_{\rm off}}\right) \tag{5}$$

where $\tau_{\rm ideal}$ is the filter time-constant with no offset, $V_{\rm bias}$ is the branch bias voltage and $V_{\rm off}$ is the input referred opamp offset voltage. Opamp offset should be minimized to maintain high tuning accuracy.

If high level of cutoff frequency accuracy is needed, startup digital tuning can be used to reduce the master–slave mismatch to negligible levels [10]. The filter has been allowed 5 bits of digital tuning by implementing the capacitors $C_{\rm sc}$ as binary weighted capacitor arrays. $C_{\rm sc}$ can be varied manually $\pm$50% from its nominal value.

D. Duty-Cycle Clock Generator

The duty-cycle clock generator is shown in Fig. 10. The control voltage $V_{\rm ctrl}$ adjusts the charging of the capacitor C via a transconductance stage made from transistors M_1 to M_4. This transconductance stage uses nMOS and pMOS inputs to provide a large input range such that sufficient current can be provided to the capacitor while operating at low supply voltages. An inverter Inv_1 triggers when the capacitor has been charged to approximately $V_{\rm DD}/2$. Depending on the amount of current provided to the capacitor, the time until the inverter triggers can be changed, thereby adjusting the duty-cycle of the output clock. A large grounding transistor M_5 discharges the capacitor at the end of each clock cycle. The reset clock ϕ_o applied to this transistor defines the minimum duty-cycle of the output clock ϕ. This reset clock is created from $\phi_{\rm clk}$ using inverter delays. $\phi_{\rm clk}$ is a 50% duty-cycle off-chip clock. An extra inverter Inv_2 is placed after Inv_1 to provide buffering and to sharpen the clock edges. Inv_2 is followed by a non-overlapping clock generator, based on inverter delays, to provide duty-cycle adjustable complementary clocks ϕ and $\bar{\phi}$.

Transistor and capacitor sizing in this stage depends on filter switch gate-capacitance loading, clock frequency and minimum required duty-cycle. Filter switch loading is determined by the size of the filter switches, which was discussed in Section III-A. Inv_1, Inv_2, and duty-cycle generator must be sized to properly drive the filter switches. The capacitor C is then chosen to dominate over the the input parasitics of Inv_1 to provide a predictable capacitance. The value of C for the implemented filter is 0.5 pF. The reset transistor M_5 and its driving circuitry are sized to provide a proper reset pulse which defines the minimum duty-cycle of the output clock. M_1 to M_4 are sized to provide enough current to C such that the minimum duty-cycle can be achieved over the input swing of $V_{\rm ctrl}$.

The minimum clock frequency is determined by anti-aliasing filter requirements which will be discussed in Section IV. The maximum allowable clock frequency is determined by the rise and fall times of the reset clock ϕ_o, such that it is able to turn on the reset transistor M_5 at the minimum duty-cycle. If the clock frequency is too high, capacitor C will not be discharged properly and the output clocks will saturate to the supplies. The minimum duty-cycle which defines the width of ϕ_o is set by the required tuning range of the filter. The width of ϕ_o can be increased by adding more inverters to the reset pulse generator. In our chip, the duty-cycle generator has been designed for a clock frequency of 128 MHz.

IV. Modulation Effects

In the SRMC architecture, modulation of the input signal occurs, similar to that which takes place in a mixer. The input is modulated by the clock, and replicas appear at multiples of the clock frequency with a conversion gain determined by the Fourier series components of the clock waveform. The SRMC

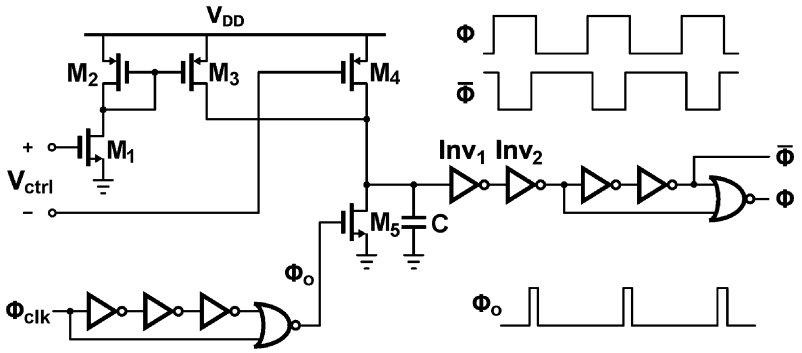


Fig. 10. Duty-cycle clock generator circuit.

filter, like a mixer, is a linear periodically time-varying (LPTV) system. The input–output behavior of an LPTV system can be characterized using harmonic transfer functions (HTFs). The Laplace domain input–output relation of an arbitrary LPTV system is given by

$$Y(s) = \sum_{n=-\infty}^{\infty} H_n(s)U(s - jn\omega_0) \tag{6}$$

where $H_n(s)$ are the HTFs of the system, $U(s)$ and $Y(s)$ are the input and output signals of the system, respectively, and $\omega_0 = 2\pi f_0 = 2\pi/T$, where T is the fundamental period of the LPTV system. This section describes the derivation of the HTFs of the SRMC filter.

Fig. 11(a) shows the block diagram of the ideal first-order SRMC filter derived from the circuit of Fig. 2. Switches in the ideal SRMC filter operate in the current domain, by either passing the full current or no current. They can therefore be represented as mixers whose duty-cycle controlled clock has been amplitude normalized to alternate between values of 1 and 0. In the frequency domain the mixing function becomes a convolution, with the normalized clock represented by its Fourier series components. The HTFs of this system can be obtained numerically using a harmonic balance method [11]. Though a numerical analysis provides accurate solutions for the HTFs, more insightful symbolic results can be obtained by making some simplifying observations.

We can simplify the block diagram of Fig. 11(a) by noting that the filter itself can act as both an anti-aliasing filter and a reconstruction filter for the mixer in the feedback path. Any high-frequency signals which are modulated down in frequency have already been attenuated by the filter. At the same time, any low-frequency signals which are modulated up in frequency are attenuated by the subsequent filtering. If we assume that the clock frequency f_{clk} is high compared to the bandwidth of the filter f_{cutoff}, then the filter provides sufficient attenuation of aliased components and only the baseband signal is passed. Using this assumption, the feedback path mixer can be replaced by a gain block whose value is the DC component of the normalized clock. The DC or average value of the duty-cycle controlled normalized clock is its duty-cycle or d. This gain block can be combined with the feedback voltage-to-current conversion of $1/R$ for a total feedback gain of d/R.

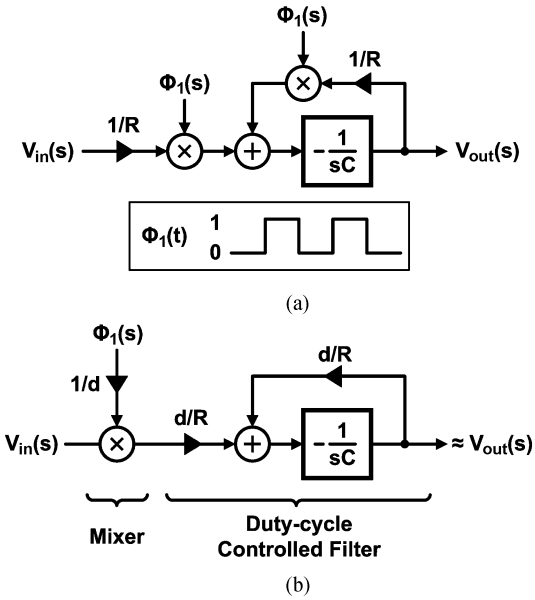


Fig. 11. (a) Block diagram of the ideal first-order SRMC filter. (b) Simplified block diagram of the ideal first-order SRMC filter, assuming a clock frequency much higher than the filter cutoff frequency.

Further simplification of the block diagram can be achieved by moving the input mixing function to the front of the filter, ahead of the voltage-to-current conversion. By adding a gain of d after the input mixer and a gain of $1/d$ after the clock input, the filter structure can be separated into a time-varying mixer followed by a time-invariant duty-cycle controlled filter. This simplified block diagram is shown in Fig. 11(b). The mixer section mixes the filter input with a clock whose duty-cycle is d and whose average value is 1. The mixer therefore has a gain of 1 for non-frequency-translated signals. The filter section has resistance values equal to the average equivalent resistance of a duty-cycle controlled R-MOSFET branch given by (1).

By removing the time-varying mixer from the filter feedback path, the HTFs of the simplified SRMC filter can be obtained symbolically as

$$H_n(s) = \frac{-sinc(nd)}{1 + s\dfrac{RC}{d}} \tag{7}$$

where $sinc(x) = sin(\pi x)/(\pi x)$. These symbolic HTFs closely match the numerically calculated HTFs for $f_{\rm clk} > 2f_{\rm cutoff}$. Symbolic HTFs can also be obtained using harmonic transfer matrices [12]. This method requires a similar simplification as was made above to simplify the time-varying feedback component. Using (6) and (7), the simplified input–output relation is given as

$$V_{\rm out}(s) \approx \frac{-\sum_{n=-\infty}^{\infty} sinc(nd)\cdot V_{\rm in}(s-jn\omega_{\rm clk})}{1+s\dfrac{RC}{d}}. \quad (8)$$

Fig. 11(b) and (8) show that the mixing function occurs before filtering, therefore an anti-aliasing filter is required. Unlike SC filters, the SRMC filter has no opamp/capacitor settling time requirements. The clock frequency can be set arbitrarily high, limited only by the ability of the switching transistors to turn on for a minimum duty-cycle. By making the clock frequency high, the requirements of the anti-aliasing filter are greatly reduced compared to a SC filter. The anti-aliasing filter bandwidth can be much higher than the SRMC filter bandwidth and therefore need not be tuned. The anti-aliasing filter can also be implemented with a low-order filter.

V. Noise Folding

The two dominant noise sources that affect the performance of the filter are resistor noise and opamp noise. Noise from the switching MOSFETs is negligible compared to that of the resistors and opamps, because the on-resistance of the switches is small compared to the filter resistors. Clock phase noise is another noise source that has been measured to cause only minimal noise performance degradation. Clock phase noise will mix with the input signal and appear at the output after filtering. With no input signal, phase noise from the clock has no effect on filter noise performance. When an input signal was applied to the prototype filter, the measured increase in noise was negligible, showing that clock phase noise has a minimal effect on output noise. This section derives the output-referred noise for the dominant noise sources in the first-order SRMC filter. At the end of each derivation, the noise in the SRMC filter is compared to that of a continuous-time (CT) filter.

Thermal noise from the filter resistors can be modeled by white noise voltage sources in series with the resistors as shown in Fig. 12. Assuming equal valued resistors, both noise sources have the same HTFs to the output. The HTFs of these noise sources are the same as that of the filter, given by (7). As was shown in Section IV, the filter HTFs can be obtained by modeling the filter as a mixing function followed by a filtering function.

When white noise is mixed with a clock signal, in the frequency domain the noise power spectral density (PSD) is replicated and scaled by the squared value of each of the Fourier series coefficients of the clock. Each of these replicas is considered a noise sideband. Because the noise is white, noise in separate sidebands are uncorrelated and their PSDs simply add [13]. The summation of noise from separate sidebands caused by mixing with a clock signal can be viewed as stacking of the PSDs. Also known as noise folding, this process is depicted

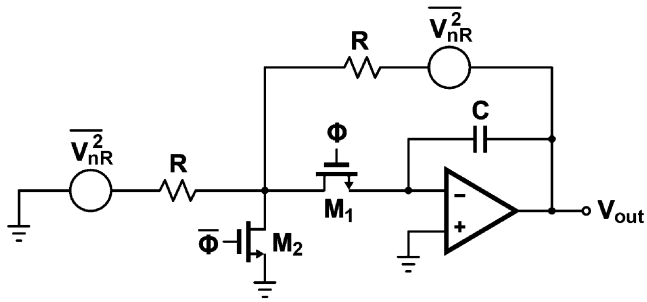


Fig. 12. Resistor thermal noise sources.

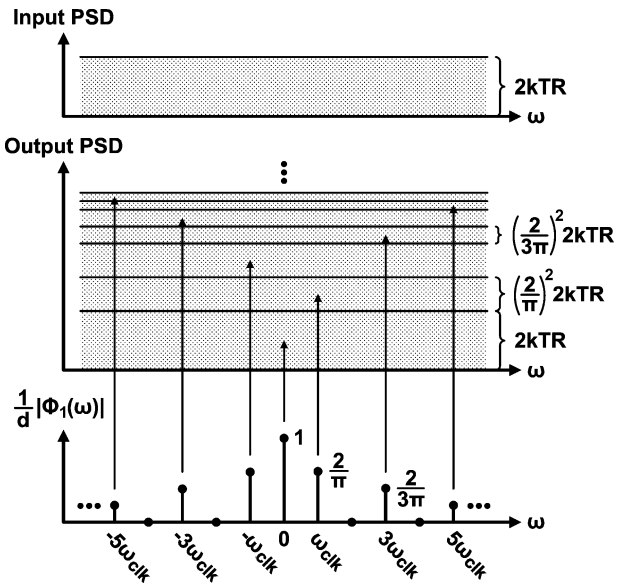


Fig. 13. Noise folding caused by mixing white noise with a duty-cycle normalized clock for a duty-cycle of 50%.

in Fig. 13 for a duty-cycle normalized clock with a duty-cycle of 50%. Because the noise is wideband, frequency translation of the noise has little influence on the shape of the PSD at the mixer output. After folding, the noise is then low-pass filtered before appearing at the SRMC filter output. Assuming that the filter bandwidth is much lower than the clock frequency, low-pass filtering removes the cyclostationarity from the noise at the mixer output. The noise at the output of the filter can be considered to be stationary and can be characterized using the time-average PSD.

The time-average output PSD from each noise source can be obtained using the input–output PSD relation, which is analogous to (6)

$$\tilde{S}_y(\omega) = \sum_{n=-\infty}^{\infty} H_n(\omega) S_u(w - n\omega_0) H_n^*(\omega) \quad (9)$$

where * denotes complex conjugation. This equation relates the output time-average PSD $\tilde{S}_y(\omega)$ to the input PSD $S_u(\omega)$ and HTFs $H_n(\omega)$ [14]. To obtain the output PSD from the resistor thermal noise, we assume that the HTFs $H_{Rn}(\omega)$ are given by (7), and the input resistor thermal noise is modeled as white

noise with double-sided PSD $S_{nR} = 2kTR$. The output time-average PSD is therefore given by

$$\tilde{S}_{\mathrm{out}R}(\omega) = \sum_{n=-\infty}^{\infty} S_{nR} \left|H_{Rn}(\omega)\right|^2 \tag{10}$$

$$= 2kTR \sum_{n=-\infty}^{\infty} \frac{sinc^2(nd)}{1+\left(\omega\dfrac{RC}{d}\right)^2} \tag{11}$$

$$= 2kTR \frac{1/d}{1+\left(\omega\dfrac{RC}{d}\right)^2} \quad \text{for } 0 < d \leq 1. \tag{12}$$

This result closely matches simulated data.

We can now compare this output-referred resistor noise PSD to that of an equivalent CT filter given by

$$S_{C\mathrm{out}R}(\omega) = 2kTR_c \frac{1}{1+(\omega R_c C_c)^2}. \tag{13}$$

Here, R_c and C_c are the continuous-time resistor and capacitor values, respectively. In Section II, we found that when the filter bandwidth and capacitor values are kept the same between the CT and SRMC filters, the CT filter resistance is given as $R_c = R/d$. The CT filter output PSD can therefore be written as

$$S_{C\mathrm{out}R}(\omega) = 2kTR \frac{1/d}{1+\left(\omega\dfrac{RC_c}{d}\right)^2}. \tag{14}$$

This CT filter output PSD is the same as the SRMC filter output PSD of (12). This derivation shows that the noise contribution from the filter resistors in the SRMC filter is the same as that of an equivalent CT filter, independent of duty-cycle.

A second major contributor of noise is the opamp, which contributes both thermal noise and flicker noise. Flicker noise is low frequency in nature and does not experience noise folding, therefore it can be analyzed using continuous time techniques. For this reason, only thermal noise is analyzed in this section. Thermal noise from the opamp can be modeled as a white noise source at the opamp input, as shown in Fig. 14. The HTFs of the opamp noise voltage to the filter output are given by

$$H_{\mathrm{AMP}n}(\omega) = \begin{cases} \dfrac{sinc(nd)}{1+j\omega\frac{RC}{d}} & \text{for } n \neq 0 \\ \dfrac{2+j\omega\frac{RC}{d}}{1+j\omega\frac{RC}{d}} & \text{for } n = 0. \end{cases} \tag{15}$$

A similar procedure as was used to derive the output-referred resistor noise PSD can be used to find the output-referred opamp noise PSD. The output-referred opamp noise PSD is found to be

$$\tilde{S}_{\mathrm{outAMP}}(\omega) = S_{n\mathrm{AMP}} \frac{1/d+3+\left(\omega\dfrac{RC}{d}\right)^2}{1+\left(\omega\dfrac{RC}{d}\right)^2}. \tag{16}$$

Again, this symbolic result closely matches simulated data.

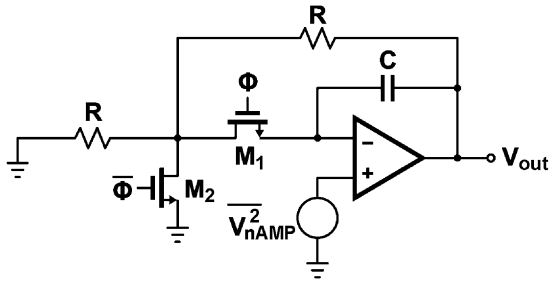


Fig. 14. Opamp thermal noise source.

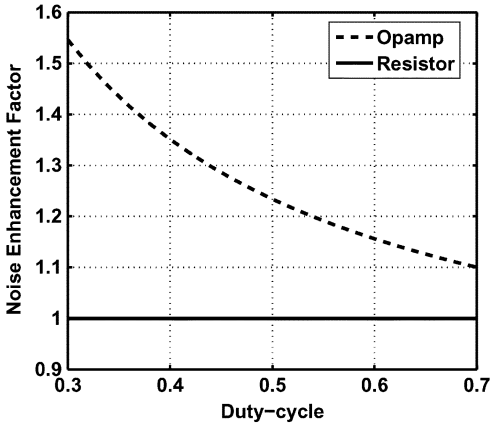


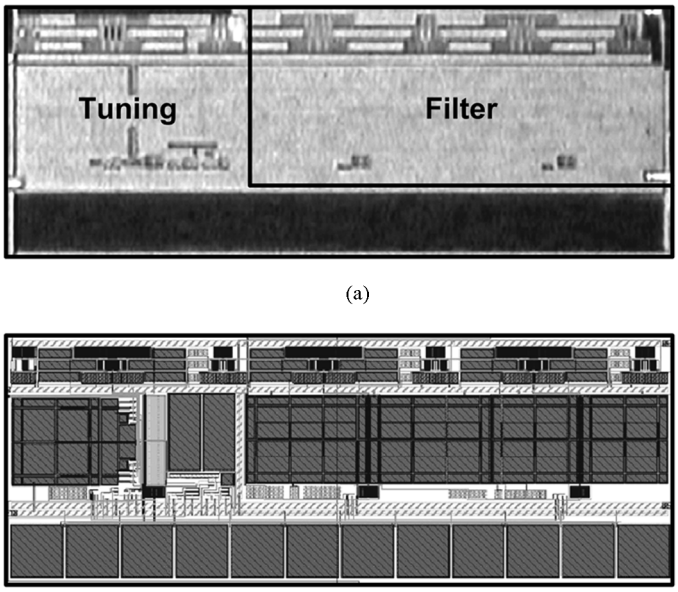
Fig. 15. Noise enhancement factor.

We can now compare this output-referred opamp noise PSD to that of an equivalent CT filter given by

$$S_{C\mathrm{outAMP}}(\omega) = S_{n\mathrm{AMP}} \frac{4+(\omega R_c C_c)^2}{1+(\omega R_c C_c)^2}. \tag{17}$$

Comparing the opamp noise PSD in the SRMC filter to that of the CT filter, we see a duty-cycle dependency in the first term of the numerator of the SRMC filter PSD. For this ideal case, the output noise from the opamp will be slightly higher in the SRMC filter compared to the CT filter. In reality, the finite bandwidth of the opamp will limit the noise folding that occurs. For opamp bandwidths much lower than the clock frequency, the noise contribution from the opamp will be the same in the SRMC filter as in the CT filter. The results given above are therefore a worst-case noise analysis of opamp noise.

To obtain an overall comparison between noise in the SRMC filter and the noise in a CT filter, we define a metric called the noise enhancement factor. The noise enhancement factor is the output noise of the SRMC filter normalized to that of the CT filter. Fig. 15 shows the noise enhancement factor plotted versus duty-cycle for the resistor and opamp noise sources. In the calculation of opamp noise, the PSD has been integrated to the bandwidth of the filter ω_{cutoff}. As shown previously, resistor noise in the SRMC filter is equal to that of an equivalent CT filter, therefore the noise enhancement factor is 1 over all duty-cycles. Noise from the opamp is at most 25% higher in the SRMC filter compared to a continuous-time filter at the nominal 50% duty-cycle.



(a)

(b)

Fig. 16. (a) Die micrograph. (b) Layout.

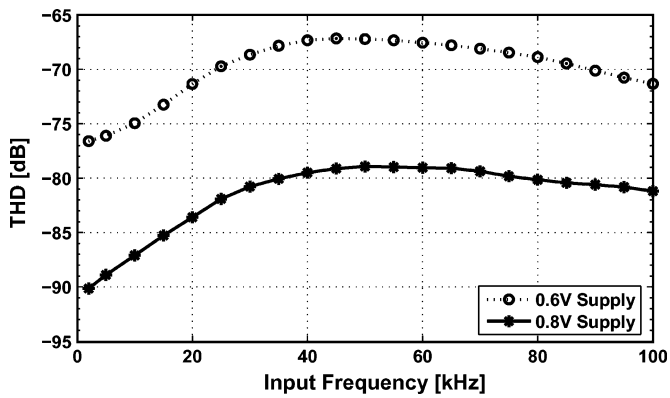


Fig. 17. Measured harmonic distortion.

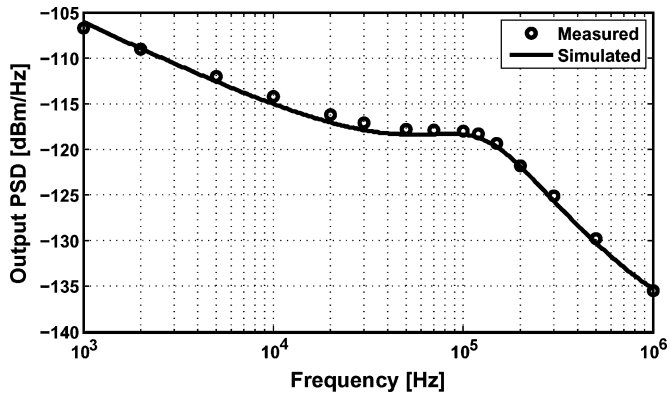


Fig. 18. Measured and simulated output noise power spectral density.

VI. Experimental Results

The prototype IC was fabricated in a 0.18-μm CMOS technology. The die micrograph and layout are shown in Fig. 16. The active die area is 0.5×1.4 mm^2. Fig. 17 shows the measured total harmonic distortion (THD) of the filter over an input frequency range of 2 kHz to 100 kHz, for 0.6-V and 0.8-V supply voltages. The input sinusoid was held at 0.6 Vpp differential in both cases. The linearity of the filter is limited by the opamp distortion. Fig. 18 shows the measured and simulated output noise PSDs of the filter. As can be seen, the measured PSD closely matches the simulated PSD. The measured filter response of five chips is shown in Fig. 19. The measured -3 dB cutoff frequency of 135-kHz has a standard deviation within 5%. In order to demonstrate the full tuning range capability of the filter, the cutoff frequency of one sample was varied by changing the reference clock frequency. The measured filter response over a tuning range of $\pm 50\%$ is shown in Fig. 20. Figs. 21 and 22 show

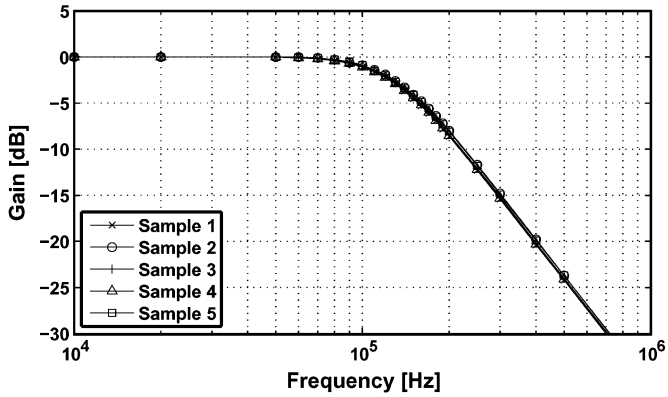


Fig. 19. Measured filter response of five chips.

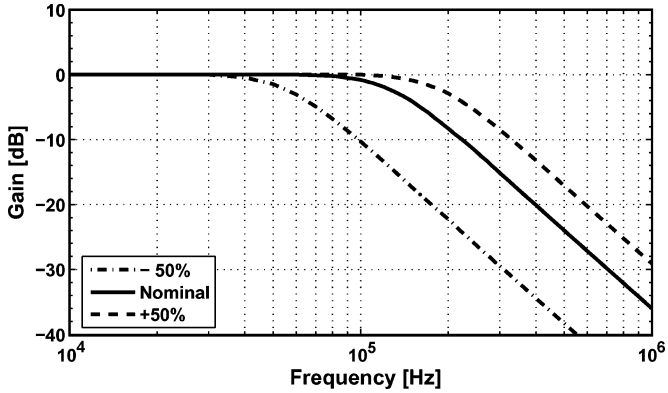


Fig. 20. Measured filter response over a $\pm 50\%$ tuning range.

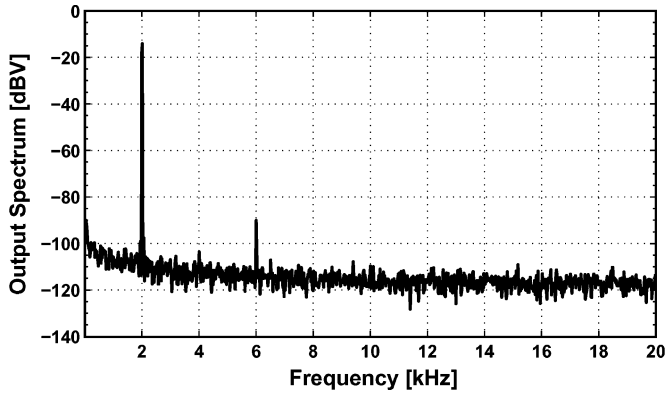


Fig. 21. Measured output spectrum at 0.6 V with 0.6-Vpp 2-kHz input.

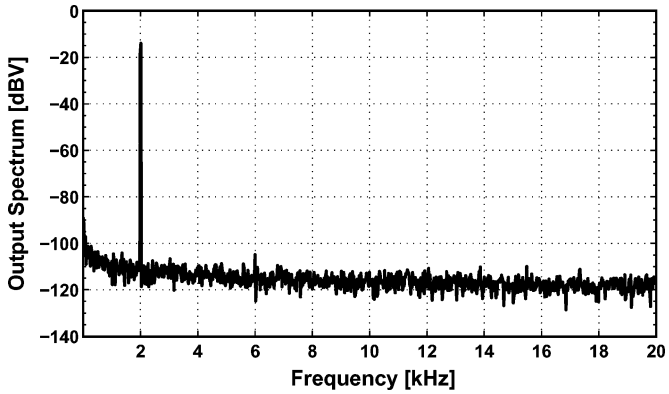


Fig. 22. Measured output spectrum at 0.8 V with 0.6-Vpp 2-kHz input.

TABLE I
PERFORMANCE SUMMARY

Supply voltage	0.6V	0.8V
THD Vin = 0.6Vpp diff. @ 2-kHz	-77dB	-90dB
IIP3	20dBV	27dBV
1dB Compression Point	-11dBV	-8.7dBV
SNR Vin = 0.6Vpp diff.	64dB	64dB
Power consumption	1mW	1.2mW
Filter type	2^{nd}-order Butterworth	
Cutoff frequency	135-kHz	
Clock frequency	128-MHz	
Die area	0.5×1.4 mm^2	
Technology	0.18μm CMOS	

the output spectrum at 0.6-V and 0.8-V supplies with a 0.6-Vpp 2-kHz input signal.

The performance summary of the filter is presented in Table I. All dB values given here and in Table I are referred to a 0.6-Vpp differential sinusoid. This prototype achieves −77-dB THD and 64-dB SNR with a 0.6-V supply voltage and 0.6-Vpp differential 2-kHz sine input. With a 0.8-V supply, the THD can be as low as −90 dB. Intermodulation measurements were taken with a center frequency of 5 kHz and an offset of 500 Hz. Noise is integrated from 1 kHz to 200 kHz. The circuit power consumption is 1 mW at 0.6 V and 1.2 mW at 0.8 V. The filter performance was measured with a 128-MHz clock frequency. Clock feedthrough and charge injection were below the noise floor of 130 dB. The measured PSRR is 28 dB over the bandwidth of the filter. The filter can operate down to 0.5-V supply with some performance degradation.

VII. CONCLUSION

The SRMC filter architecture allows highly linear and accurate operation at low supply voltages through the use of duty-cycle-based tuning inside a feedback loop. Because the tuning MOSFET is switched completely on when it is conducting, its nonlinear resistance is much lower than that of the linear filter resistors. Most of the voltage drop occurs across the linear resistors, so that distortion from the tuning MOSFET is suppressed. Including the tuning MOSFET in the filter feedback loop further decreases the distortion. Because tuning is done in the time domain rather than the voltage domain, the tuning range is independent of the supply voltage. The measured performance of the prototype IC fabricated in a 0.18-μm CMOS technology confirms the expected advantages of the proposed design techniques.

ACKNOWLEDGMENT

The authors would like to thank National Semiconductor for providing fabrication of the prototype IC and Prof. L. Lucchese for useful discussions.

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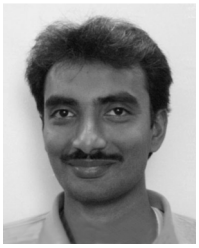

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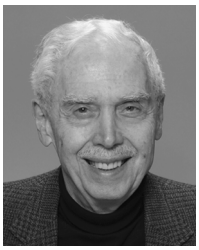

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