A 0.5-GHz to 2.5-GHz PLL With Fully Differential Supply Regulated Tuning

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***Abstract*—This paper describes a wide-range clock generation phase-locked loop (PLL) incorporating several features that make it suitable for integration in highly scaled processes. A fully differential supply regulated tuning scheme is used to combat power supply noise. The charge pump uses a resistor rather than an active current source to define the pumping current in order to reduce the charge pump flicker noise. Fabricated in a 0.18-μm CMOS process, the PLL occupies 0.15 mm^2 die area and achieves a frequency range of 0.5 to 2.5 GHz. When operating at 2.4 GHz, the power consumption is 14 mA from a 1.8-V supply while the jitter is 2.36 ps rms.**

***Index Terms*—Phase-locked loop, power supply noise, supply regulation, charge pump, flicker noise, voltage-controlled oscillator.**

I. Introduction

As INTEGRATED circuit fabrication technologies progress, reduced minimum feature size and supply voltages improve the speed, power consumption, and die area consumption of digital circuitry. This trend toward higher levels of integration, however, complicates the design of the supportive analog circuitry by increasing device noise, increasing mismatch, and decreasing supply voltage. One of these important analog circuits is the phase-locked loop (PLL) that is used to generate and distribute clocks in all high-performance digital systems.

This paper describes a PLL design well suited to highly integrated digital environments [1]. The rest of this introduction is divided into two parts: the first discusses the PLL design issues specific to such highly integrated environments while the second reviews PLL noise issues. The issues raised provide the motivation for the two unique ideas used in this work which are described in Sections II and III: fully differential supply regulated tuning and a low flicker noise charge pump, respectively. The phase-frequency detector (PFD) and divider designs are briefly covered in Section IV. Finally, measurement results are shown in Section V before conclusions are drawn in Section VI.

A. Integration Issues

A typical application where a PLL would face the aforementioned integration problems is shown in Fig. 1. High levels of integration lead to large digital systems that must be partitioned into many smaller subsystems in order for the design to be manageable and efficient. Each subsystem operates at a different frequency as speed requirements will vary and, therefore, each requires its own clock generation PLL. Rather than design a separate PLL optimized for each frequency, a single wide-range design is desirable.

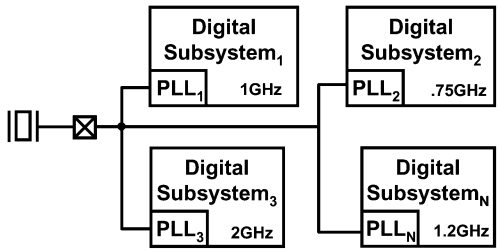

Fig. 1. Typical highly integrated clock generation PLL application.

Having many instances of the PLL integrated on the same die means that die area consumption is critical. This die area constraint and the need for a wide tuning range mandates the use of a ring voltage-controlled oscillator (VCO). Integrating many PLLs also magnifies the importance of power consumption. Since the PLL will cover a wide range of frequencies, it is important that the design be power efficient over the entire frequency range.

Another major consequence of the highly integrated environment is that the digital circuitry will induce switching noise on the PLL supply. Scaling trends allow higher levels of digital functionality, which increases these switching currents. At the same time, the supply voltage is shrinking because of power considerations. Therefore, supply noise is quickly becoming a larger fraction of the total supply voltage and any reasonable deep-submicron PLL design must have good supply noise immunity.

B. PLL Noise Issues

The most critical performance specification for PLL clock generators is jitter. Any uncertainty in the clock provided by the PLL subtracts from the timing margins for the digital logic and ultimately limits the speed of the digital system. An important step in clock generation design is to identify the PLL blocks that are the major contributors to jitter.

One of these noise critical blocks is the VCO. In fact, ring VCOs are known to be particularly noisy. It can be shown that VCO jitter due to intrinsic noise sources (thermal and flicker) is reduced when the delay cells are designed for high swing and fast switching [2]. Such delay cells, however, operate by

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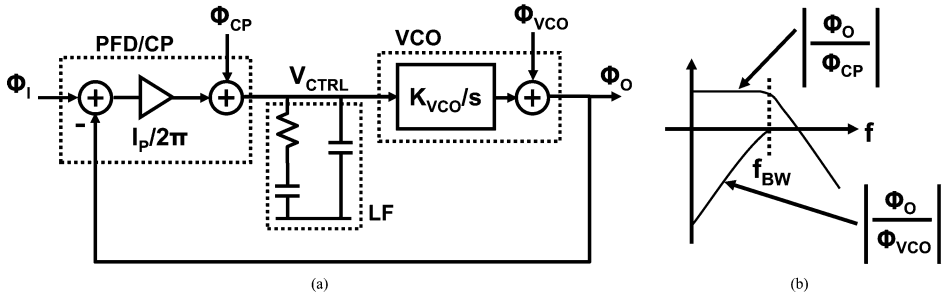

Fig. 2. (a) PLL block diagram. (b) Charge pump and VCO noise transfer functions.

charging a load capacitance through a low resistance switch connected to either ground on the falling edge or $V_{\rm DD}$ on the rising edge (e.g., an inverter). The problem with these full-swing delay cells is, therefore, that they are very sensitive to the supply voltage.

The charge pump is the second major PLL noise contributor. Using the block diagram shown in Fig. 2(a), transfer functions from the charge pump and VCO to the PLL output can be calculated, revealing the relevant noise band for each. The charge pump transfer function is found to be low-pass while the VCO transfer function is high-pass with an equal bandwidth [3], [4] [see Fig. 2(b)]. This exposes a bandwidth tradeoff that restricts the designer. A low bandwidth reduces low-frequency charge pump noise contribution at the cost of increasing the high-frequency VCO noise contribution, whereas a high bandwidth reduces the VCO noise contribution while increasing the charge pump noise contribution.

For our application, it was determined that the VCO noise was a more inherent noise source and a wide bandwidth was chosen to suppress it. Therefore, the reduction of low-frequency charge pump noise became essential. In deep-submicron processes, flicker noise is dominant at low frequencies. In fact, the flicker noise corner was found to be comparable to the wide PLL bandwidth, so that charge pump flicker noise was largely unsuppressed while thermal noise was mostly suppressed. The charge pump described in Section III circumvents this problem by using a unique architecture that drastically reduces the charge pump flicker noise corner.

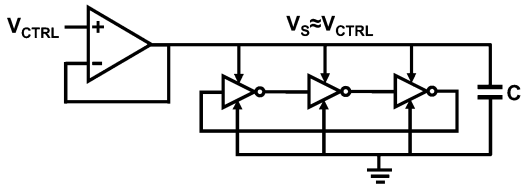

Fig. 3. Supply regulated tuning concept.

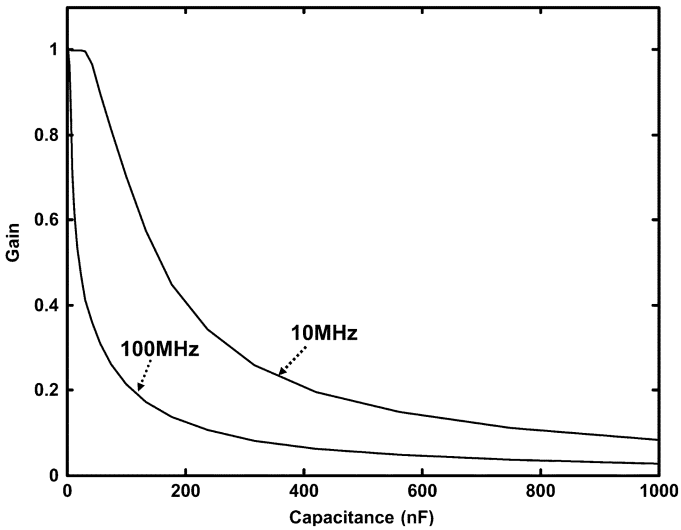

Fig. 4. Ground noise to differential supply noise gain as a function of decoupling capacitance.

II. Fully Differential Supply Regulated Tuning

Single-ended supply regulated tuning is an existing technique [5], [6] that makes use of the fact that the oscillation frequency of full-swing VCOs is proportional to the supply voltage. Therefore, the supply voltage of the delay cells can be used as the control voltage as shown in Fig. 3. This isolates the delay cells from the positive supply. The buffer in Fig. 3 is needed to keep the VCO from loading the loop filter and is essentially a supply regulator.

This regulation loop is able to isolate the positive supply of the delay cells from noise on the positive external supply, but has no effect on the ground noise. Therefore, a decoupling capacitor is added between the positive supply and ground to keep the difference constant in the presence of ground noise. For a finite decoupling capacitor, however, the translation of ground noise to common-mode noise is imperfect and some amount of ground noise will appear as differential supply noise. Fig. 4 shows the simulated ground noise to differential supply noise gain as a function of decoupling capacitance for 10-MHz and 100-MHz sinusoidal ground noise. As expected, for small capacitance values, the capacitor couples the positive supply to ground very poorly and almost all of the ground noise appears as differential supply noise $(\mathrm{Gain} = 1)$. As the capacitor size increases, the coupling improves and approaches perfect coupling $(\mathrm{Gain} = 0)$ for very large capacitance. It is also expected that faster noise components will be better coupled, so the 100-MHz noise is the best case.

If we use the liberal estimate of ground noise as a single high-frequency (100-MHz), 50-mV tone, a 120-nF capacitor is required to reduce this noise to 10 mV. A MOS capacitor of this size would be approximately 100 times larger than the entire active die area of the chip described in this paper.

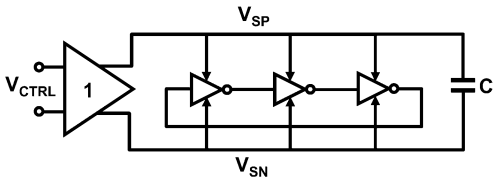

Fig. 5. Fully differential supply regulated tuning.

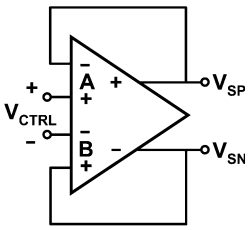

Fig. 6. Fully differential buffer.

In this work, rather than regulating the positive supply and relying on a large capacitor to couple the positive and negative supplies, both supplies are included in the regulation loop. This can be achieved by using the difference between positive and negative delay cell supplies as a differential control voltage as shown in Fig. 5. A much smaller decoupling capacitor is included to reduce noise not attenuated by the imperfect regulation loop and for stability of the regulation loop (see the Appendix for details). Fully differential tuning also accommodates a fully differential charge pump and loop filter which isolates those blocks from supply noise. Another benefit is that the need for a low-to-high-swing converter is eliminated since the common-mode feedback of the fully differential buffer will force the common-mode of the oscillator output to midrail. Although not available for this work, a triple-well process should be used when possible so that the bulks of the nMOS devices in the delay cells can also be isolated from the negative supply.

The fully differential buffer needed for fully differential supply regulated tuning is not a simple extension of the single-ended case, as that would lead to an operational amplifier (opamp) with both outputs shorted to both inputs. Instead, the two-input opamp in unity gain configuration shown in Fig. 6 can be used. The problem with opamps in unity gain configuration is that the input common-mode range limits the output swing which, in this case, limits the VCO tuning range. Noticing, however, that the input pair labeled "A" in Fig. 6 will be forced by the loop to be approximately equal to the positive supply voltage of the delay cells, which is always above midrail, it is possible to use an nMOS input pair to achieve a large input common-mode range. Similarly, pair "B" can achieve a large input common-mode range by using a pMOS input pair. The resulting opamp is shown in Fig. 7.

The amount of current consumed by the ring VCO is proportional to the oscillation frequency and inversely proportional to the jitter. Therefore, a high-speed low-jitter VCO requires the opamp to provide a prohibitively large current. A solution is to add transistors between the external supply ($V_{\rm DD}$ and ground) and the internal supply ($V_{\rm SP}$ and $V_{\rm SN}$), so that current is drawn from the external supply rather than the output of the opamp. Another benefit of adding these transistors is that the output

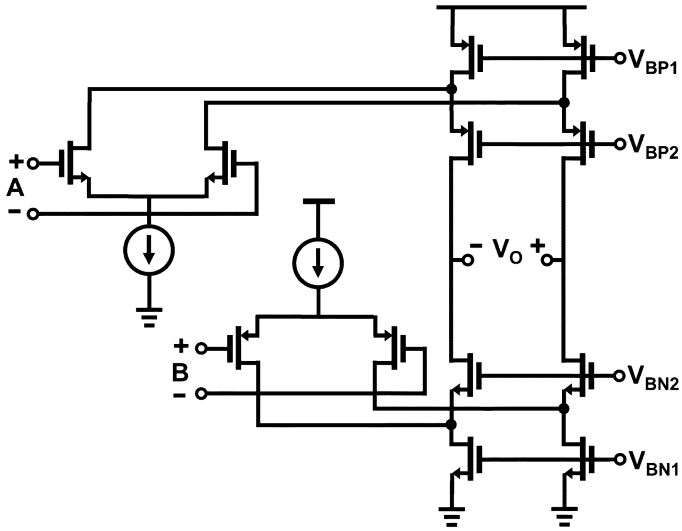

Fig. 7. Two-input-pair fully differential buffer opamp with large input common-mode range.

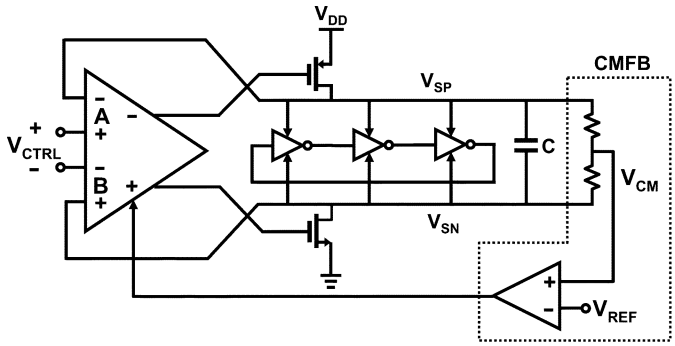

Fig. 8. Final VCO configuration.

swing requirements of the opamp are relaxed. The final VCO configuration incorporating this idea is shown in Fig. 8. A minimum number (3) of basic inverter delay cells are used to minimize parasitics and noise-contributing transistors. The single-ended nature of the inverter delay cells is tolerated because of supply regulation. As shown in Fig. 8, poly resistors are used to sense the common-mode of the delay cell supplies and a simple feedback loop forces this common-mode voltage to midrail.

There are several considerations in the design of the supply regulation loop, including stability, bandwidth, dropout, and peaking in the transfer function from the external to internal supply. The Appendix gives detailed information on this design process.

As mentioned earlier, low-power operation that scales well with frequency is an important consideration in wide-range PLL design [7]. Power consumption in full-swing ring VCOs can be expressed as

$$P \propto I_{\rm PEAK} V_{\rm DD} f_{\rm osc} \tag{1}$$

where P is the power, $I_{\rm PEAK}$ is the peak current drawn by the delay cell during switching, $V_{\rm DD}$ is the supply voltage, and $f_{\rm osc}$ is the frequency of oscillation. For traditional tuning methods where the VCO output swing is constant over the tuning range, $I_{\rm PEAK}$ and $V_{\rm DD}$ are also constant over the tuning range, and

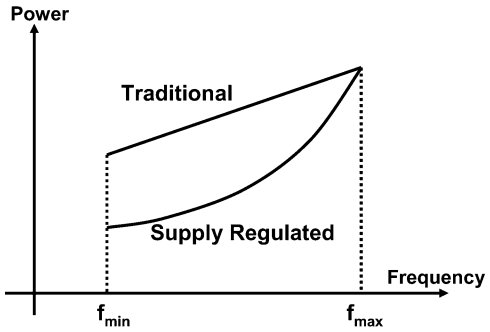

Fig. 9. Power savings of quadratic scaling compared to linear scaling.

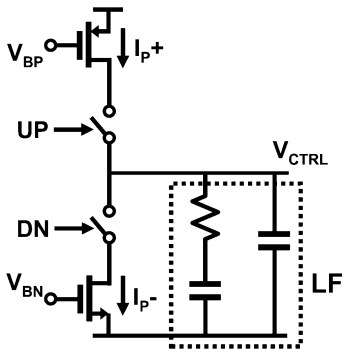

Fig. 10. Traditional charge pump.

power scales linearly with the oscillation frequency. Supply regulated tuning, on the other hand, scales the internal supply of the delay cells with frequency, which means that I_{PEAK} scales with frequency. Therefore, the power in the supply regulated tuning case is proportional to f_{osc}^2 and the scaling with frequency is quadratic. Fig. 9 illustrates how quadratic scaling gives significant power savings for the lower end of the VCO tuning range.

III. Low Flicker Noise Charge Pump

As explained earlier, charge pump flicker noise is a problem in deep-submicron PLL designs. A potential solution to this problem is to find a way to use a flicker-noise-free passive device to define the charge pump current rather than an active device with large flicker noise. Before explaining how that can be done, it is instructive to review the operation of a traditional charge pump. In a traditional charge pump (Fig. 10), the UP and DN pulses from the PFD drive switches connected in series with transistor current sources which convert the voltage pulses to current pulses of equal width. The down current pulse is subtracted from the up current pulse at the output node and the resulting signal drives the loop filter.

The proposed charge pump is shown in Fig. 11. Here, the voltage pulses are converted to current pulses by the resistors between the UP and DN inputs and the opamp inputs [8]. Instead of directly subtracting the current pulses before driving the loop filter, the difference information is contained in a differential signal which drives a differential loop filter. As desired, the charge pump current is now defined by a flicker-noise-free resistor rather than a transistor.

The opamp needed in the proposed charge pump does contribute flicker noise as modeled by the noise source $V_{n,\mathrm{op}}$ at the output of the opamp shown in Fig. 11. The control-voltage-to-output transfer function of the PLL is bandpass, however, so the opamp flicker noise contribution is significantly reduced.

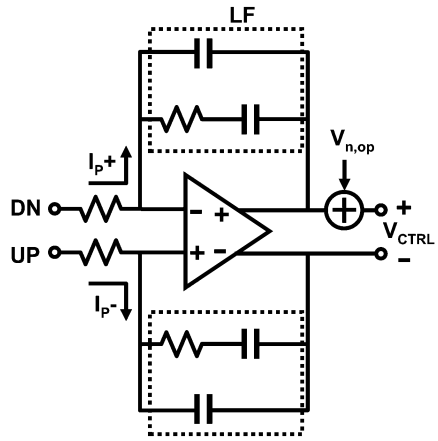

Fig. 11. Proposed charge pump.

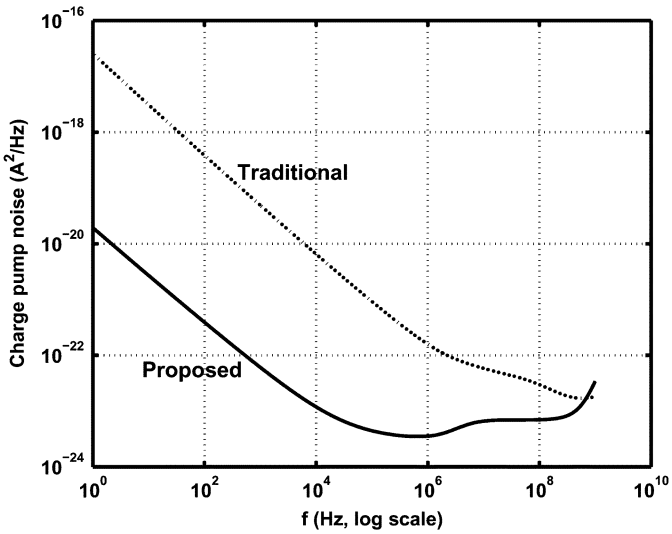

Fig. 12. Comparison of current noise spectra of traditional and proposed charge pumps.

The simulated charge pump current noise spectrum is plotted in Fig. 12. For the sake of comparison, the current noise spectrum of a traditional charge pump with equal pumping current is also shown. It is apparent that the flicker noise corner is reduced in the proposed design. These noise spectra were obtained from periodic noise simulations which take into account the fact that the traditional charge pump current noise is passed only during the fraction of the reference period when the PFD reset pulse is high.

IV. PFD and Divider

The PFD is a simple digital state machine. When driving a traditional charge pump, it is important that the reset pulses are wide enough to turn on the switches in the charge pump in order to avoid a dead zone. A wider reset pulse, however, exaggerates the ripple on the control voltage caused by mismatch between the UP and DN current sources. The proposed charge pump reduces this ripple in two ways. First, the mismatch is less because

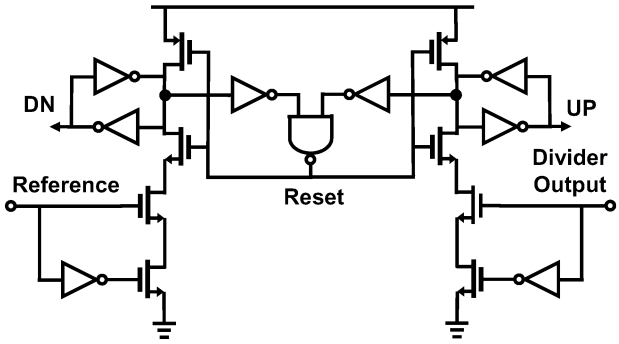

Fig. 13. Narrow reset pulse phase-frequency detector.

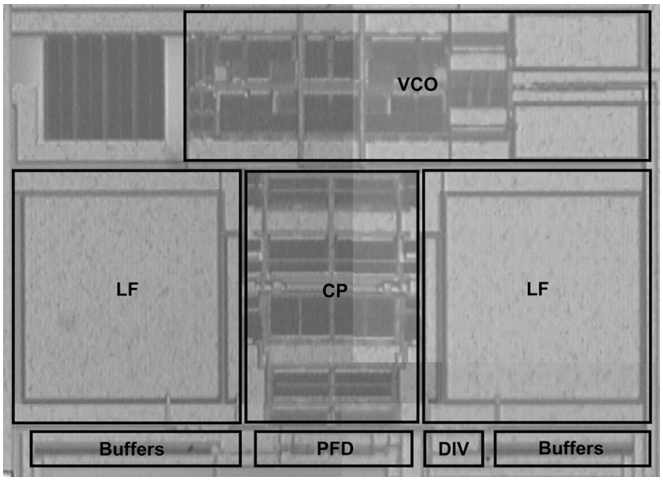

Fig. 14. Die photograph.

the two resistors have better matching than a pMOS current source has to an nMOS current source. Second, the reset pulse width can be minimized since there are no switches that must be turned on. The PFD described in [9] and shown in Fig. 13 was used in this work. This PFD was designed for high-speed operation where narrow reset pulses are required.

The divider is a cascade of divide-by-two stages. The first stage must operate at a relatively high frequency to cover the high end of the VCO tuning range. In order to meet the speed requirements, the divide-by-two stage was implemented using truly single phase clock (TSPC) flip-flops which are described in [10].

V. Measurement Results

The PLL was fabricated in a 0.18-μm CMOS technology and occupies 0.15 mm^2. Fig. 14 shows a die photograph. The measured jitter histogram[1] showing 2.36 ps rms jitter at an oscillation frequency of 2.4 GHz is depicted in Fig. 15. Shown in Fig. 16 is the measured jitter over the frequency range. As expected, the jitter increases linearly with the period, maintaining a constant fraction of the period.

In order to quantify the dynamic power supply noise sensitivity, the experiment depicted in Fig. 17 was performed where

[1]The histogram shows absolute jitter with respect to the PLL reference clock [11].

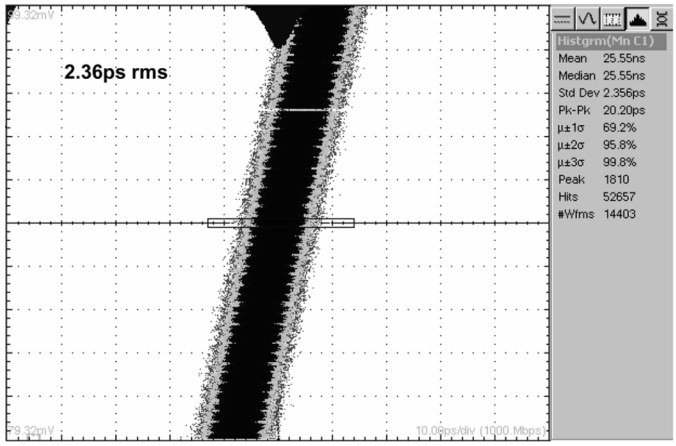

Fig. 15. Measured jitter histogram at 2.4 GHz.

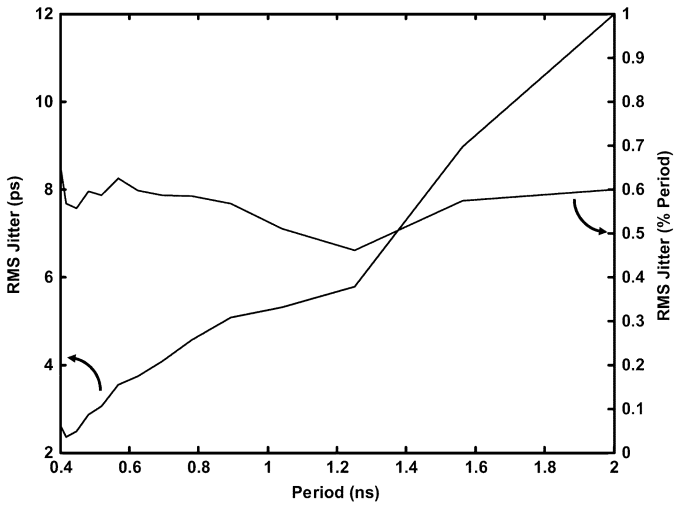

Fig. 16. Measured jitter as a function of oscillation period (left axis) and as a percentage of oscillation period (right axis).

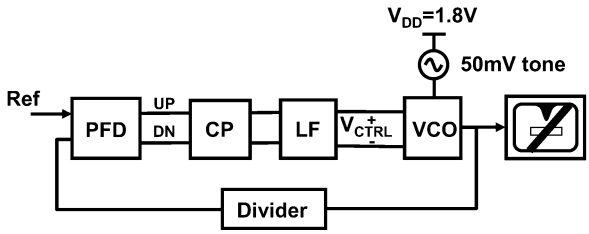

Fig. 17. Dynamic supply noise sensitivity measurement.

a 50-mV tone was added to the supply and the jitter degradation was measured. The amplitude of the tone was measured at the supply pin to accurately obtain the signal level entering the device under test. As described in the Appendix, the supply regulation loop will cause the supply sensitivity to be a low-pass shape. Fig. 18 shows the measured jitter for 1-MHz, 10-MHz, and 1-GHz supply tones, which demonstrates the ability of the loop to suppress high-frequency supply noise. For the 1-MHz case, the rms jitter is degraded to 14.8 ps. At 10 MHz, the rms jitter has reduced slightly to 9.92 ps, while at 1 GHz, the rms jitter is only 3.11 ps, which is very close to the jitter measured with a clean supply. The performance of the PLL is summarized in Table I.

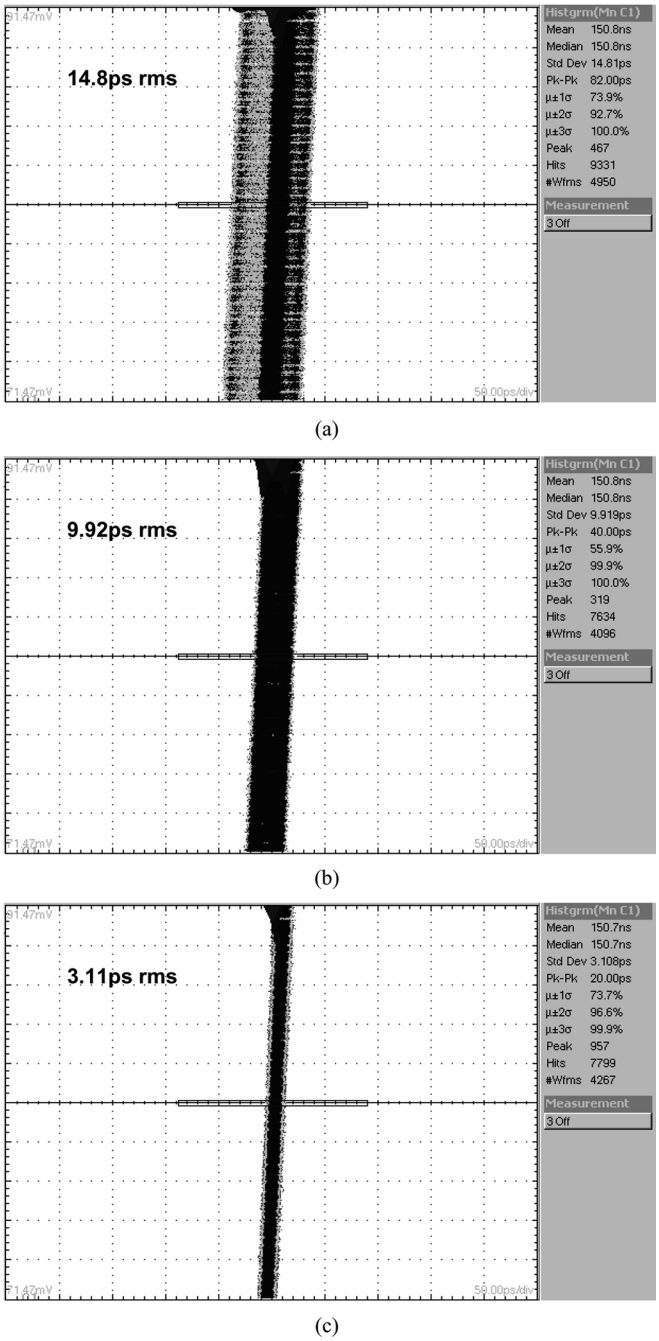

Fig. 18. Measured jitter histogram for (a) 1-MHz, (b) 10-MHz, and (c) 1-GHz supply tone.

The quadratic scaling expected by the analysis in Section II was verified by measuring the VCO power as a function of frequency. The measurement, shown in Fig. 19, does indeed show quadratic scaling.

VI. Conclusion

By addressing integration related issues, we have demonstrated a PLL well-suited for clock generation in modern digital integrated circuits. The wide range and small die area of the ring VCO used in the PLL enable the design to be reused for each of the many digital subsystems operating at different speeds that comprise a large digital system. The supply noise sensitive delay cells used in the ring VCO are tolerated in the presence of large digital switching noise through the use of fully differential supply regulated tuning. A wide bandwidth is employed to reduce the inherently large ring VCO jitter. Since the wide bandwidth exacerbates the charge pump flicker noise problem, a novel low flicker noise charge pump architecture was developed. With many instances of the PLL on the same die, power consumption is important. The design was shown to be power efficient over the entire frequency range.

TABLE I
Performance Summary

Technology	$0.18\mu m$ CMOS
Frequency Range	0.5 to 2.5GHz
Power Dissipation	25mW
Die Area	$0.15mm^2$
RMS Jitter	2.36ps
RMS Jitter with 50mV Supply Tone	14.8 ps (1MHz) 9.92ps (10MHz) 3.11ps (1GHz)

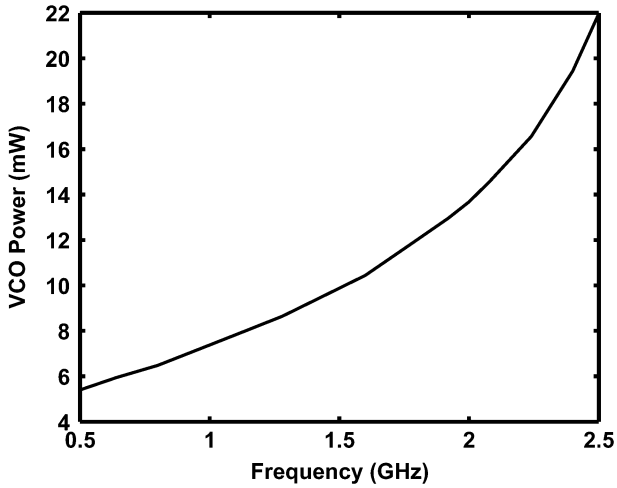

Fig. 19. Measured VCO power as a function of frequency showing quadratic scaling.

Appendix
Supply Regulated Tuning Design Process

Designing a supply regulated tuning loop requires careful balancing of several considerations. Referring to Fig. 20, which shows the single-ended case for the sake of simplicity, we can list the following considerations.

- Since the attenuation of supply noise is characterized by the transfer function $V_S/V_{\rm DD}(s)$, we want high DC attenuation, a low bandwidth for better high-frequency attenuation (since the transfer function is low-pass), and no peaking.
- Since the transfer function $V_S/V_C(s)$ is in the PLL signal path, it must have sufficiently high bandwidth so that it does not compromise the PLL loop stability.

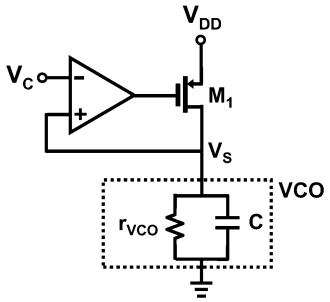

Fig. 20. Simplified supply regulated tuning for analysis.

- The supply regulation loop must also be stable, so care should be taken to ensure sufficient phase margin for the regulator loop transfer function $\mathrm{LG_{REG}}(s)$.
- Since the tuning range of the VCO is constrained by the swing at V_S, the dropout of the regulator should be low.
- The above considerations must be met with minimal power and die area overhead.

This Appendix is intended to yield insight into the process of designing a supply regulated tuning loop that successfully balances these considerations.

As derived in [12], the transfer function from the external supply V_{DD} to the internal supply V_S can be written as

$$\frac{V_S}{V_{\mathrm{DD}}}(s) = \frac{S_V\omega_o\omega_a(s/\omega_a+1)}{s^2+s(\omega_o+\omega_a)+(1+A)\omega_o\omega_a} \tag{2}$$

where r_{o1} is the output impedance of M_1, $S_V = r_{\mathrm{VCO}}/(r_{\mathrm{VCO}}+r_{o1})$, $A = A_oA_a$, $A_o = g_{m1}(r_{o1}\|r_{\mathrm{VCO}})$, which is the DC gain of the pMOS device, A_a is the DC gain of the amplifier, $w_o = [(r_{\mathrm{VCO}}\|r_{o1})C]^{-1}$ is the pole at V_S, and ω_a is the amplifier pole.

Rewriting (2) using control system notation, we get

$$\frac{V_S}{V_{\mathrm{DD}}}(s) = \frac{S_V\omega_o\omega_a(s/\omega_a+1)}{s^2+2\zeta\omega_n s+\omega_n^2}. \tag{3}$$

From (2) and (3),

$$\omega_n = \sqrt{(1+A)\omega_o\omega_a} \tag{4}$$

$$\zeta = \frac{\omega_o+\omega_a}{2\omega_n}. \tag{5}$$

Peaking occurs if the zero frequency is lower than the frequency where the transfer function rolls off due to the two poles. Therefore, care must be taken to ensure that ω_a is greater than ω_n.

To that end, we define a parameter $x > 1$ so that

$$\omega_a = x\omega_n. \tag{6}$$

From (4) and (6), we can write ω_a in terms of ω_o as

$$\omega_a = x^2(1+A)\omega_o \tag{7}$$

which shows that ω_o must be the dominant pole.

It can be shown that for $x < 2$, the two poles are complex. From (5) and (7), we see that

$$\zeta \approx x/2. \tag{8}$$

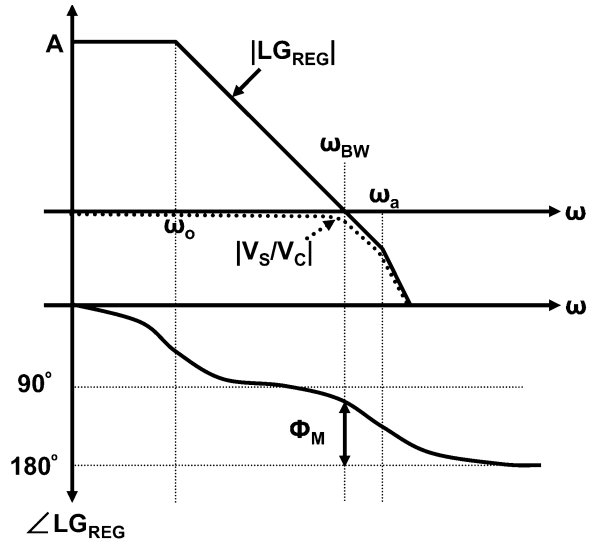

Fig. 21. Typical open- and closed-loop gain response.

In order to ensure that there is no peaking due to the complex poles, we will restrict $\zeta > 1/\sqrt{2}$, which means $x > \sqrt{2}$.

When $x > 2$, there are two real poles. As x increases, the poles split and the higher pole is approximately ω_a. Therefore, the higher pole and the zero cancel and the transfer function is single-pole-like. The bandwidth of the transfer function is set by the lower real pole, which decreases with x.

Behavioral PLL simulations reveal that the bandwidth of $V_S/V_C(s)$ must be about 5–10 times larger than the PLL bandwidth to ensure that the regulator does not compromise the stability of the PLL. $V_S/V_C(s)$ can be written in terms of the regulator loop gain $\mathrm{LG_{REG}}(s)$

$$\frac{V_S}{V_C}(s) = \frac{\mathrm{LG_{REG}}(s)}{1+\mathrm{LG_{REG}}(s)} \tag{9}$$

where

$$\mathrm{LG_{REG}}(s) = \frac{A}{(s/\omega_o+1)(s/\omega_a+1)}. \tag{10}$$

Fig. 21 shows a plot of $|\mathrm{LG_{REG}}|$ and $|V_S/V_C|$. Since the feedback factor in this case is 1, the bandwidth of $|V_S/V_C|$, ω_{BW}, is simply the unity-gain bandwidth of $\mathrm{LG_{REG}}(s)$, so

$$\omega_{\mathrm{BW}} \approx A\omega_o. \tag{11}$$

From (7) and (11), we see that

$$\omega_a \approx x^2\omega_{\mathrm{BW}}. \tag{12}$$

Also shown in Fig. 21 is the loop-gain phase response $\angle\mathrm{LG_{REG}}(s)$ for phase margin calculation. The phase margin can be written as

$$\Phi_M = 180^\circ - \arctan(\omega_{\mathrm{BW}}/\omega_o) - \arctan(\omega_{\mathrm{BW}}/\omega_a). \tag{13}$$

Assuming a large gain A, the second term is approximately -90° and substituting (12) into the third term simplifies (13) to

$$\Phi_M \approx 90^\circ - \arctan(1/x^2). \tag{14}$$

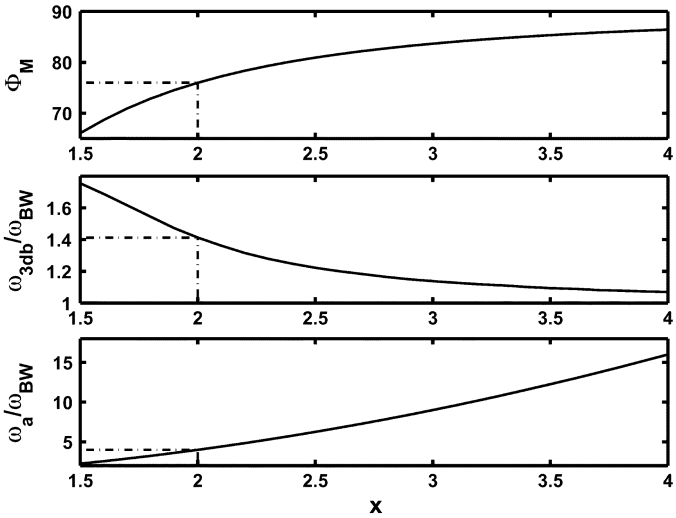

Fig. 22. Φ_M, $\omega_{3\mathrm{dB}}$, and ω_a as a function of x.

From (2), the DC gain of $|V_S/V_{\mathrm{DD}}|$ is $S_{\mathrm{VDD}}/(1+A)$. Therefore, to increase the DC supply noise attenuation, we want a large r_{o1} and a large DC gain A. Rearranging (11), we get

$$\omega_o \approx \omega_{\mathrm{BW}}/A \tag{15}$$

which shows that increasing A decreases ω_o, which increases the size of the capacitor C. Thus, there exists an optimum choice of A that balances DC supply noise attenuation with capacitor area. Notice from (15) that the choice of a wide PLL bandwidth, and thus a large ω_{BW}, eases this tradeoff somewhat.

Having chosen a value for A, the only remaining decision is the value of parameter x, from which we can derive Φ_M, ω_a, and the -3-dB bandwidth of $V_S/V_C(s)$, $\omega_{3\mathrm{dB}}$, which determines how much high-frequency supply noise is filtered by the regulation loop. Shown in Fig. 22 is a plot of these three parameters as a function of x.

In order to choose x properly, we must consider the value of x that is optimum for each parameter individually. The phase margin approaches its maximum value of 90° as x increases. A large value of x is also desired to yield a small $\omega_{3\mathrm{dB}}$ which is desired to filter supply noise. On the other hand, for low dropout the pMOS device M_1 must have a small overdrive voltage which mandates a large aspect ratio. We have also seen that this device should be long to maximize r_{o1} for DC supply noise attenuation. Having a large M_1 decreases ω_a because of the large M_1 gate capacitance. Therefore, a small x is desired to enable a small ω_a.

The dashed lines in Fig. 22 show a reasonable compromise of $x = 2$ which leads to $\Phi_M = 76°$, $\omega_{3\mathrm{dB}} = \sqrt{2}\omega_{\mathrm{BW}}$, and $\omega_a = 4\omega_{\mathrm{BW}}$.

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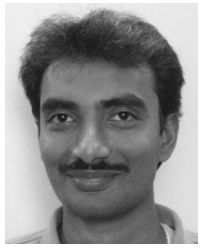

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