Design of a Low-Distortion 22-kHz Fifth-Order Bessel Filter

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***Abstract*—A linearity improvement technique employing passive resistors and current-steering MOS transistors as a variable resistance element is proposed to implement a low-distortion filter in CMOS technology. This proposed implementation relies on the linearity of the passive resistors and the tunability of the current-steering MOS transistors operating in the triode region to overcome the limited linearity performance in continuous-time electronically tunable filters. By using the existing systematic feedback loops in the active filters and placing the nonlinear elements inside the feedback, the distortion resulting from the nonlinear devices is greatly reduced by the filter loop gain. A 22-kHz fifthth-order Bessel filter, its dynamic range optimized by applying Karmarkar's rescaling algorithm and self-tuned with a switched-capacitor reference resistor, demonstrates better than −90-dB THD with a 2-kHz, 4-V_{pp} signal in 5-V 2-μm CMOS.**

I. Introduction

NUMEROUS continuous-time IC filter design techniques have been reported with a common effort to achieve high linearity while trying to maintain tunability [1]–[5]. Despite the enhancements of these techniques, one underlying problem for all cases is their limited linearity performance. Recently, a straightforward digital trimming method has demonstrated a high linearity performance by trimming weighted capacitors in parallel [6]. This kind of switching occurring in the signal paths, however, prohibits having the signal present while the digital tuning is being performed.

Among the various implementations of electronically tunable filters, MOSFET-C filters are easily implemented with operational amplifier blocks while maintaining the identical structure of an active RC filter [5], [7]. These MOSFET-C filters, fabricated in a standard CMOS process, utilize the linearized model behavior of a MOS transistor operating in the triode region in place of a passive resistor. Such devices as these have been proposed as linear tunable resistor elements in monolithic integrated circuits [5], [7]–[11]. However, due to mismatches and the inherent nonlinear behavior of MOSFET's in triode, THD of only about 40–60 dB can be achieved with a volt-level signal swing in a single 5-V system. With an ongoing interest in building highly linear tunable continuous-time filters, and given that switched-capacitor filters have demonstrated good linearity performance [12], [13], a linearity improvement technique for low-distortion tunable CMOS filters is investigated.

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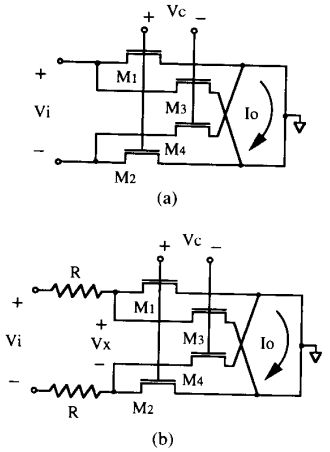


Fig. 1. (a) Conventional balanced variable resistor and (b) improved R-MOSFET resistor.

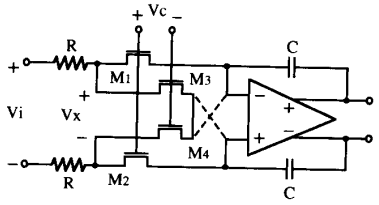


Fig. 2. Improved R-MOSFET-C integrator.

In comparison with conventional tunable filters, the proposed linearity improvement herein moves the nonlinear variable resistance inside a feedback loop for a large improvement of distortion. Furthermore, the actual voltage applied to the nonlinear elements is scaled down to operate more closely within their linear range. Allowing a simplified signal summing for multiple inputs and high linearity performance, this proposed technique leads to a practical design of low-distortion tunable filters in CMOS.

The following sections will include discussions of the proposed variable resistor referred to as the R-MOSFET (Section II), the low-distortion integrator implementation referred to as the R-MOSFET-C (Section III), the use of the feedback loop for linearity improvement (Section IV), automatic tuning implementation using a switched-capacitor reference resistor (Section V), design of a fifth-order Bessel filter with dynamic range optimization (Section VI), experimental results of the prototype fifth-order Bessel filter (Section VII), and the conclusions.

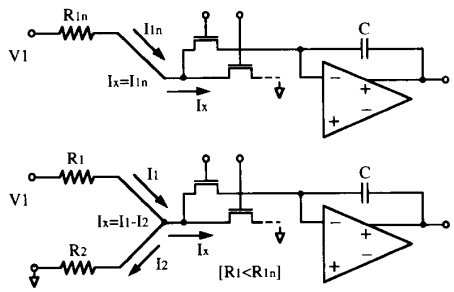


Fig. 3. Dual-input loading effect.

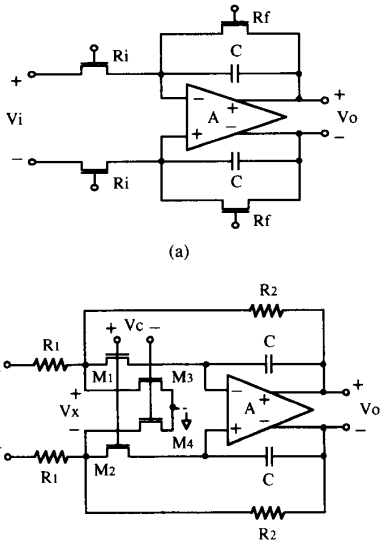


Fig. 4. (a) MOSFTET-C first-order filter and (b) R-MOSFET-C first-order filter.

II. Proposed R-MOSFET Variable Resistor

A differentially balanced variable resistor made of four identical MOS transistors M_1, M_2, M_3, and M_4 biased in triode is shown in Fig. 1(a). This variable resistor is known to behave purely linearly under ideal conditions such as perfectly matched devices, bias independent mobility, and perfectly balanced input signals [8]–[11]. Despite the fact that these ideal conditions can never be fully satisfied (thus the limited linearity in the 60-dB range) the key advantage of this topology is its current-steering capability for tuning. The current-steering variable resistor of Fig. 1(a) has an equivalent resistance (used as a part of an active integrator) given by

$$R_{\text{eq}} = \frac{1}{G_{1,2} - G_{3,4}} = \frac{1}{KV_C} \tag{1}$$

where G_i is the triode region channel conductance of M_i defined by

$$G_i = K(V_{\text{GS}i} - V_{\text{th}i}), \text{ and } K = \mu C_{\text{OX}} \frac{W}{L}. \tag{2}$$

(1) implies that the equivalent conductance is linearly controlled by the control voltage V_C.

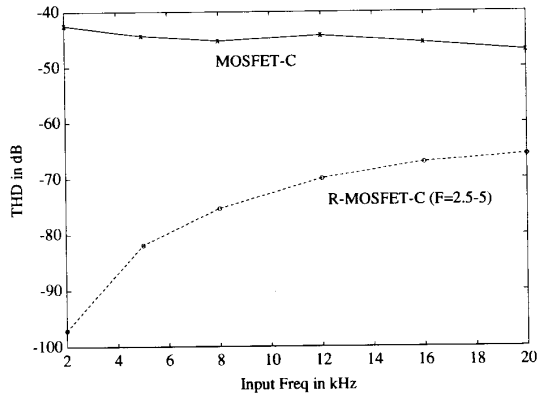


Fig. 5. Simulated THD: MOSFET-C filter versus proposed R-MOSFET-C filter.

An improved version of this, proposed as an R-MOSFET stage, is shown in Fig. 1(b), where four transistors are degenerated by passive resistors. Just as in Fig. 1(a), the resistance (inherently conductance) of the current steering portion (MOSFET's) is set by any control voltage V_C. The improved R-MOSFET stage shown in Fig. 1(b) has an equivalent resistance of

$$R_{\text{eq}} = \frac{F}{G_{1,2} - G_{3,4}} = \frac{F}{KV_C} \tag{3}$$

where the voltage scale factor F is defined by

$$F = \frac{V_i}{V_{\text{x}}} = 1 + 2\overline{G}R \tag{4}$$

and the average conductance of M_1, M_2, M_3, and M_4 is

$$\overline{G} = \frac{(G_{1,2} + G_{3,4})}{2}. \tag{5}$$

This yields an appropriate design value for F because the quantity $2\overline{G} = (G_{1,2} + G_{3,4})$ represents the equivalent conductance of the MOSFET's in parallel combination that is seen at V_{x}. As a result of the voltage scaling given by (4), the distortion improves as the signal swing across the MOSFET's decreases. This effect is identical in concept to the local feedback of an emitter degeneration in BJT. Unlike the conventional balanced resistor, which relies on transistor matching for high linearity, given the unavoidable level of imperfect balance and device mismatches, the R-MOSFET stage systematically improves linearity in proportion to the amount of voltage scaling. The MOSFET devices in this arrangement can be viewed as current-steering devices, operating in the triode region, rather than as "resistors."

III. Low-Distortion Integrator

A. R-MOSFET-C Integrator

The combined circuit block of the R-MOSFET stage of Fig. 1(b) in conjunction with an op amp with feedback capacitors is a low-distortion R-MOSFET-C integrator, as shown in Fig. 2. The solid and dotted lines in the figure represent two different versions of the R-MOSFET-C implementation. The

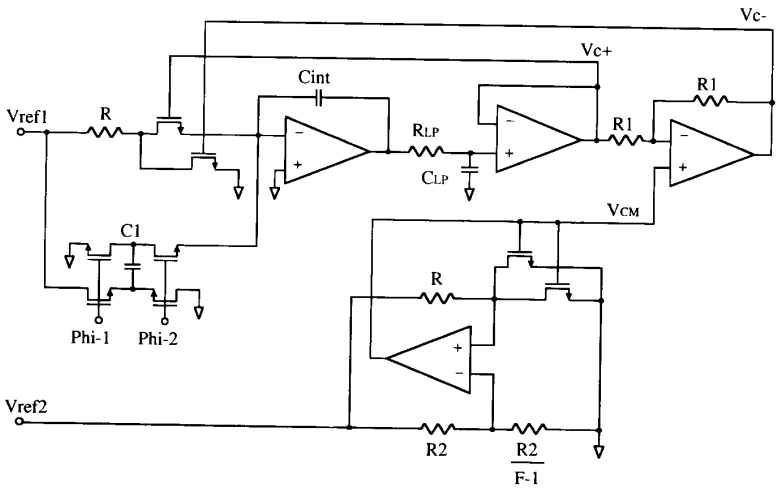


Fig. 6. Frequency tuning circuitry.

criss-cross configuration (dotted lines) contains the identical variable resistor of Fig. 1(b) and behaves just as described in (3)–(5). In addition, the integrator displays a linearly controlled unity-gain frequency

$$\omega_{\text{unity}} = \frac{G_{1,2} - G_{3,4}}{FC} = \frac{KV_C}{FC}. \tag{6}$$

Although the criss-cross integrator of Fig. 2 has a desirable symmetry in generating a more linear input resistance, it reduces the effective dc gain and bandwidth of the integrator and enhances the unity-gain frequency sensitivity to component mismatches. Other than the overall filter's performance error due to the lower effective gain and bandwidth [14], [15], and the increased sensitivity [11], another practical limit is an increase in noise due to the low-resistance paths between the summing nodes of the operational amplifier. That is, the current noise of the low-resistance paths degrades the dynamic range of the filter. As a result, a slight modification of this topology is made to improve the noise performance, as shown by the solid line in Fig. 2. In this *current-dumping* configuration, the bypassing current from the input is not fed to the opposite side but instead dumped to the ground (conceptually in a single-ended configuration). The advantage of this arrangement is approximately a factor of four increase in the resistance between the summing nodes of the operational amplifier. This improvement comes at the cost of a slight sacrifice in the balance of the electrical symmetry at the variable resistance cell. In reality the symmetry is not as critical in the linearity-improved filter implementation because the MOSFET's are merely being used as a current-steering element with a small voltage swing across it. Due to this modification, (3) and (6) are also modified as follows for the current-dumping integrator:

$$R_{\text{eq}} = \frac{F}{G_{1,2}} = \frac{F}{K\hat{V}_C} \text{and} \tag{7}$$

$$\omega_{\text{unity}} = \frac{G_{1,2}}{FC} = \frac{K\hat{V}_C}{FC}, \tag{8}$$

TABLE I
ADJUSTMENT OF FILTER COEFFICIENTS

L-C	R-C	NS	Optimized	R-MOSFET-C
L1=0.1743	C1=15.5 pF	15.6 pF	43.1 pF	43.1 pF
C2=0.5072	C2=45.0 pF	48.4 pF	62.3 pF	62.3 pF
L3=0.8040	C3=71.4 pF	76.0 pF	75.8 pF	75.8 pF
C4=1.1110	C4=98.6 pF	86.6 pF	72.4 pF	72.4 pF
L5=2.2582	C5=200 pF	100 pF	73.2 pF	73.2 pF
R=1.000	R=81.5 kΩ	R1=81.5 kΩ	29.5 kΩ	12.6 kΩ
		R2=80.9 kΩ	29.3 kΩ	12.5 kΩ
		R3=80.9 kΩ	62.9 kΩ	22.1 kΩ
		R4=75.8 kΩ	76.0 kΩ	30.0 kΩ
		R5=76.5 kΩ	91.5 kΩ	37.7 kΩ
		R6=92.8 kΩ	127 kΩ	87.1 kΩ
		R7=163 kΩ	223 kΩ	153 kΩ
		R8=75.8 kΩ	27.4 kΩ	11.7 kΩ
		R9=76.5 kΩ	59.5 kΩ	20.9 kΩ
		R10=92.8 kΩ	93.1 kΩ	36.7 kΩ
		R11=163 kΩ	195 kΩ	80.4 kΩ

where

$$\hat{V}_C = \frac{V_C}{2} + (V_{CM} - V_{th}) \text{and}$$

V_{CM} = common-mode control voltage.

B. Voltage Scale Factor F versus Noise and Distortion

Studying the independent noise sources in detail in the current-dumping configuration of Fig. 2 (solid line), the resistors, MOSFET's, and operational amplifier, the equivalent input referred noise of the current-dumping integrator at low frequencies is given by

$$\frac{\overline{V_{\text{eq}}^2}}{\Delta f} = 4kT\left\{2R + \left(\frac{R}{R_{3,4}}\right)^2 2R_{3,4} + \left(\frac{R+R_{3,4}}{R_{3,4}}\right)^2 (2R_{1,2} + R_i)\right\} \tag{9}$$

where R_i is an equivalent input noise resistance of the

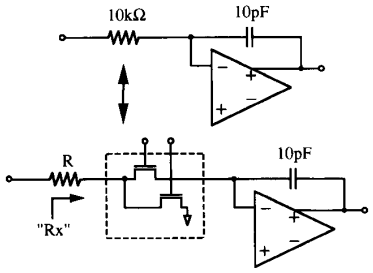


Fig. 7. Active R-C to R-MOSFET-C transformation.

op amp. (Also note the implied notations $R_{1,2} = 1/G_{1,2}$ and $R_{3,4} = 1/G_{3,4}$.) It can be shown from the given expression that the noise increases as F increases (R increases with respect to $R_X = R_{1,2}||R_{3,4}$) and V_C decreases ($R_{3,4}$ decreases with respect to $R_{1,2}$). Since the linearity improves with increasing voltage scale factor F a linearity versus noise trade-off is necessary in the design when choosing an optimum value for F.

Another way of scaling the input voltage swing has been suggested in [7], where the input is predivided by a factor (3 in their setup) and the output is postmultiplied by the same factor to reduce distortion. This kind of input scaling directly trades off THD with S/N. For example, effective voltage scaling of $F = 5$ would cost 14-dB noise while making approximately the same amount of linearity improvement. For the prototype filter implemented using a set of varied voltage scaling factors (discussed in Section VI–C), $F = 2.5$-5, the noise increase due to this technique is about 2.3 dB in simulation. This result comes from the worst-case condition for a tuning range of ±50%. Considering even a greater reduction of distortion by feedback (discussed in Section IV), this relatively higher noise floor can be offset by the larger undistorted signal this technique provides.

C. Multiple-Input Integrator

In the case of a multiple-input implementation the inputs are arranged with multiple resistors but with only one current-steering quad (four MOSFET devices operating in the triode region) per integrator. However, an appropriate loading effect of the multiple inputs should be taken into account when the resistor values are chosen. As shown in Fig. 3 for a dual-input setting, because of the extra loading of the second input a fraction of the input current is subtracted before the current flows through the MOSFET's. Thus the loading effect calls for a reduced input passive resistor R_1 from the original value R_{1n}. The loading effect of a dual-input stage yields that the actual resistances, R_1 and R_2, are related to the nominal values of R_{1n} and R_{2n} by

$$R_1 = R_{1n}\frac{1 - S_1S_2}{1 + S_2} \text{ and } R_2 = R_{2n}\frac{1 - S_1S_2}{1 + S_1}, \tag{10}$$

where the constants are

$$S_1 = \frac{1}{2\overline{G}R_{1n}} \text{ and } S_2 = \frac{1}{2\overline{G}R_{2n}}.$$

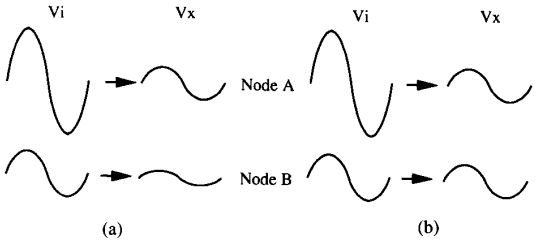


Fig. 8. Constant-ratio versus constant-voltage scaling.

Similarly for a triple-input stage, the actual resistance R_1, R_2, and R_3 are

$$\begin{aligned} R_1 &= R_{1n}\frac{1 - S_1S_2 - S_1S_3 - S_2S_3 - 2S_1S_2S_3}{1 + S_2 + S_3 + S_2S_3}, \\ R_2 &= R_{2n}\frac{1 - S_1S_2 - S_1S_3 - S_2S_3 - 2S_1S_2S_3}{1 + S_1 + S_3 + S_1S_3}, \text{ and} \\ R_3 &= R_{3n}\frac{1 - S_1S_2 - S_1S_3 - S_2S_3 - 2S_1S_2S_3}{1 + S_1 + S_2 + S_1S_2}, \end{aligned} \tag{11}$$

where the constants are

$$S_1 = \frac{1}{2\overline{G}R_{1n}}, S_2 = \frac{1}{2\overline{G}R_{2n}}, \text{ and } S_3 = \frac{1}{2\overline{G}R_{3n}}.$$

IV. Reducing Distortion by Feedback

In the preceding discussions, a linearity improvement technique was shown to reduce distortion due to the scaling of the input signal swing by F. In an active filter configuration, however, the second input (and third input exists in some cases) to the integrator forms a feedback loop. Shown in Fig. 4(b) is the linearity improved version (R-MOSFET-C) of the first-order filter in contrast to the first-order filter using nonlinear MOSFET resistors (MOSFET-C) as shown in Fig. 4(a). The proposed topology shown in Fig. 4(b) has a better THD over the conventional topology of Fig. 4(a) because the MOSFET's are operating with a reduced V_{DS}. Furthermore, distortion is improved by a greater factor because the nonlinear components (current-steering MOSFET's) are now inside a feedback loop.

To observe the change in the feedback loop configuration for this low-distortion filter, as an exemplary comparison, we can observe first the transfer function of the first-order MOSFET-C filter example as shown in Fig. 4(a). Observing the single-ended case for simplification of analysis, some algebra yields the closed-loop transfer function

$$-\frac{V_o}{V_i} = \frac{Z_f}{R_i}\frac{A(\frac{R_i}{R_i+Z_f})}{1 + A(\frac{R_i}{R_i+Z_f})}; \text{ where } Z_f = R_f||C. \tag{12}$$

This can also be expressed as

$$\begin{aligned} -\frac{V_o}{V_i} &= \frac{R_f}{R_i}\frac{A\{\frac{R_i||C(1+A)}{R_i||C(1+A)+R_f}\}}{1 + A\{\frac{R_i||C(1+A)}{R_i||C(1+A)+R_f}\}} \\ &= \frac{R_f}{R_i}\frac{A\{\frac{R_i}{R_i+R_f+sCR_iR_f(1+A)}\}}{1 + A\{\frac{R_i}{R_i+R_f+sCR_iR_f(1+A)}\}}. \end{aligned} \tag{13}$$

It can be observed from the transfer function that the right half of the expression, in the format of $X/(1 + X)$, is

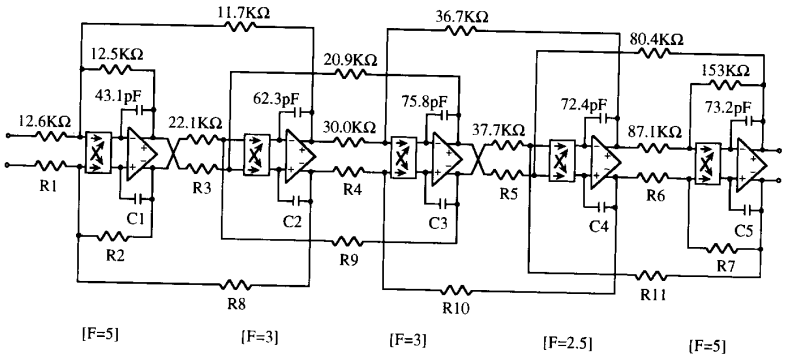


Fig. 9. Fifth-order Bessel filter after dynamic range optimization and constant-voltage scaling.

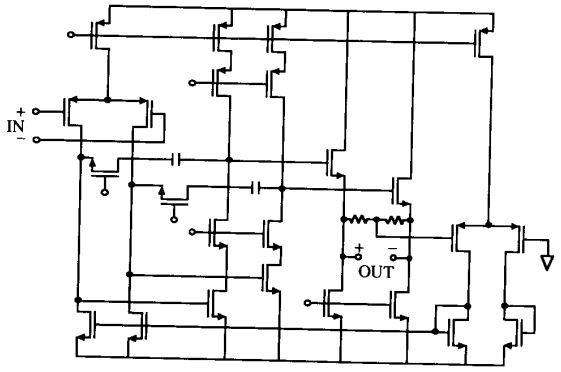


Fig. 10. Two-stage balanced op amp.

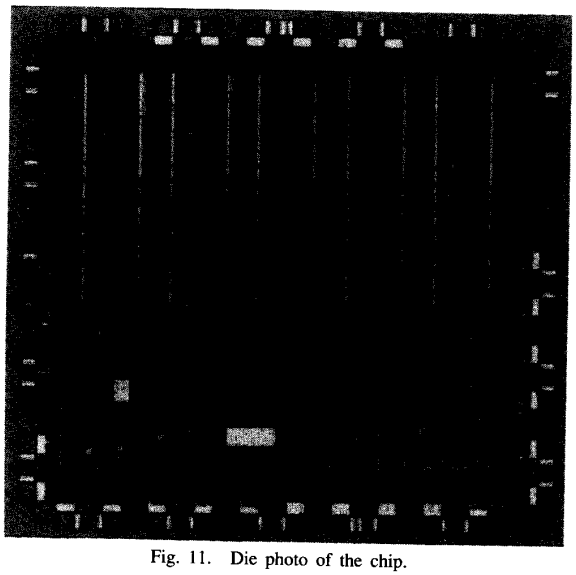


Fig. 11. Die photo of the chip.

highly linear inside the bandwidth of the filter because of the linearity improvement by the feedback loop gain. Thus the distortion in this MOSFET-C filter is dominated by the ratio R_f/R_i, which can never be sufficiently linear. Even though a fully differential architecture can cancel much of the even harmonics, the mismatch of transistors limits the linearity performance. Limited linearity achieved by this kind of configuration can vary over the input frequency and has been discussed for a biquad example in [16].

Now observe the feedback loop configuration used in the proposed linearity improvement technique as shown in Fig. 4(b). The loop gain is $\overline{A}f$ if the transfer function of the MOSFET-C integrator inside the loop is $\overline{A} \approx G_{1,2}/sC$ (with the same dc gain of the op amp), and the transfer function (for single ended) is

$$-\frac{V_o}{V_i} = \frac{R_2}{R_1}\frac{\overline{A}\left(\frac{R_1||Z_X}{R_1||Z_X+R_2}\right)}{1+\overline{A}\left(\frac{R_1||Z_X}{R_1||Z_X+R_2}\right)}, \text{ where}$$

$$Z_X = \frac{1}{G_{3,4}}||\left\{\frac{1}{G_{1,2}} + \frac{1}{sC(1+A)}\right\}. \quad (14)$$

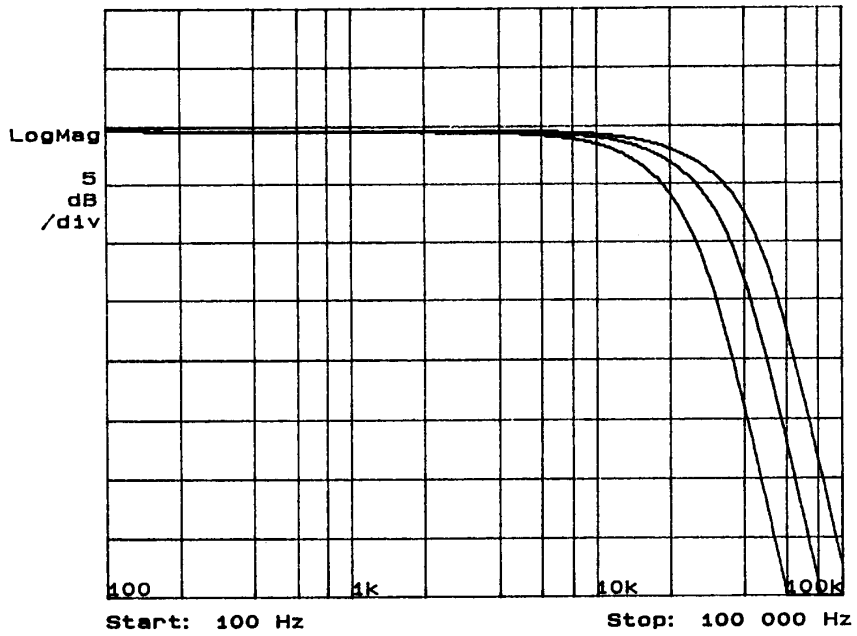
Note that

$$f = \frac{R_1||Z_X}{R_1||Z_X+R_2} \approx \frac{R_1||R_X}{R_1||R_X+R_2}, \text{ where}$$

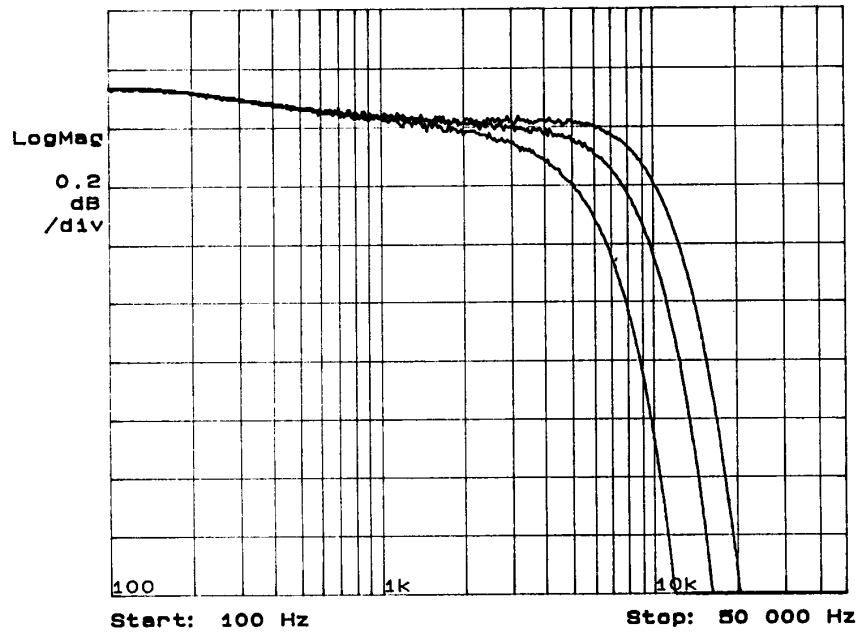
$$R_X = \frac{1}{G_{3,4}+G_{1,2}} = \frac{1}{2\overline{G}}, \quad (15)$$

and also for the condition where $R_1 = R_2$, $f \approx 1/F$. It is clear from the transfer function that the ratio R_2/R_1 is perfectly linear, fully depending upon the linearity of passive resistors, and the right half of the expression is in the format $T/(1+T)$. This means that all nonlinear functions are inside of the feedback loop where the loop gain, $T = \overline{A}(R_1||Z_X)/(R_1||Z_X+R_2)$, reduces distortion within the bandwidth of the filter. The reduction of distortion approaches a minimum as the input frequency approaches the corner frequency of the filter where the magnitude of the loop gain T becomes unity.

This effect of feedback on filter linearity is easily understood in the simulation result of a fifth-order Bessel filter, as shown in Fig. 5. (The prototype R-MOSFET-C filter has varied voltage scale factor, $F = 2.5 - 5$, as discussed in Section VI–C.) A similar filter with the same level of MOSFET mismatches, an implementation using the conventional MOSFET-C integrator of Fig. 4(a), exhibits a constant THD independent of the frequencies in the passband, while the improved implementation using the proposed R-MOSFET-C integrator of Fig. 4(b) exhibits a much lower THD, particularly



(a)



(b)

Fig. 12. (a) Measured frequency responses with tuning and (b) passband flatness.

at lower frequencies due to the effect of the feedback loop gain. At the passband edge, as loop gain decreases this improvement disappears, but the voltage scaling still maintains THD lower than the conventional filter by the factor of F.

V. Automatic Tuning by Switched Capacitor

The automatic tuning proposed herein takes advantage of switched-capacitor network accuracy to implement a reference time constant [17], which depends solely on capacitor matching. This switched-capacitor tuning method is no different from the conventional indirect tuning method in that it tunes the filter in the master–slave configuration; an equally satisfactory component matching is required for an equivalent accuracy of tuning. But replacing the core of the complex tuning circuitry by a mere RC time-constant matching circuit greatly simplifies the task.

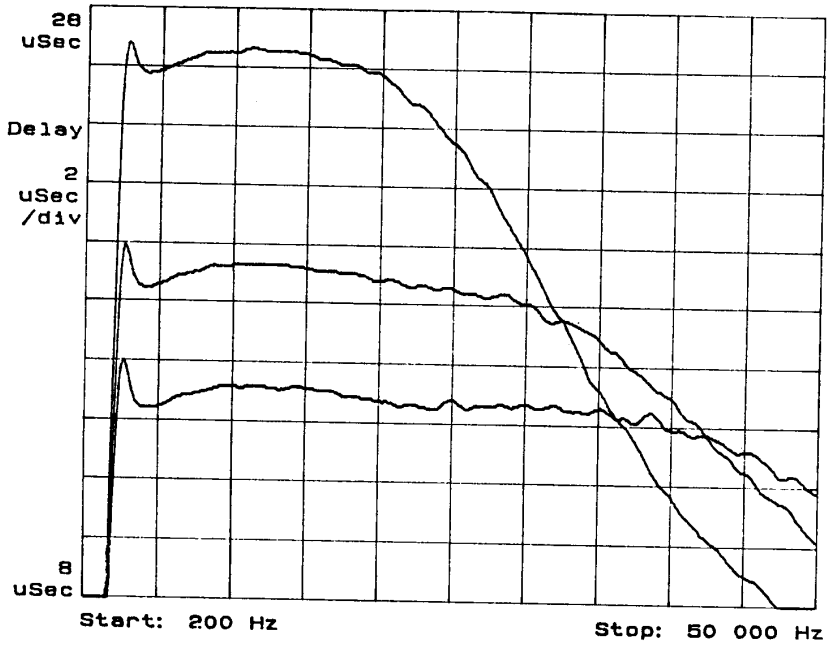


Fig. 13. Measured group delays with linear frequency.

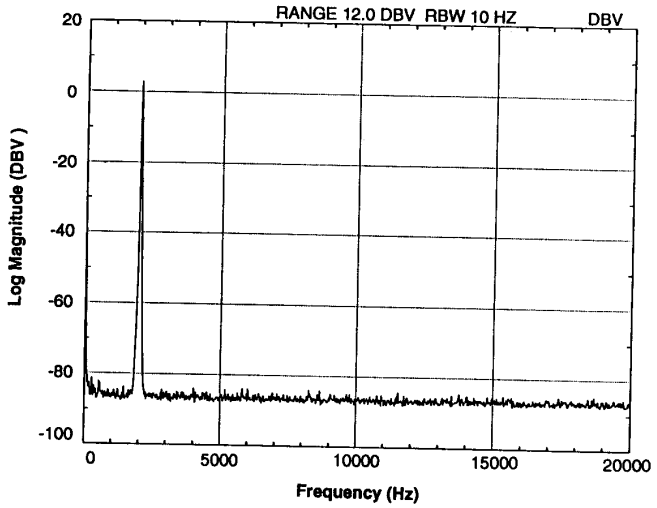


Fig. 14. Measured output spectrum (2-kHz tone).

Shown in Fig. 6 is the overall schematic of the tuning circuitry. Shown in the upper left portion of the schematic is the time-constant matching integrator of the linearity-improved continuous-time path and the switched-capacitor path. The time constant of the continuous-time path is $R_{\rm eq}C_{\rm int}$, and that of the switched-capacitor path is $C_{\rm int}/(f_{\rm clk}C_1)$. The mismatch of the two time constants, which simplifies as the mismatch of $R_{\rm eq}$ and $1/(f_{\rm clk}C_1)$, is reflected at the output of the integrator. That voltage is then translated to the control voltage of the current-steering MOSFET's. Equilibrium is reached when $R_{\rm eq} = 1/(f_{\rm clk}C_1)$. The lower portion of the schematic is the tuning circuitry for the common-mode control voltage. This common-mode control voltage, $V_{\rm CM}$, maintains the designed voltage scale factor F, and actual time constant matching is accomplished by varying the differential control voltage $V_C = V_{C+} - V_{C-}$. Placing a dominant pole in the control loop by choosing the product $R_{\rm LP}C_{\rm LP}$ very large (alternately a large $C_{\rm int}$ can be used), a stable control is established. Among the fabricated filters, the passband f_{-3dB} standard deviation (in percent of the nominal f_{-3dB}) is 5%, measured under a fixed capacitance, C_1, and the same reference frequency, $f_{\rm clk}$. If a greater accuracy of the corner frequency is desired, a

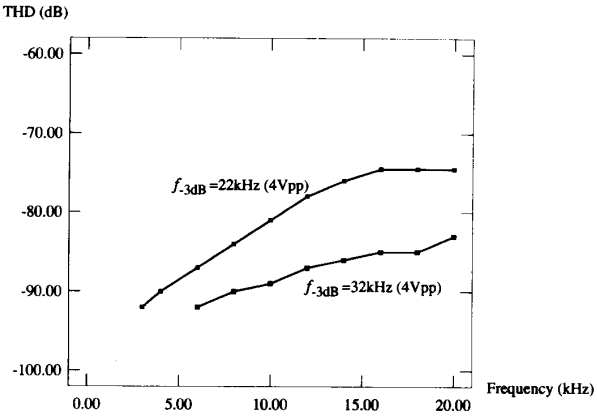


Fig. 15. Measured THD versus frequency.

TABLE II
SUMMARY OF MEASURED PERFORMANCE

Technology	2μ double poly CMOS
Filter Type	Fifth-order Bessel
Cutoff Frequency	22 kHz
Tunable Range	2 kHz–35 kHz
Passband f_{-3dB} (std. dev.)	5%
Passband Deviation	0.1 dB
Group delay	19 $\pm$0.5 μs
Control Voltage Feedthrough	10 μV_{rms}
THD (4-V_{pp}, 2-kHz input)	-90 dB
SNR	83 dB
CMRR/PSRR+/PSRR	58 dB/58 dB/47 dB
Power Supply	5 V
Power Consumption	40 mW
Active Die Area	7 mm^2

fine adjustment can be provided by means of either digitally trimming the capacitor C_1 or varying the clock frequency f_{clk}. Having placed a set of binary-weighted capacitors in place of C_1 for digital tuning, the fine tuning for the desired corner frequency of the prototype filter can be accomplished within a $\pm 1\%$ absolute accuracy.

VI. Fifth-Order Bessel Filter Design

A. Dynamic Range Optimization

In addition to many techniques used for improving the dynamic range of an active filter as in [18], the dynamic range can further be improved after node-voltage scaling by an optimization method that uses chip area as the constraint condition. Simply increasing all capacitances and reducing all resistances by the same proportion in an active filter will maintain the identical frequency response and improves the dynamic range by an equal proportion, but there is no true net gain in this kind of dynamic range improvement because the chip area taken up by the capacitors is commonly quite dominant, especially in low-frequency filters. Thus a better focus is to maximize the dynamic range per total chip area (approximately the total capacitance). This approximation results from neglecting the silicon area taken up by the resistors in comparison to the area taken up by the capacitors. This optimization problem naturally leads to a linear programming.

Table I shows the progression of changes in the filter coefficients starting from the basic L-C ladder. The fifth-order Bessel filter coefficients in the third column, NS, have been obtained from the L-C ladder to active R-C filter transformation and node-voltage scaling [19], [20]. In order to maintain the frequency response of the filter, each time constant for all integrating signal paths needs to be fixed. A total of eleven time constants exist. The time constants are $\tau_1 = R_1C_k$, $\tau_2 = R_2C_k$, $\tau_3 = R_3C_k$, up to $\tau_{11} = R_{11}C_k$, where C_k is one of the five capacitors connected to the given resistor at a summing node. As each equivalent noise voltage source in series with a resistor sees a different gain to the output of the filter, the total noise power of the filter at the output is proportional to a cost function defined by

$$\text{Cost} = \sum_{i=1}^{11} R_i {A_i}^2, \tag{16}$$

where A_i is the gain from R_i to the output. The constraint condition on the other hand is

$$C_{\text{total}} = C_1 + C_2 + C_3 + C_4 + C_5, \tag{17}$$

where C_{total} is a constant (i.e., fixed area). Each C_k can also be replaced by terms in R_i and fixed time constant τ_i. Linearizing the constraint equation by a first-order Taylor's approximation at each step of the iteration and applying Karmarkar's rescaling algorithm [21], the fifth-order Bessel filter of the optimum dynamic range is calculated as shown in the fourth column of Table I. Note the changes in the sizes of resistors and capacitors (and total capacitance unchanged), yet this filter displays exactly the same frequency response as the previous filter in the third column. The optimized filter yields a dynamic range improvement of about 0.7 dB. Even though the improvement is not very large, it partly compensates for the incremental reduction of the dynamic range resulting from the linearity improvement technique at no other costs. A more rigorous linear programming approach can also be implemented by considering the area taken up by the resistors and the influence of the voltage scaling F by including the information in the constraint and cost functions.

B. Active R-C to R-MOSFET-C Transformation

As discussed in Section II with a particular focus on the R-MOSFET portion, each of the resistors in an active R-C filter needs to be changed to a variable resistor R-MOSFET, resulting in a highly linear R-MOSFET-C implementation. In the example shown in Fig. 7, the R-MOSFET combination $R+R_X$ represents a sum that is equal to the original single resistor 10 kΩ, and the capacitor value 10 pF stays unchanged. Because the parallel combination of the two MOSFET's in triode, R_X, is independent of the differential control voltage V_C, the voltage scale factor $F = (R + R_X)/(R_X)$ is maintained at any V_C, and this differential control voltage tunes the variable resistance. Once this active R-C to R-MOSFET-C

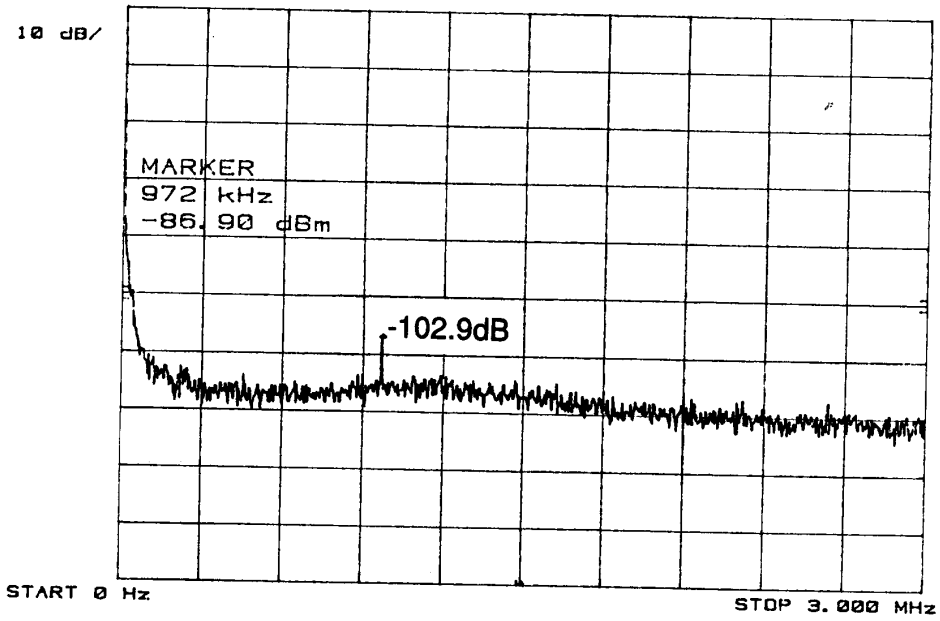


Fig. 16. Measured clock feedthrough.

transformation has taken place in either the criss-cross or the current-dumping configuration, the multiple-input loading effect needs to be compensated by adjusting the size of the passive resistors as discussed in detail in Section II–C.

C. Constant-Voltage R-MOSFET Scaling for THD Optimization

Even though one can choose a constant *ratio* for the R-MOSFET voltage scaling (example shown in the preceding section) uniformly throughout the filter, a more optimum choice of voltage scale factor F for each of the summing nodes should be used to minimize the larger noise due to larger F. This can be achieved by applying a constant-*voltage* R-MOSFET scaling. This approach will ensure a fixed voltage swing across the MOSFET's (which is proportional to the distortion) rather than allowing one tuning element to have the largest signal swing, causing it to be the dominant source of distortion. Shown in Fig. 8 is a graphical illustration of this method. The illustration in Fig. 8(a) shows that the node B of the constant-ratio scaling results in an unnecessarily small voltage swing across the MOSFET's. On the other hand, for node B in Fig. 8(b), the constant-voltage scaling allows the signal swing across the MOSFET's to be comparable to node A. The net result is an improvement in the dynamic range by reduced F at the particular node B with a negligible sacrifice in linearity.

VII. Experimental Results

Considering the process and temperature variation of the device parameters and the loading effect of the multiple inputs, an audio-band (22 kHz) fifth-order Bessel filter with a voltage scaling factor F varied between 2.5 to 5 (a fixed value for each of the integrators—see Section VI–C) was designed and fabricated using a double-poly 2-μm CMOS technology. The design steps include an L-C ladder to active R-C filter transformation, node-voltage scaling, dynamic range optimization with area constraint (Section VI–A), and finally active R-C to R-MOSFET-C transformation using constant-voltage scaling (Sections VI–B and VI–C). In the design verification phase of the Bessel filter, simulations were performed using an extended precision in numerical calculations with a particular interest in harmonic distortion results. The measurements were in good agreement with the predicted results from the simulation.

Shown in Fig. 9 is the prototype fifth-order Bessel filter using this linearity improvement technique. The box with the crossing arrows indicates the current steering portion of the variable resistance stage with the current-dumping topology, and the voltage scale factor F, given at each of the tunable elements, is the assigned value according to the constant-voltage scaling. Two-stage fully differential operational amplifiers with approximately 90-dB dc gain, 27-MHz unity-gain bandwidth, and 69° phase margin (from simulation) are used in the filter. A high-gain amplifier was chosen to minimize the distortion of the filter. The operational amplifier with its frequency compensation network (standard Miller compensation) is shown in Fig. 10. In the performance of the filter, the majority of distortion is expected to be coming from the MOSFET transistors in triode, and the passive resistors (undoped poly) are assumed to be sufficiently linear. Fig. 11 is a microphotograph of this fifth-order Bessel filter. The upper portion is composed of the five R-MOSFET-C integrators, including the passive components (R's and C's),

and the lower portion consists of the filter tuning circuitry and the bias circuit.

From the experimental results, the frequency response shown in Fig. 12(a) displays the tunability of the filter. Three different corner frequencies are chosen using different digital word settings for the binary weighted capacitors in place of C_1 in Fig. 6 (discussed in Section V). The control of the corner frequency can also be accommodated by changing the input reference clock, which is fixed at about 1 MHz in this test setup. Fig. 12(b) is the expanded passband for flatness measurement with the identical setting of the corner frequencies displayed in Fig. 12(a). As observed from the figure, the measured passband deviation is about 0.1 dB. The constant group delay of the Bessel filter can also be observed in Fig. 13. Again, the corner frequencies are the same but the plot is shown on a linear frequency scale. The group delay is sufficiently flat within the given passband for each of frequency settings, displaying the variation limited to no more than $1\mu s$. The output spectrum in reference to a 2-kHz 4-V_{pp} input is shown in Fig. 14. The output displays a very pure 2-kHz tone showing no distortion above -90 dB, bound by the limited resolution of the spectrum analyzer at that level. Using a separate distortion analyzer the measured THD versus input frequency is shown in Fig. 15. For the measurement taken with f_{-3dB} = 22 kHz (solid line), the plot verifies a close agreement with the simulation result of Fig. 5. The input signal is fixed at 4-V_{pp} differential. As predicted, this plot nicely captures the effect of the feedback loop on distortion. Consider again, as an example, the solid line representing a 22-kHz corner frequency setting. As the input frequency approaches the filter passband edge the loopgain is reduced and the distortion increases. Also in this figure the two separate lines represent the two different control voltages set to place the f_{-3dB} at 22 kHz and 32 kHz. Even though the THD partially depends on the control voltage itself, THD improvement resulting from the widening of the filter bandwidth is also observed in this plot. This implies that for an oversampling digital-audio application, if f_{-3dB} can be allowed to be higher than the audio band (22 kHz), even a greater linearity in the audio band (frequencies of interest) is feasible. Finally, while the clock feedthrough coming from the tuning loop is unseen at the output of the filter for the level of about 90 dB resolution, with an expanded window of frequency spectrum and without the presence of the input signal, a measurement is made at below -100 dB ($10\mu V_{rms}$), as shown in Fig. 16. Table II summarizes the measured performance of the prototype filter.

VIII. Conclusion

A method of implementing a highly linear tunable continuous-time filter in CMOS has been proposed. This linearity improvement technique reduces the signal swing across the nonlinear tunable devices by a voltage scale factor F. The feedback loops in the active filter configuration, which encircle the nonlinear current-steering MOSFET's, further reduce the THD by the feedback loop gain. This proposed technique greatly improves the THD at the cost of a slight increase in the noise power. The performance of the prototype filter displays the feasibility of digital-audio filters in CMOS and further extends the low-distortion capabilities of continuous-time CMOS filters.

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