CMOS High-Frequency Switched-Capacitor Filters for Telecommunication Applications

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***Abstract*—A digitally programmable high-frequency switched-capacitor filter for use in a switched digital video (SDV/VDSL) link is described. The highest available clock frequency in the system is 51.84 MHz ($f_s = 2f_{\rm clock} = 103.68$ MHz for double sampling) while the three desired low-pass corner frequencies (f_c) are 8, 12, and 20 MHz. The double-sampling, bilinear, elliptic, fifth-order switched-capacitor filter meets the desired −40-dB attenuation at $1.3f_c$, and −30 dB at $1.25f_c$. For the 12-MHz corner frequency setting, given the $2V_{pp}$ differential input, the measured worst case total harmonic distortion is −60 dB, with signal-to-noise ratio of 54 dB. The analog power dissipation is 125 mW from a 5-V power supply. The test results indicate that the clock frequency can be increased to 73 MHz without any ill effects. More measurements verify that an all-digital CMOS implementation, utilizing *metal-sandwich capacitors*, performs as well as the special-layer analog capacitors implementation, with a small reduction in the absolute corner frequencies. The prototype IC's are fabricated in a 0.35-μm 5-V (0.48 μm drawn) CMOS process.**

***Index Terms*—Bilinear, CMOS, digitally programmable, double sampling scheme, elliptic, high-frequency, switched-capacitor filter, telecommunications.**

I. Introduction

As THE demand for video and high-speed data continues to grow, a variety of system architectures using various modulation schemes surfaced as efficient solutions. Many of these systems are similar and often have a set of unique features that claim to fulfill the future telecommunications needs, but the two-fold emphasis that is common among all the architectures seems to be the robustness and the economical implementation of the system. Most likely this is why many efforts in this area have been in CMOS integration of a large digital system with many of the traditionally external analog components on chip.

Current systems available on the market and the trial sites are impressive and clearly demonstrate the robustness of the system, but undoubtedly they are multichip solutions (typically the separation of very large digital system and high-speed analog interface circuits), and there are significantly large amount of external passive inductance–capacitance (*LC*) filtering. Just the cost associated with the use of external filters is a problem in itself, but the physical parameters of external filters tend to limit the amount of achievable attenuation at higher frequencies. Practically achievable filter attenuation is in the range of −40 to −60 dB, and it is very difficult and expensive to design a filter that can attenuate as much as −80 dB. Given the driving force of increasing integration (ultimately the single-chip solution), these ill-defined conditions of the external filters naturally call for a maximized integration of these components.

A prototype, digitally programmable, high-frequency switched-capacitor (SC) filter was designed with this future single-chip solution in mind. The initial thoughts are that this SC filter would be used at the receiver end of the data link such that the discrete-time output of the SC filter may be directly fed into the receiver analog-to-digital (A/D) converter. From the existing system, where a very large amount of attenuation (−70 to −80 dB) is required due to highly attenuated receive signal and relatively large amount of transmit signal being coupled back into the receiver, the integrated SC filter can drastically reduce the external filtering requirements.

In Section II, the system description of the application in mind will be briefly explained in conjunction with the SC filter requirements. Presented in Section III are the high-frequency SC filter architecture and the implementation details of the circuit design. The experimental results of prototype IC's are given in Section IV, followed by concluding comments in Section V.

II. System Description

A. Variable-Rate SDV/VDSL System

One of the systems considered for switched digital video (SDV), a subset of video digital subscriber loop (VDSL), is a variable-rate system where downstream (*to* home) data rate may be as high as 51.84 Mbit/s and as low as 12.96 Mb/s. Specifically, the initial consideration is given for a system which works in three modes: 51.84, 25.92, and 12.96 Mb/s. The motivation behind these multiple-rate systems is that the system may be reconfigured to service a longer distance of unshielded twisted pair (UTP) while the data rate is reduced. The carrier frequency of the fixed-rate upstream (*from* home) data will also be reduced accordingly, to accommodate for the extended length of UTP.

Shown in Fig. 1 are the three approximate data profiles for the variable-rate (and -length) system. As shown in the figure, signal bands of the downstream data is extended to various upper frequencies. The SC filter requirements derived from this conceptual system are three corner frequencies (f_c) 20, 12, and 8 MHz, and the required attenuation of −30 dB at $1.25f_c$. This prototype SC filter is designed with the carrier-less amplitude/phase (CAP) modulation downstream signal in mind, which is identical to quadrature amplitude modulation (QAM) for all practical purposes, but the SC filter implementation in itself is not specific to any type of wide-band input signal. It

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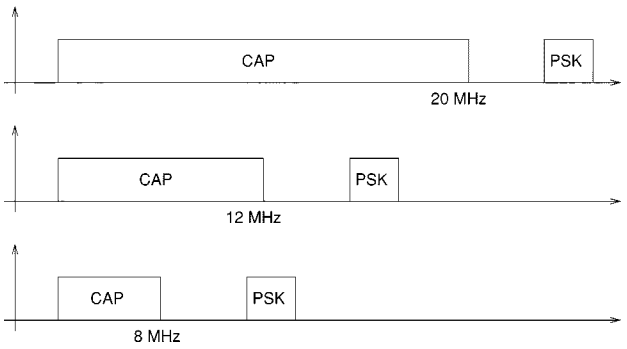

Fig. 1. Spectrum profiles for variable-rate system.

will be revealed in Section III that the wide-band nature of the input signal is assumed in order to improve capacitor matching while accepting suboptimal node-voltage scaling.

It is important to recognize that the choice of *switched-capacitor* filter is significant for this application. Self-tuned continuous-time filters were considered, but the unavoidable corner frequency variation typically in the range of ±5%–10% due to process variation and matching was found unacceptable (and factory trimming was to be avoided). This is due to the relative tight frequency allocations of the signal bands for the downstream and upstream pair.

The intended front end of the receiver system is composed of a variable-gain amplifier (VGA), followed by this SC filter, the discrete-time output of which is fed directly into an A/D converter.

B. Double-Sampling and Programmable Filter

Given the desired filter specifications, one of the key issues to be resolved was the 20-MHz corner frequency filter. For such high corner frequency, with respect to the sampling frequency that was limited by the highest clock frequency available on the system (51.84 MHz), it was found that the feedback factor around the op-amp was unreasonably small, and it was difficult to optimize the circuit design for three programmable frequency settings. The double-sampling SC filter seemed a logical option to consider. The issues regarding capacitor mismatch and unbalanced duty cycle for double-sampling scheme (DSS) also had to be considered [1], but the possibility of using an additional clock multiplier to generate 103.68-MHz clock was eliminated due to the significant increase in high-frequency clock phase jitter that the system needed to avoid.

The most significant drawback of the DSS is the uncanceled aliased input signal that is the direct result of the unbalanced duty-cycle input sampling [1]. According to the frequency profiles for the application in mind, however, the expected aliased input signal produced by the unbalanced double sampling of the SC filter is expected to be fully contained outside of the band-reject frequency ($1.25f_c$), and the z-domain SC filtering will filter out these unwanted aliased energy. Since the main purpose of this SC filter is to take out the unwanted upstream signal that is coupled into the received downstream signal, the input signal does not contain wide-band noise of any significance beyond the SC filter's *kT/C* noise.

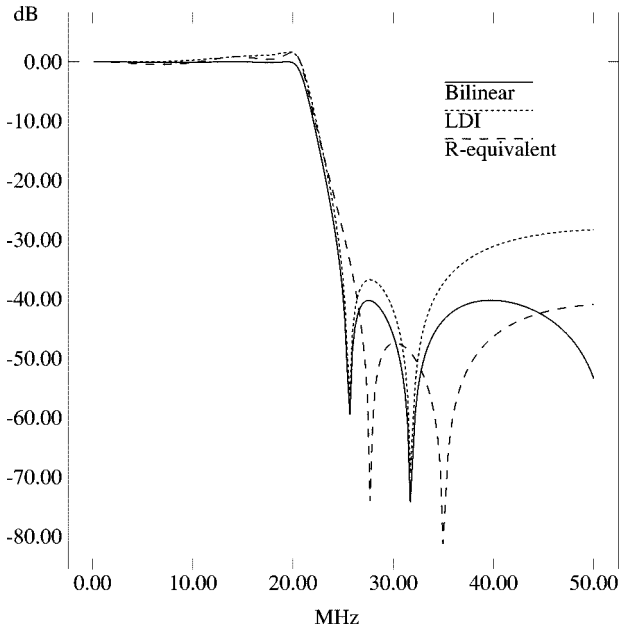

Fig. 2. Ideal z-domain frequency responses.

Last, the programmability for the three desired frequency settings is implemented by placing extra capacitors in parallel and digitally swapping and/or adding capacitors. Careful design can establish many programmable frequencies without having to implement separate filters or synthesizing variable frequencies. Synthesizing multiple frequencies was not an option due to the problem of added phase jitter as already mentioned above, and also due to the fixed-rate A/D converter that follows this SC filter.

III. Filter Implementation

A. Exact SC Filter Synthesis Using Bilinear Transformation

Active *LC* ladder synthesis was chosen for this SC filter design. Even though the low pass-band sensitivity of the *LC* ladder [2], [3] was not an absolutely necessary requirement, this prototype filter was designed with the desire to gauge the achievable accuracy of a CMOS implementation for high-frequency SC filters.

Given that the desired corner frequencies are significantly high (20, 12, and 8 MHz) in comparison to the sampling frequency of 103.68 MHz (twice the clock frequency), both the commonly used *resistor-equivalent* approach ($R_{\text{eq}} \approx 1/f_sC$) and the well-known standard lossless discrete integrator (LDI) design were found insufficient for this high-frequency SC filter application. This is because of the *frequency-dependent termination* that is inherent in the above approximations. Among a variety of *exact* SC filter synthesis [4]–[10], Datar, Sedra, and Snelgrove outline a convenient set of rules for an exact implementation using Bilinear transformation [9], [10]. This set of design guidelines are used for the prototype fifth-order elliptic SC filter implementation.

For a clear distinction, a set of ideal z-domain simulation results for the 20-MHz corner frequency is shown in Fig. 2. The resistor-equivalent design (dashed line) displays obvious flaws

in the passband as well as the reject-band (even though the absolute corner frequency error has been compensated), while the standard LDI (dotted line) design displays an improved passband behavior with a further degradation in the reject-band. The exact Bilinear design yields the desired response over all frequencies.

The bilinear implementation will require adjustments in the capacitor values throughout the commonly known active *LC* ladder SC filter structure, but one very important aspect of the bilinear implementation is that the sampled input of the SC filter needs to perform the $1+z^{-1}$ operation before the signal is further processed through the *LC* ladder. This is simply the net result of necessary modifications required in order to compensate for the frequency-dependent termination. An extra stage for delaying the input by one sample delay is used in this implementation. Other techniques suggesting modified switching configurations [7], [8] still require that the input is a sampled data (needing a sample-and-hold) for a high-frequency application (higherf_c/f_s ratio), and the techniques are not directly applicable to double-sampling scheme.

The input sample delay cell is shown in Fig. 3. The DSS is incorporated in the figure, but a single-ended version is illustrated for simplicity while the circuit realization is fully differential. It is a very straightforward implementation for a half-cycle delay (one phase delay is equivalent to one sample delay in DSS), capable of high-speed operation. This sample delay cell does not have an explicit stabilizing loop during the nonoverlapping clock phases, and no problem associated with this was observed in the lab. However, placing an unswitched small integrating capacitor (≈5–10% of the sampling capacitor) can avoid the possibility of op-amp output glitching out of range without significantly affecting the overall transfer function.[1] (≈5% leads to ≈0.3-dB droop in the worst case corner frequency setting.) The output of this sample delay cell as well as the unsampled input is fed into the active ladder portion of the SC filter. The input *RC* network of the ladder portion also works as the sampling circuit for the unsampled input.

By following the design process outlined in [9] and [10], and after applying a semi-optimum node-voltage scaling, the resulting switched-capacitor structure is shown in Fig. 4, and the normalized component values for a 20-MHz filter are shown in the first column of Table I. The semi-optimum node-voltage scaling was chosen to maintain integer multiple unit-size capacitor values for all fixed-size capacitors. The Fig. 4 represents a single-ended, single-sampling implementation, but the prototype realization is fully differential, double sampling, and utilizes early-phase sampling to minimize signal-dependent charge injection. Double-sampling simply implies that there is a duplicate set of fixed-size capacitors (omitting the integrating and coupling capacitors C_3,C_6,C_9,C_{12},C_{15}, and C_{21}–C_{24}) that will operate with the opposite phases (e.g., $\phi_2 \rightarrow \phi_1$,$\phi_1{}' \rightarrow \phi_2{}'$, etc.) similar to the sample delay cell in Fig. 3.

The corner frequency programmability is implemented by altering only the integrating and coupling capacitors. A set of parallel capacitors for each capacitance is digitally switched in/out. The three columns of Table I lists the calculated integrating

[1]The author appreciates the feedback from an anonymous reviewer.

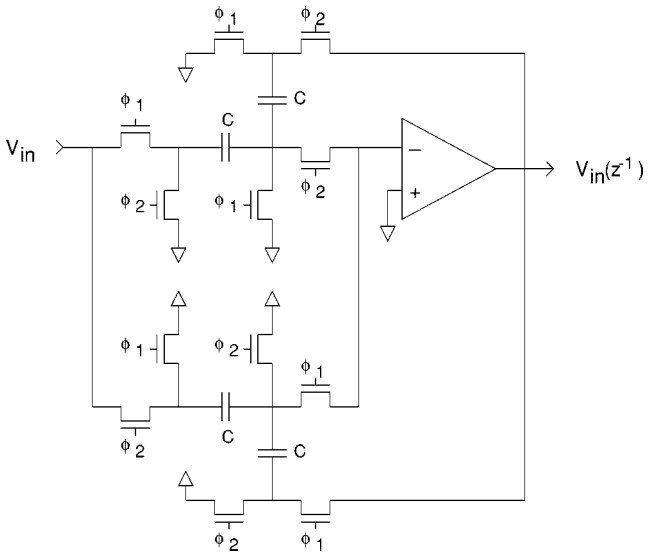

Fig. 3. Single-ended (double-sampling) version of sample delay cell.

and coupling capacitor values for 20-, 12-, and 8-MHz corner frequencies. As an example, the implementation of the capacitances C_3 andC_{24} is shown in Fig. 5. In order to establish the desired values at all three programmable settings, C_3 adds on extra capacitors as the corner frequency is lowered from 20 to 12 to 8 MHz, but C_{24} will switch in only one of the three capacitors for each frequency setting.

B. Circuit Design

One of the important aspect of high-frequency SC filter design is the op-amp design. Most often, single-stage folded-cascode op-amps are used in a variety of SC applications. Because of the purely capacitive loads in switched-capacitor circuits, the amount of op-amp compensation is directly proportional to the amount of capacitive loading at the output. More important, for high dynamic range applications requiring large signal-to-noise ratio (SNR), a single-stage op-amp performs with the least amount of sampled-noise resulting from the op-amp itself. This is because all thermal noise generated in the op-amp is frequency shaped by the compensating load capacitor.

Despite these traditional advantages of single-stage folded-cascode op-amps, there are drawbacks that become significant in high-frequency SC filter design. One drawback is that, in order to maintain a high unity-gain frequency, the G_m of an op-amp has to be very large, resulting also in large power dissipation. This is especially a problem in a CMOS folded-cascode op-amp due to multiple branches of bias current used. The other drawback is that the op-amp input capacitance also ends up being large due to the high transconductance required. When a small unit-size capacitance is used for high-frequency performance, and relatively small integrating capacitors due to high f_c/f_s ratio, the feedback factor around an op-amp becomes greatly reduced due to this high input capacitance.

Another common choice for op-amp used in SC circuits is the telescopic op-amp. The telescopic op-amps have reduced power consumption in comparison to folded-cascode op-amps because of reduced number of current branches, but the drawback due

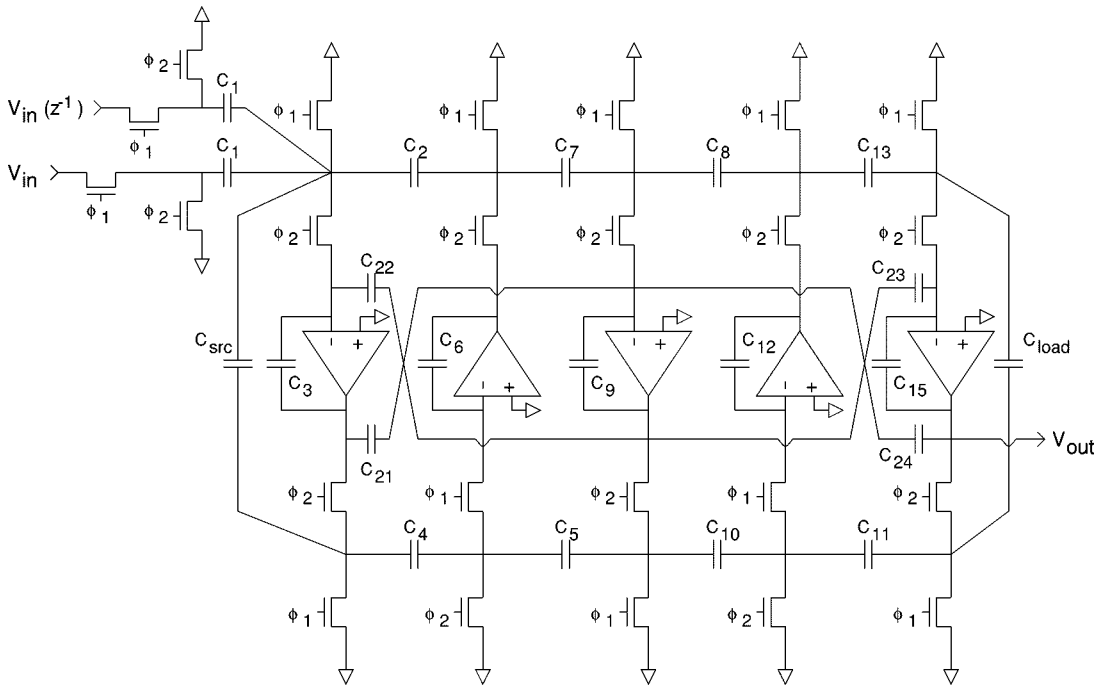

Fig. 4. Single-ended single-sampling version of fifth-order filter.

TABLE I
NORMALIZED CAPACITOR SIZES

Name	20-MHz	12-MHz	8-MHz
C_3	2.313	4.298	6.982
C_6	1.387	2.526	3.887
C_9	7.495	10.917	15.753
C_{12}	3.008	5.478	8.430
C_{15}	1.958	3.330	5.258
C_{21}	1.338	1.290	1.545
C_{22}	1.338	1.290	1.545
C_{23}	2.543	3.046	4.079
C_{24}	1.696	2.031	2.719
C_1	2.0		
C_2	5.0		
C_4	1.0		
C_5	1.0		
C_7	5.0		
C_8	5.0	same	same
C_{10}	3.0		
C_{11}	2.0		
C_{13}	5.0		
C_{src}	3.0		
C_{load}	2.0		

to large op-amp input capacitance is unchanged. Another drawback, specific only to this prototype SC filter, is that the telescopic op-amp will require complementary transmission gate switches due to higher common-mode voltage at the op-amp output and lower common-mode voltage at the input. In order to minimize increased routing complications regarding double-sampling scheme implementation, an initial design decision was

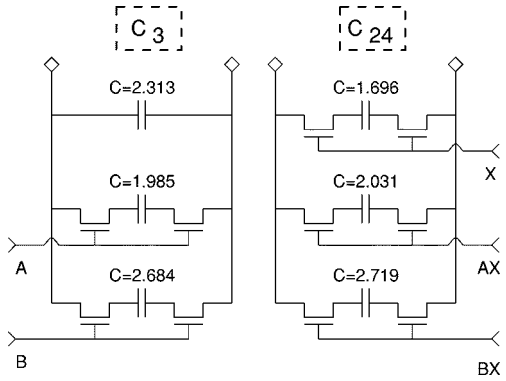

Fig. 5. Examples of programmable capacitor banks.

made to use only the N-channel switches and operate the entire SC circuit with a low common-mode voltage.

The above discussion is summarized in Fig. 6. The final choice of the op-amp architecture, as also shown in the figure, is a two-stage op-amp. Because the first stage is no longer driving the output load, the power consumption in the telescopic portion is negligible to the second/buffer stage, and this also produces a low input capacitance op-amp. The frequency compensation is also contained within the first stage. The second stage acts as a buffer to the higher capacitance output loads and at the same time provides level shifting to yield a lower output common-mode voltage. The bulk of the op-amp power consumption is contained within this second/buffer stage, and the main drawback of this two-stage op-amp is the increased sampled noise due to the *unshaped* thermal noise coming from the second stage.

A more detailed schematic of the two-stage op-amp used in the prototype filter is shown in Fig. 7. A complete bias circuit (trivial portions are not shown) is an integral part of each op-amp in order to minimize coupling between the op-amps

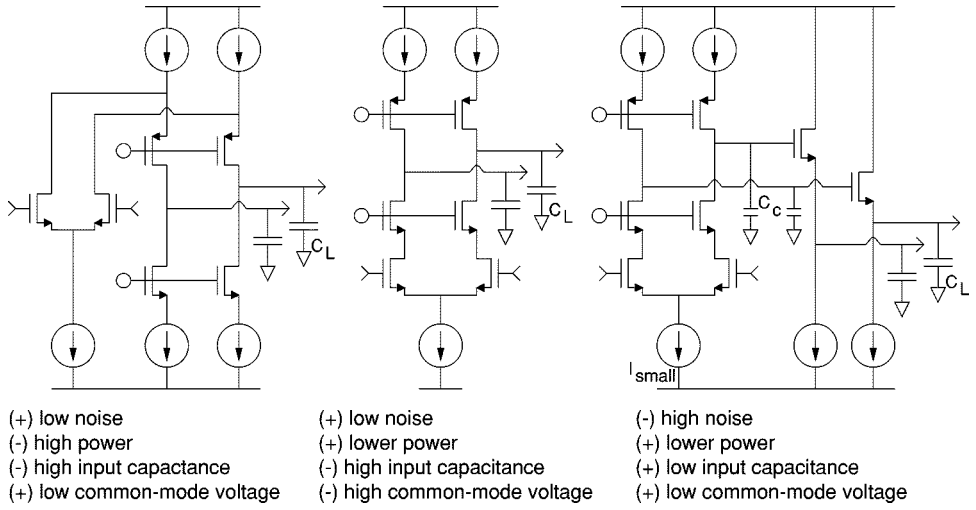

Fig. 6. Comparison of op-amp architectures.

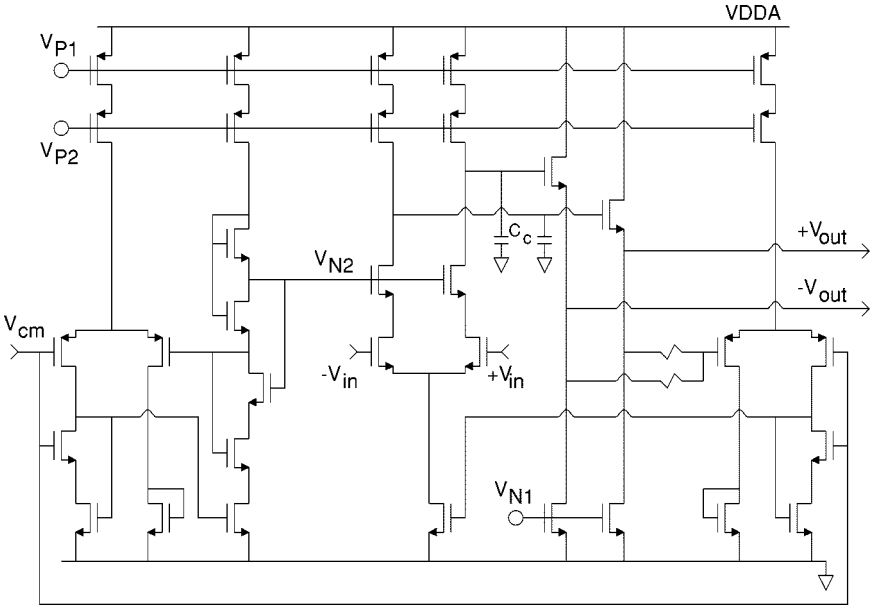

Fig. 7. Differential two-stage operational amplifier.

used throughout the filter. For a unit-size capacitor as small as 0.1 pF (chosen value for this prototype filter), the op-amp input capacitance affecting the loop-gain around each op-amp is minimal due to this two-stage architecture, where the output loading is solely driven by the large buffer (second stage). A very small amount of capacitance was needed at the output of the first stage to frequency compensate the op-amp. Also, a sufficiently wide bandwidth of 80 MHz is achieved for the common-mode feedback loop (additional common-mode frequency compensation not shown the figure).

The telescopic first stage is only able to yield a marginal op-amp dc gain. A small amount of variation in the filter's frequency response (reduced dc gain, a small shift in corner frequency, a small frequency drooping, etc.) due to the limited dc gain was found acceptable for this high-frequency application, and no correction schemes, such as the precise op-amp gain (POG) technique [11] or gain-boosting techniques [12], [13], were attempted. The simulated nominal op-amp dc gain of this two-stage op-amp is 54 dB, with a very small variation over process and temperature.

Shown in the left portion of Fig. 7 is a floating version of the Sooch cascode biasing [14]. In order to attain replica biasing with respect to the op-amp's differential input (same as the common-mode voltage), which tracks process and temperature variations, the Sooch cascode circuit is simply placed inside a feedback loop. The net result is the maximized voltage swing at the output of the telescopic stage.

Among all of the op-amps used in the prototype SC filter, the simulated worst case (slow process extreme, layout parasitics, high-temperature, 20-MHz corner frequency setting, etc.) loop bandwidth and phase margin were found to be approximately 180 MHz and 60°. This is a bit short of the popular rule-of-thumb requiring loop bandwidth to be five times the clock frequency [12]. Some side-effects resulting from this limited loop bandwidth will be revealed in the lab measurements. For 12- and 8-MHz corner frequency settings, the loop band-

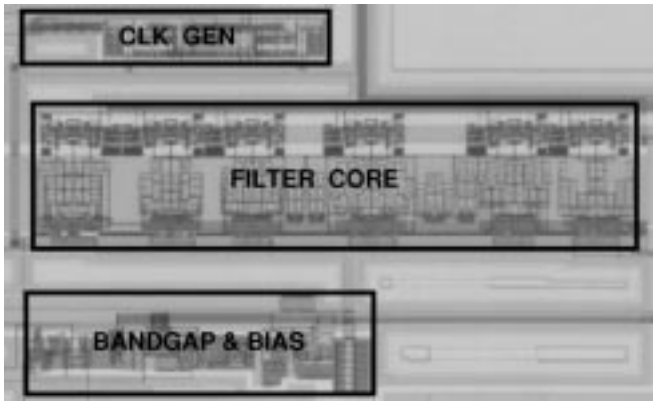

Fig. 8. Die photograph of prototype IC.

widths comfortably exceed this rule-of-thumb requirement. Various other rules-of-thumb regarding high-frequency SC filter design such as the maximum *RC* time constant of sampling switches and minimum slew-rate requirements were fully satisfied with large design margins.

Last, a combination of various sampled-noise simulation techniques were employed in getting a good approximation for the filter's SNR. Knowing that the thermal noise coming from the second stage of the op-amp significantly degraded the total SNR, it was important to ensure that the IC would yield required 8-bit level SNR. A set of modified simulation techniques for approximating total sampled noise (including op-amp and *kT/C* noise) proved to be very well correlated to the measurement. The modified techniques outlined in [16] and [17] allowed the use of a standard circuit simulator such as SPICE, while correctly emulating z-domain transfer functions that were not contained in [18].

IV. Measurement Results

The programmable bilinear fifth-order elliptic SC filter was designed using metal-over-metal (special layer) analog capacitors. The die photograph of prototype IC fabricated in a 0.35-μm, 5-V (0.48 μm drawn) CMOS process is shown in Fig. 8. The area of the entire photograph is 2 mm^2, and the active die area of the filter core is less than 0.7 mm^2. A very small unit-size capacitor of 0.1 pF is used in this implementation. There are many duplicate sets of capacitors due to the double-sampling scheme used.

The common-mode voltage of the filter is 1.5 V, and the signal swing is 2-V peak-to-peak differential. The measurements are taken with 4.5-V power supply and room temperature unless noted otherwise.

Shown in Fig. 9 is the "Monte Carlo" measurement of nine devices, where a set of three devices each are from "fast," "nominal," and "slow" split process variation (intentional). It can be observed that the corner frequency variation is well within 1% for all three programmable corner frequencies, as intended and necessary for the application in mind.

Shown in Fig. 10 is the comparison of measured (solid line) and simulated (dashed line) frequency responses. The simulation result is from the tool WATSNAP [19] where only the modeled finite-gain, two-pole op-amp is used in conjunction with finite switch resistance. Considering the lack of detailed parasitics incorporated into the simulation and the nonideal testing environment, measurement results are in excellent agreement with the simulation results.

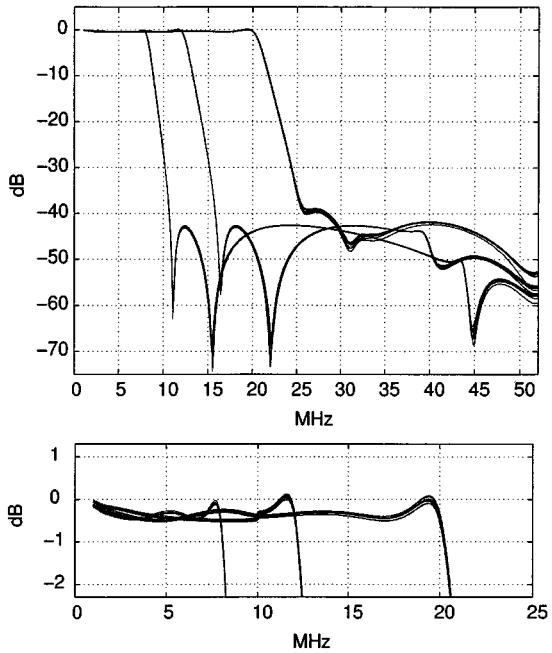

Fig. 9. Measurement of multiple (nine) devices.

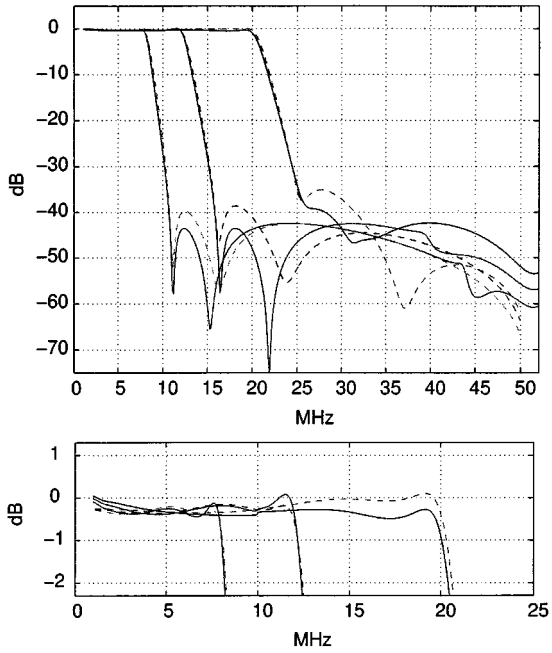

Fig. 10. Measurement (solid) versus simulation (dashed).

In addition to Fig. 9, demonstrated in Fig. 11 is a tight control of the frequency response for ambient temperature variations from –40 to +85 °C. These results reaffirm the required corner frequency accuracy obtained via switched-capacitor implementation.

Fig. 12 shows single-tone distortion measurements for three programmable profiles. The input tones are at ≈1/3 of the

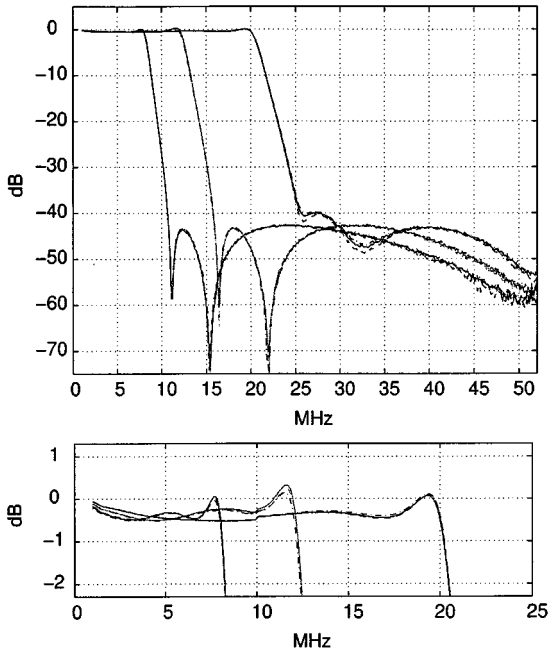

Fig. 11. Ambient temperature variation from −40 °C to +85 °C.

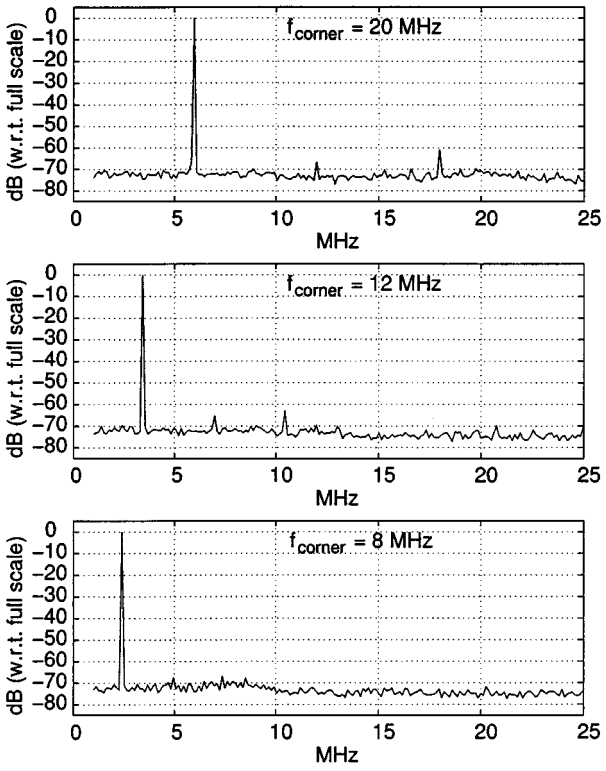

Fig. 12. Single-tone distortion measurement.

corner frequency in order to capture the worst case situation for the dominant third harmonic. The measurements at +85 °C are found to be about 2 dB worse. The multitone/intermodulation distortion shown in Fig. 13 displays further degraded performance in comparison to the single-tone test. This is mainly due to the fact that the peaks of the filter frequency response at some of the internal nodes are greater than 0 dB (≈2 dB). It

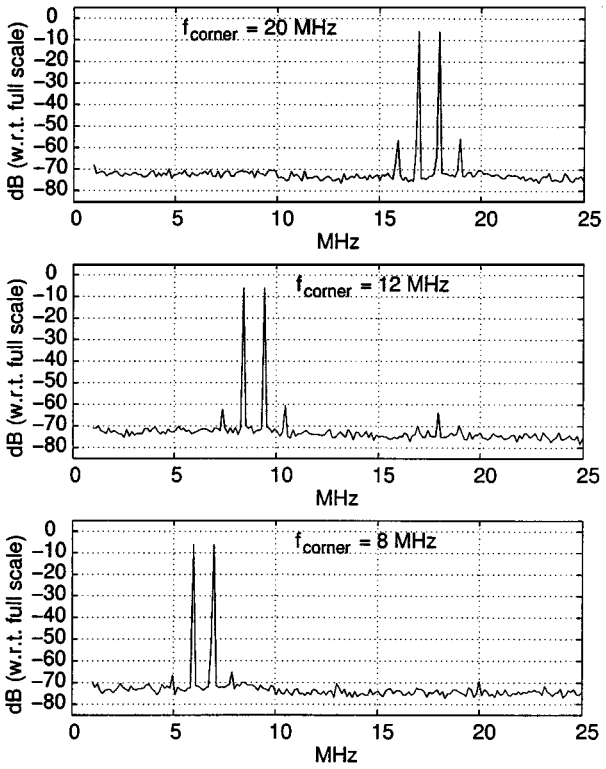

Fig. 13. Intermodulation distortion measurement.

was mentioned in Section III that a semi-optimum node-voltage scaling was used in order to maintain integer multiple ratios for the double-sampling capacitors. In the SDV application, the broad-band nature of the input signal will guarantee that the internal nodes will never saturate.

Shown in Fig. 14 are the dynamic range (SNR) measurements and simulation results obtained by incorporating techniques outlined in [16] and [17]. The lower plot is the integrated value (thus SNR) of the noise floor shown in the upper plot. The measurement results (solid lines) are well correlated to the simulation results (dashed lines). This measurement as well as previous distortion measurements include the noise/distortion from the pseudodifferential output buffer (integrated next to output pads only for the test/evaluation purposes) that can only degrade the measurements. Simulation results indicate that the degradation that may result from the test buffers is negligible.

Last, shown in Fig. 15 are the "Monte Carlo" measurements similar to Fig. 9, except that these devices use only the purely digital process—using *sandwich capacitors* made of poly and all metal layers. The measurement results indicate a slightly larger corner frequency variation due to higher random mismatches in the capacitors used, but more importantly shifted (reduced) corner frequencies. This is due to somewhat crude layout of noninteger size capacitors in these sandwich structures (the integrating and notch capacitors), and the large percentage of bottom-plate capacitance in comparison to the top-plate that was not included in simulation. These factors can easily be taken into account, and a set of accurate corner frequencies may be obtained. The only significant drawback in the all-digital process implementation is the increased capacitor area, approximately by a factor of two.

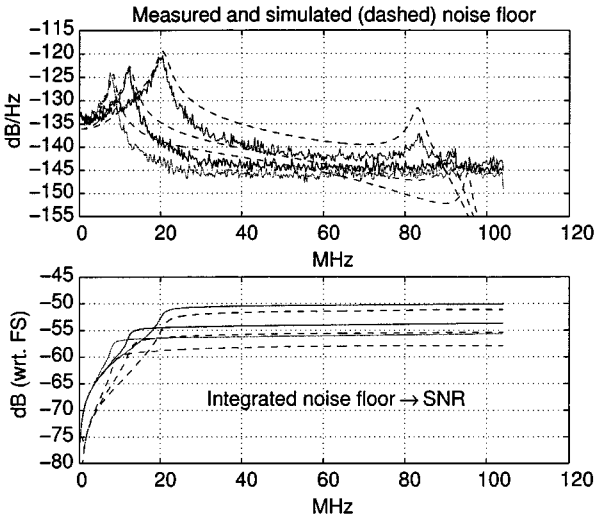

Fig. 14. Noise floor and SNR measurement (solid) versus simulation (dashed).

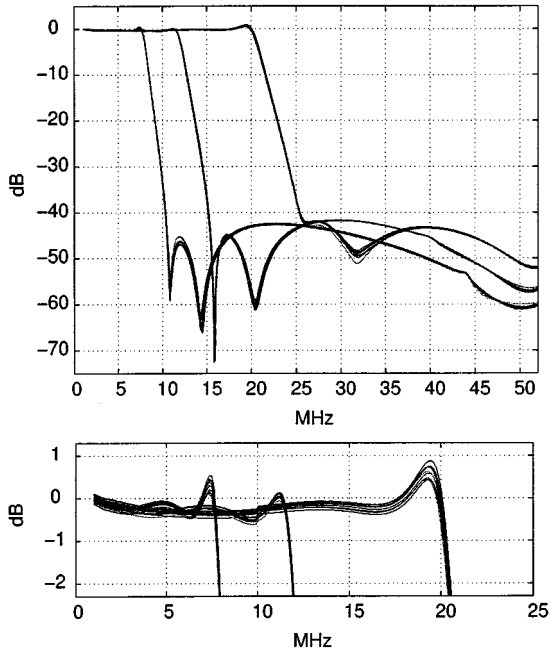

Fig. 15. Measurement of purely digital process implementation.

V. Conclusions

A programmable high-frequency, double-sampling, switched-capacitor filter implementation was described. The bilinear fifth-order elliptic filter prototype demonstrates accurate performance required by the multirate switched digital video application in mind. For the given 51.84-MHz clock (sampling rate of 103.68 MHz with double sampling), the successful demonstration of digitally programmable corner frequencies of 8, 12, and 20 MHz allows a compact and flexible use of this type of filter implementation for variety of applications where programmability is needed, even for a large corner frequency to sampling frequency ratio. Filter architectural issues as well as op-amp design tradeoffs were mentioned. Pros and cons of the final implementation as well as the important aspects of double-sampling schemes were also discussed.

Acknowledgment

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References

[1] J. Rijns and H. Wallinga, "Spectral analysis of double-sampling switched-capacitor filters," *IEEE Trans. Circuits Syst.*, vol. 38, pp. 1269–1279, Nov. 1991.

[2] W. A. Rutala, M. F. Gergen, and D. J. Weber, "Comparative evaluation of the sporicidal activity," *Amer. J. Infect. Contr.*, vol. 26, no. 4, pp. 393–398, May 1998.

[3] F. E. J. Girling and E. F. Good, "The leapfrog or active-ladder synthesis," *Wireless World*, vol. 76, pp. 341–345, 1979.

[4] M. Tawfik, C. Terrier, C. Caillon, and J. Borel, "Exact design of switched capacitor band pass ladder filters," in *Proc. IEEE Int. Symp. Circuits*, May 1983, pp. 793–796.

[5] S. O. Scanlan, "Analysis and synthesis of switched-capacitor state-variable filter," *IEEE Trans. Circuits Syst.*, vol. CAS-28, pp. 85–93, Feb. 1981.

[6] J. Taylor, "Exact design of elliptic switched-capacitor filters by synthesis," *Electron. Lett.*, vol. 18, no. 19, pp. 807–809, Sept. 16, 1982.

[7] M. Lee, G. Temes, C. Chang, and M. Ghaderi, "Bilinear switched-capacitor ladder filters," *IEEE Trans. Circuits Syst.*, vol. CAS-28, pp. 811–822, Aug. 1981.

[8] R. Gregorian and G. Temes, *Analog MOS Integrated Circuits for Signal Processing*. New York: Wiley, 1986.

[9] R. Datar and A. Sedra, "Exact design of strays-insensitive switched-capacitor ladder filters," *IEEE Trans. Circuits Syst.*, vol. CAS-30, pp. 888–898, Dec. 1983.

[10] A. Sedra and M. Snelgrove, "Switched-capacitor filter synthesis," in *Design of Analog-Digital VLSI Circuits for Telecommunications and Signal Processing*, 2nd ed. Englewood Cliffs, NJ: Prentice-Hall, 1994, ch. 7.

[11] A. Baschirotto, F. Montecchi, and R. Castello, "A 15-MHz 20-mW BiCMOS switched-capacitor biquad operating with 150 Ms/s sampling frequency," *IEEE J. Solid-State Circuits*, vol. 30, pp. 1357–1366, Dec. 1995.

[12] L. Larson and G. Temes, "Switched-capacitor building-blocks with reduced sensitivity to finite amplifier gain, bandwidth, and offset voltage," in *Proc. IEEE Int. Symp. Circuits and Systems*, May 1987, pp. 334–338.

[13] Y. Huang, G. C. Temes, and P. Ferguson, "Experimental results on reduced harmonic distortion with correlated double sampling," *Dig. Symp. VLSI Circuits*, pp. 224–227, June 1998.

[14] N. Sooch, "MOS cascode current mirror," U.S. Patent 4 550 284, Oct. 1985.

[15] G. Fischer and G. Moschytz, "Frequency limitations of SC networks," in *Proc. Eur. Conf. Circuit Theory and Design*, Sept. 1983, pp. 300–305.

[16] J. H. Fischer, "Modeling switched-capacitor filters and Δ–Σ converters in ADVICE," Lucent Technologies Bell Labs Internal Memo. 538 832 000-970 519-01 IM, May 19, 1997.

[17] T. Misawa, "Analysis of switched capacitor circuits with classical computer simulation program," AT&T Bell Labs Tech. Memo., May 1981.

[18] J. H. Fischer, "Noise sources and calculation techniques for switched capacitor filters," *IEEE J. Solid-State Circuits*, vol. SC-17, pp. 742–819, Aug. 1982.

[19] J. Vlach and A. Opal, "WATSNAP, program for analysis of externally clocked linear switched networks," Department of Electrical and Computer Engineering, University of Waterloo , 1992.

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