A 1-V 10-MHz Clock-Rate 13-Bit CMOS $\Delta\Sigma$ Modulator Using Unity-Gain-Reset Opamps

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***Abstract*—The problem of low-voltage operation of switched-capacitor circuits is discussed, and several solutions based on using unity-gain-reset of the opamps are proposed. Due to the feedback structure, the opamps do not need to be switched off during the reset phase of the operation, and hence can be clocked at a high rate. A low-voltage $\Delta\Sigma$ modulator, incorporating pseudodifferential unity-gain-reset opamps, is described. A test chip, realized in a 0.35-μm CMOS process and clocked at 10.24 MHz, provided a dynamic range of 80 dB and a signal-to-noise + distortion (SNDR) ratio of 78 dB for a 20-kHz signal bandwidth, and a dynamic range of 74 dB and SNDR of 70 dB for a 50-kHz bandwidth, with a 1-V supply voltage.**

***Index Terms*—ADC, charge-pump circuits, delta–sigma, low voltage, sigma–delta, switched-capacitor circuits, switched opamp.**

I. Introduction

STATE-OF-THE-ART fine-linewidth CMOS technologies allow fully integrated mixed-signal (digital and analog) circuits on the same chip. This increases the level of integration, and permits higher clock frequencies, and hence, the implementation of more sophisticated and powerful digital systems on a single IC. However, the design of analog circuits then becomes more challenging. Currently, the most critical issues affecting analog circuits include thermal noise, digital noise coupling, high clock rates, low supply voltages, and reduced signal swings.

In this work, circuit design techniques for low supply voltage and reduced signal swing will be discussed. Low supply voltage is important in two contexts: reliability and power dissipation. The miniaturization on IC structures in all three dimensions introduces two critical issues related to reliability [1]: long-term voltage stress on the gate oxide, and short-term junction breakdown due to high voltages. Low-voltage (LV) circuit design must take these into account. The demand for low power dissipation is often motivated by the desire to achieve long battery life for portable devices. In digital circuits, lowering the supply voltage decreases the power consumption. However, in analog circuits, lower supply voltage typically increases, rather than decreases, the power dissipation for a specified performance. In addition, the low voltage supply may make it difficult, if not impossible, to turn on those switches which operate at signal voltage levels. This makes the realization of the commonly used switched-capacitor (SC) circuits impractical. An ingenious technique [10]–[16] for solving this problem is based on switching the operational amplifiers (opamps) of the SC stages on and off in alternating clock phases. However, the disabling of the amplifiers slows down the operation. In this paper, a novel solution is proposed, based on the periodic resetting (rather than shutting down) of the opamp. This enables faster operation, since the opamp remains in its linear region of operation at all times.[1]

Section II will discuss the implications of LV supply for SC circuits, and available techniques for the design of LV SC circuits, especially LV SC integrators. Section III will describe the proposed novel circuit technique using unity-gain-reset opamps. Finally, in Section IV, the design and performance of a specific LV $\Delta\Sigma$ analog-to-digital modulator implementation is discussed.

II. Low-Voltage Switched-Capacitor Circuits

In many analog and mixed-signal devices, SC circuits perform linear analog signal processing. They are used in various practical applications, such as data converters, analog filters, sensor interfaces, etc. However, there are some fundamental limitations on the operation of switches with low supply voltages. The low supply voltage may not allow enough overdrive to turn on the transistors used as switches even if complementary switches are used.

As seen in Fig. 1, the nMOS transistor conducts for an input signal from 0 up to $V_{dd}-V_{t,n}$ and the pMOS transistor conducts from $|V_{t,p}|$ to V_{dd}. The operation fails when the supply voltage is less than $|V_{t,p}| + V_{t,n}$. In this case, none of the switches will be turned on for some signal values. Hence, the signal is no longer obtained at the output [2].

The basic building block of most SC circuits is the stray-insensitive integrator shown in Fig. 2. Switches S1 and S5 operate at the signal voltage, while switches S2 and S3 are connected to signal ground, and S4 is connected to virtual ground. The problem described above will occur for the "floating" switches S1 and S5.

There are several solutions proposed to the problem of operating the floating switches. These include using low-threshold

Manuscript received October 29, 2001; revised January 21, 2002. This work was supported by the National Science Foundation Center for Design of Analog-Digital Integrated Circuits (CDADIC).

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Publisher Item Identifier S 0018-9200(02)05863-8.

[1]As pointed out by one of the reviewers, the proposed technique shares several features with the switched-opamp (SO) method: it eliminates the signal-level switches and it switches the function of the opamp between clock phases. It can be thus considered to be an improved variant of the SO technique.

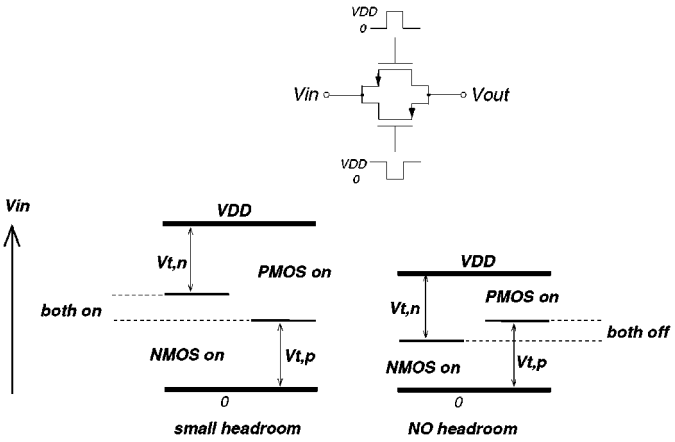

Fig. 1. Fundamental problem of CMOS switch.

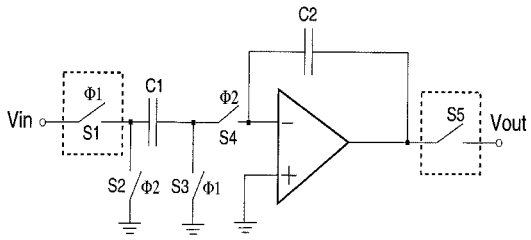

Fig. 2. A conventional SC integrator.

devices [3], charge-pump circuits [6], [7], and switched-opamp circuits [10]–[14]. The limitations of these techniques are discussed next.

There exist CMOS processes with low threshold voltages, at least for the nMOS devices [3]. However, when the threshold of the device is lowered, its leakage current is also increased during the "off" period of the switch. This may be unacceptable for SC circuits, where charge conservation is important, and charge loss may cause harmonic distortion. Another drawback is the high cost of a dedicated low $V_{\rm th}$ process.

A common solution to the LV switch problem is to employ charge-pump (voltage multiplier) circuits [4], [5] to generate higher supply voltages on the chip. This technique provides a convenient way of designing LV SC circuits, since it allows the rest of the circuit to use low supply voltage and save power, while the switches utilize the boosted voltage from the charge pump. However, the charge-pump circuitry may require substantial chip area and power. Also, the gate oxide may be overstressed by the boosted voltage for some signal voltages.

There are also other techniques similar to the charge-pump method. These apply local voltage boosting (bootstrapping) at the gates of the switches [8], [9]. These techniques offer an elegant solution to the LV switch problem. However, they require complex circuitry to realize a single switch, and may also introduce reliability issues.

Yet another solution is based on the use of switched opamps (SOs) [10]–[14]. The main idea is to replace the floating switch S5 in Fig. 2 by a switch which grounds the output terminal of the opamp (S2 in Fig. 3). To allow this, the opamp must be switched on and off during $\Phi 1$ and $\Phi 2$, respectively, and its output voltage is grounded only when it is off. This circuit is

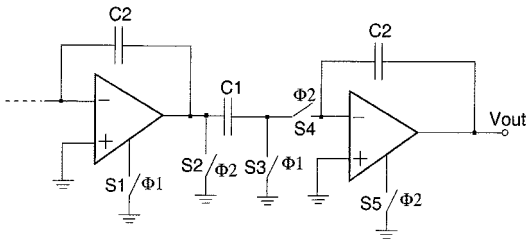

Fig. 3. Switched-opamp integrator.

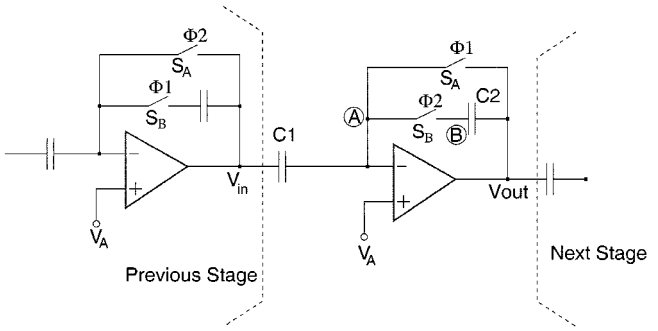

Fig. 4. Reset-opamp SC integrator.

compatible with submicron CMOS technology because none of components require high voltage. On the other hand, since the opamps are turned off during one half clock cycle, the SO circuit suffers from speed limitation due to the transients introduced by the required powerup/powerdown of the opamps. This limits the clock frequency. Recently, techniques have been reported which increase the frequency range of SO circuits [15], [16].

The technique proposed here is conceptually similar to the switched-opamp technique, in that it also sets the opamp output voltage to a fixed value in one clock phase, and thus eliminates the floating switch. It is illustrated in Fig. 4. However, in our structure, the opamp is always in linear operation. This eliminates the transient settling time required in the SO, and hence the circuit can be operated with a higher clock frequency. The new structure may be referred to as the *reset-opamp* (RO) technique, because the opamp output is reset during one clock phase [19]–[21].

Note that a straightforward implementation of this stage would introduce practical problems due to forward biasing some p-n junctions in the $\rm S_B$ switches. The operation of the circuit, and the practical problem mentioned above (as well as its solution) will be described in the next section.

III. Reset-Opamp Low-Voltage Integrators

Consider the SC integrator shown in Fig. 4, where $C1$ is the sampling capacitor and $C2$ is the integrating capacitor. During $\Phi 1 = 1$, $C1$ acquires a charge $C1(V_{\rm in} - V_A)$. At the same time, the opamp output voltage of the second stage is reset to V_A. When next $\Phi 2 = 1$, the output of the previous stage is reset to V_A, hence, $C1$ discharges into the virtual ground of the opamp at the second stage. Also, the integrating capacitor $C2$ is reconnected into the feedback branch during this phase ($\Phi 2 = 1$) and absorbs $C1$'s charge. The resulting $V_{\rm out}$ is sampled by the input capacitor of the next stage. The input–output relation of

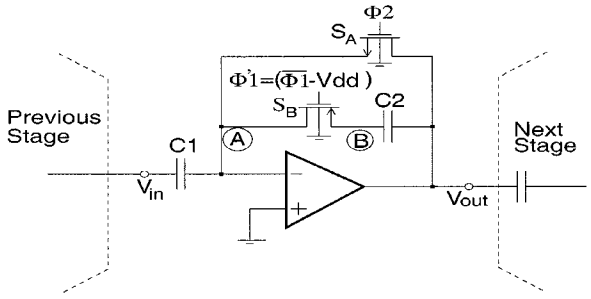

Fig. 5. Low-voltage integrator with MOS switches.

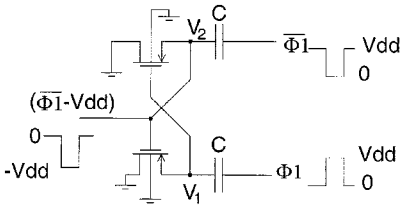

Fig. 6. Level-shifted clock generator.

the stage containing $C1$ and $C2$ is therefore that of a noninverting integrator with a half-clock-period delay.

Note that (at the cost of two additional switches) the right-hand terminal of $C1$ can be disconnected from the virtual ground and grounded during the $\Phi 1 = 1$ phase. Note also that most discussions in this paper refer to single-ended circuit realizations. In practical realization, the implementation is usually differential or pseudodifferential [21].

As mentioned in the previous section, the obvious realization of the circuit of Fig. 4 leads to some practical difficulties. Assume that the analog ground voltage is $V_A = V_{SS} = 0$, i.e., that the input common-mode voltage is true ground, as may be the case if the opamps have pMOS input devices. Then the conventional realization of the circuit would use nMOS devices for both S_A and S_B, since these are easy to turn on when they operate at ground bias. Assume also that the output voltage at the end of a $\Phi 2 = 1$ phase approaches V_{dd}. Then, at the beginning of the next $\Phi 1 = 1$ phase, V_{out} is pulled down to ground by S_A, and the floating node B (between S_B and $C2$) is pulled down to about $-V_{dd}$ by $C2$. Since node B is connected to the n+ source diffusion of S_B, the source-to-substrate junction of S_B will be forward biased, and $C2$ will lose charge to the substrate.

In the following, several techniques will be described for avoiding the forward-biased junction problem in this integrator.

A. Integrator Realization Using a PMOS Switch and Level-Shifted Clock

A possible solution to the junction leakage problem is illustrated in Fig. 5. As before, the circuit uses an nMOS implementation for S_A, but now a pMOS device is used as S_B. Clearly, here the voltage drop from 0 to $-V_{dd}$ at node B will cause the source-to-well junction to be reverse biased. Hence, the charge loss from $C2$ is avoided.

The remaining problem is that the grounded pMOS switch device requires a negative clock voltage for conduction. A level-shifting circuit which can realize this is shown in Fig. 6.

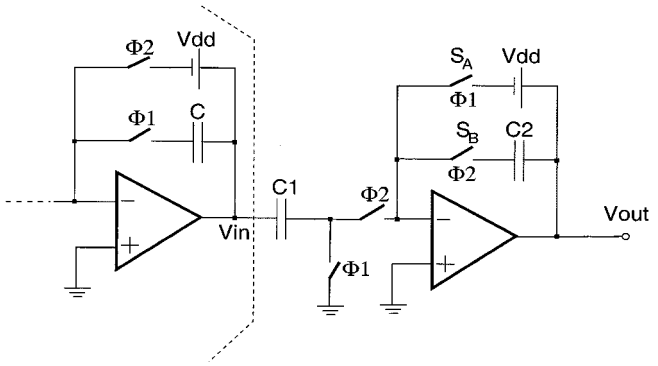

Fig. 7. Unity-gain-reset integrator.

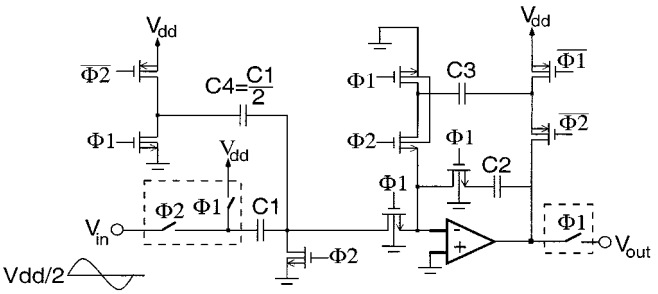

Fig. 8. Possible implementation of the floating-supply integrator.

It is based on the widely used Nakagome clock-booster stage [18]. It provides a clock signal varying between 0 and $-V_{dd}$. At powerup, the first few samples will be positive, leading to charge pumping into the well from the sources of the pMOS switches. This should not be a problem as long as the well is adequately grounded. After a few clock periods, the samples of V_1 and V_2 become negative, and the charge pumping stops.

Note that the charge pump of Fig. 6 does not introduce any voltage larger than V_{dd} on chip, and that it can be shared among all integrators.

B. Integrator Realization Using a Floating Voltage Supply

An alternative realization, which also avoids charge leakage, is shown conceptually in Fig. 7. This circuit can be implemented using only nMOS switches, since when S_A closes, the output voltage rises to the reset voltage V_{dd} (rather than dropping to 0 as in the previous realization), and hence the voltage at node B cannot fall below 0 V. Thus, the source-to-substrate junction of S_B remains reverse biased under all conditions. A more detailed circuit diagram, showing also the implementation of the floating V_{dd} source in the form of the switched capacitor $C3$, is illustrated in Fig. 8. It is also possible to implement a floating voltage source $V_{dd} - V_{\mathrm{DSAT}}$, which allows the opamp to retain a high gain during reset. This results in faster recovery.

Note that the dc bias of the input signal is assumed in Fig. 8 to be $V_{dd}/2$, and hence a compensating branch, realized by the SC branch containing $C4$, is needed to prevent the output from ramping down due to the accumulation of this input bias [14].

C. Integrator Realization Using Master–Slave Integrators

Yet another technique for avoiding charge leakage in the low-voltage integrator of Fig. 4 is to use an extra stage (a slave in-

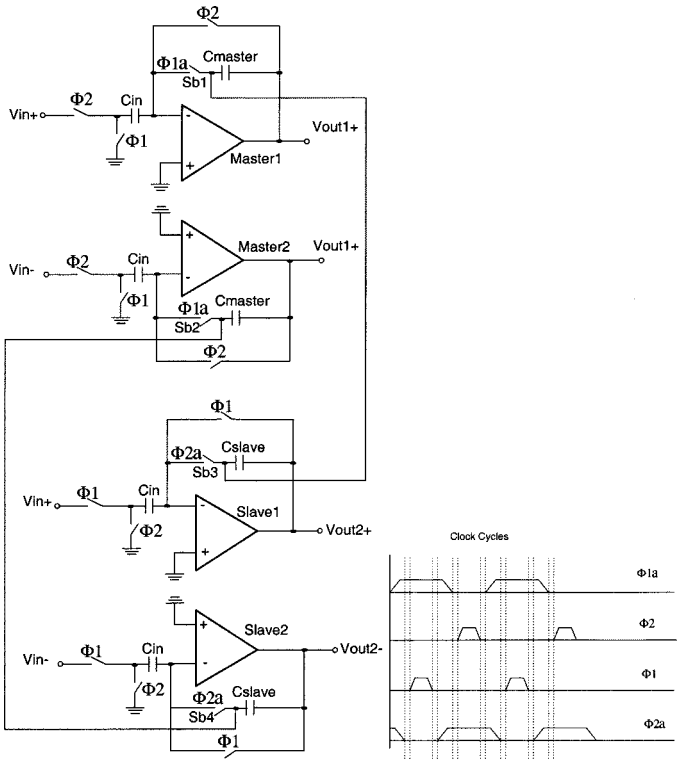

Fig. 9. Master–slave reset-opamp integrator (pseudodifferential implementation).

tegrator) for storing the charge during the reset phase when the integrating capacitor is floating. Fig. 9 shows the schematic diagram of the circuit and illustrates the clock phases. When $\Phi 2$ and $\Phi 2a$ rise, the signal charge stored in the master storage element $C_{\rm master}$ is transferred into the slave storage capacitor $C_{\rm slave}$; when clock phases $\Phi 1$ and $\Phi 1a$ rise, the charge is returned into $C_{\rm master}$. The sensitive nodes A and B are kept at or near the analog ground, and charge leakage is thereby prevented. This stage can use single-channel (nMOS) switches throughout, since all switches operate at analog ground potential. A drawback of the master–slave structure is the need for the second integrator stage. However, it is possible to operate the structure in a double-sampling mode, in which both integrators receive input charges in alternating clock periods. For such a "ping-pong" circuit, the sampling rate can be doubled without increasing the opamp bandwidth. Another drawback is that in this circuit, successive samples follow different paths. Hence, path mismatch can cause intermodulation distortion, which may be harmful in some applications, such as in $\Delta\Sigma$ modulators.

IV. Experimental Low-Voltage $\Delta\Sigma$ Modulator

To verify the effectiveness of one of the circuit techniques proposed above, a second-order delta–sigma ADC using the floating-supply integrator of Fig. 8 and a low (1-V) supply voltage was designed and fabricated. This choice of the integrator was made because it seems to be the most economical of the three circuits described above. The design issues involving a RO $\Delta\Sigma$ modulator will be discussed in the following subsections. First, the system-level design will be discussed, then

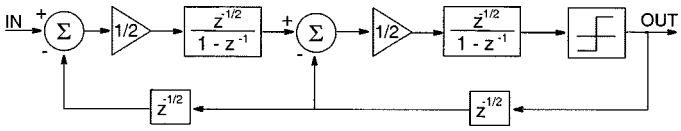

Fig. 10. Low-voltage $\Delta\Sigma$ modulator.

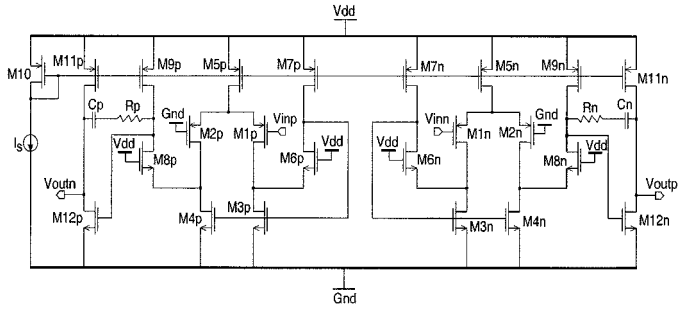

Fig. 11. Low-voltage pseudodifferential opamp.

TABLE I
Simulated Performance of the Low-Voltage Opamp

Adc	fu	PM	Tsettling	Slew Rate
68 dB	170 MHz	70°	20 ns	100 V/μs

the design of the building blocks of LV $\Delta\Sigma$, and finally, the implementation issues.

A. System-Level Design

$\Delta\Sigma$ modulators normally use integrators with a full clock period delay between input and output voltages. Since the RO technique uses half-delay integrators, an additional half-period delay is needed in each loop. These additional delays can be efficiently realized by half-delay RS flip-flops in the digital path [13]. The resulting block diagram is shown in Fig. 10.

B. Low-Voltage Opamp

The configuration chosen for the realization of the modulator is the pseudodifferential structure, which enables the efficient implementation of the common-mode feedback (CMFB) circuit [20]. The pseudodifferential opamp used is shown in Fig. 11 [22]. Each half contains a pMOS differential pair and an nMOS inverter output stage, with an *RC* compensating branch connected between them. The input stage uses a low-voltage current mirror [17]. The minimum supply voltage needed for linear operation is given by

$$V_{dd\,\min} = \max[3V_{\rm ov},\, V_{\rm th} + 2V_{\rm ov}]. \tag{1}$$

The key performance parameters of the opamp with a load of 3.5 pF are summarized in Table I.

C. Level Shifting and CMFB Circuits

A charge-domain dc level shifter is used to maintain the appropriate input and output CM voltages for the opamps. With a CM level of $V_{dd}/2$ at the opamp output, the CM at the next opamp input must be set to ground.

The SC dc level shifter and the CMFB circuit used [20] are shown in Fig. 12. The design of the CMFB circuitry is a

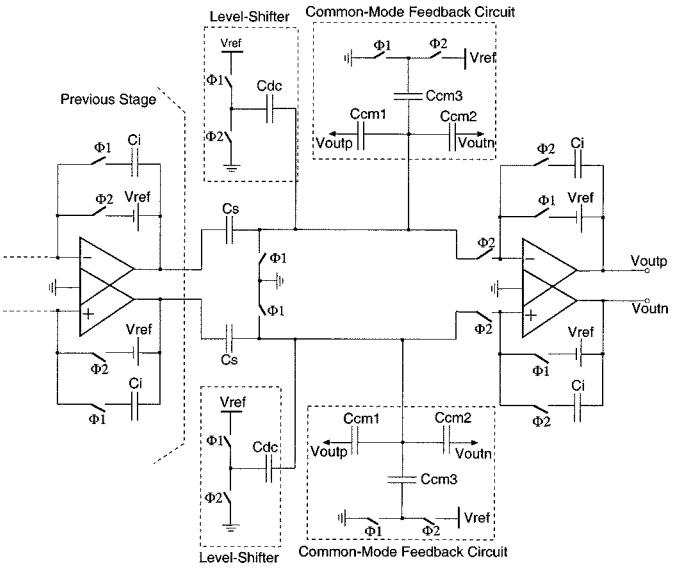

Fig. 12. Pseudodifferential integrator with CMFB.

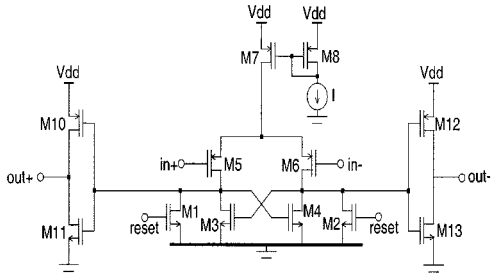

Fig. 13. Low-voltage comparator.

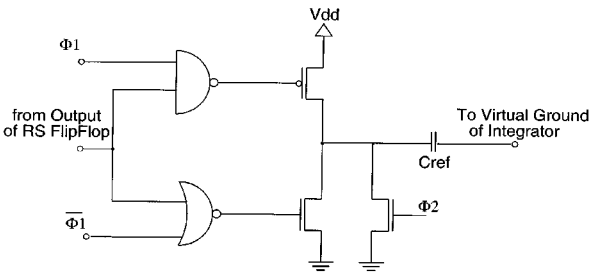

Fig. 14. Low-voltage DAC feedback branch.

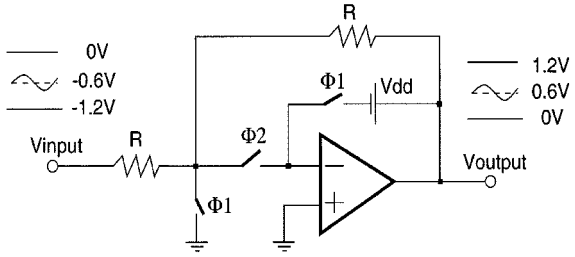

Fig. 15. Low-voltage input sampling circuit.

crucial issue in the proposed implementation, since the resetting operation is performed during one of the two alternating clock phases, and the CMFB must become active and settle within the other phase. Hence, instead of a continuous-time CMFB, a switched-capacitor CMFB was realized using a pseudodifferential structure, without serious speed limitation.

The CMFB circuitry contains capacitors $C_{\rm cm1}$, $C_{\rm cm2}$, and $C_{\rm cm3}$. During phase Φ_1, the common node of these three capacitors is pulled to ground, while the opamp outputs are set to $V_{\rm ref} = V_{dd}$. When phase Φ_2 rises, the average voltage of the opamp outputs is set to their CM value, which equals $V_{dd}/2$ if there is no common-mode offset error. Due to this shift, the capacitors $C_{\rm cm1}$ and $C_{\rm cm2}$ inject a negative charge into the virtual grounds of the opamps. The capacitor $C_{\rm cm3}$ acts to neutralize this charge. If the CM output voltage is exactly $V_{dd}/2$, the net charge injected by the three capacitors cancel. However, if there is any common-mode error accumulation at the outputs of the opamps, then charges will be injected into the input nodes of the opamps, which will correct the error.

D. Low-Voltage Comparator and DAC

The low-voltage comparator used [13] is shown in Fig. 13. It requires dc level shifters at the input terminals to set the input CM level to its desired value (ground). Reset switches are used to ground both latch outputs, since floating reset switches cannot be used in LV operation. The simulated transition time of the comparator was 12 ns.

Fig. 14 shows the circuit diagram of the DAC feedback branches [13]. All switches operate at ground or V_{dd}. The CM level of the DAC signal is corrected by the level shifter circuits at the opamp inputs.

E. Low-Voltage Input Sampling Circuit

The input branch of the first integrator poses a special problem, since its capacitor is not connected to the output of an RO. The circuit used in the modulator described in this paper is shown in Fig. 15. It is similar to the buffers described in [23], [24]. It is basically a track-and-reset (T/R) circuit used as a sampling stage. During Φ_2, it samples the input signal and provides the inverted input signal to the input capacitor of the first stage. During Φ_1, the opamp is in a unity-gain-reset configuration, providing an input voltage V_{dd} to the first integrator stage.

F. Signal-Processing Circuitry

The signal-processing circuitry of the modulator containing the stages described above (but with the CMFB circuits and input buffers omitted for clarity) is shown in Fig. 16. The element values (scaled for optimum dynamic range) are given in Table II.

G. Layout and Floor Plan

Fig. 17 shows the die photo of the prototype IC, realized in a 0.35-μm double-poly triple-metal CMOS technology. The digital and analog circuitries are well separated, with the opamps located at the maximum available distance from the digital stages. Well and substrate guard strips and rings were also used to shield the sensitive analog elements from substrate noise. By using static selector switches, it was possible to allow operation using either the input stage of Fig. 15 or a floating input transmission gate at the front end. This feature was implemented to allow operation even if the actual threshold

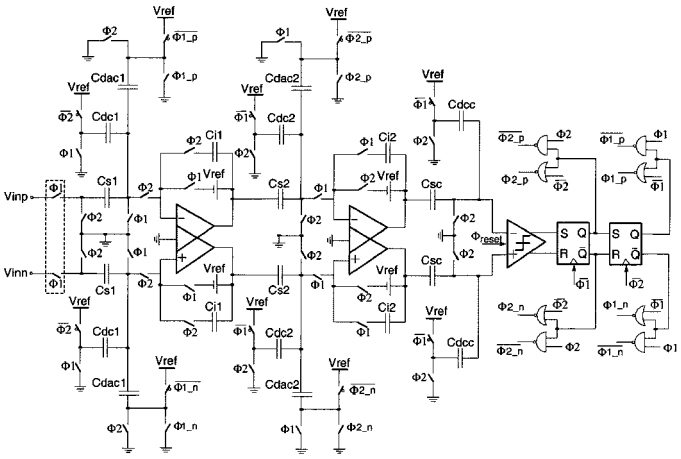

Fig. 16. Low-voltage second-order $\Delta\Sigma$ modulator.

TABLE II
CAPACITANCE VALUES

Cs1	2 pF	Cs2	0.8 pF	Csc	0.4 pF
Cdac	2 pF	Cdac2	0.4 pF	Cdcc	0.4 pF
Cdc1	1 pF	Cdc2	0.12 pf		
Ci1	8 pF	Ci2	1.6 pF		

TABLE III
MEASURED PERFORMANCE OF THE SECOND-ORDER $\Delta\Sigma$ ADC

Supply Voltage	1 V	1 V
Signal Bandwidth	20 kHz	50 kHz
Sampling Frequency	10.24 MHz	10.24 MHz
Max. Diff. Input	1.2 Vpp	1.2 Vpp
Dynamic Range	80 dB	74 dB
Peak SNR	78.6 dB	70.6 dB
Peak SNDR	77.8 dB	70.4 dB
Power Dissipation	5.6 mW	5.6 mW

voltages of the fabricated chip are different from the simulated values. The total chip area (excluding the input buffer) was 0.41 mm^2 and power consumption was 5.6 mW.

H. Test Results

The fabricated chip was tested with a 10.24-MHz clock signal and with 1-V supply voltage. Table III gives a summary of the measured results. For audio-band (0–20-kHz) operation, a true 13-bit accuracy resulted. Extending the input frequency range to 50 kHz, an equivalent number of bits (ENOB) $= 12.5$ bits was obtained. When V_{dd} was lowered, the chip remained operational down to 0.95-V supply voltage, but at an ENOB $= 10.5$ bits. The signal-to-noise+distortion ratio (SNDR) and signal-to-noise ratio (SNR) curves for a 2.5-kHz input sine wave are shown in Fig. 18. The typical measured spectrum of the digital output stream is illustrated in Fig. 19. No harmonics were detected.

In the actual chip, the MOSFET threshold voltages were found to be different from the values assumed for the simulation models. While the models assumed $V_{\rm thn} \cong |V_{\rm thp}| \cong 0.55$ V, in the chips $V_{\rm thn}$ ranged from 0.486 to 0.563 V, and $|V_{\rm thp}|$ from 0.422 to 0.486 V. In the lower-threshold chips, the floating input switch could be turned on; in the others, the input buffer had to be used. The performance did not vary significantly between the two modes of operation.

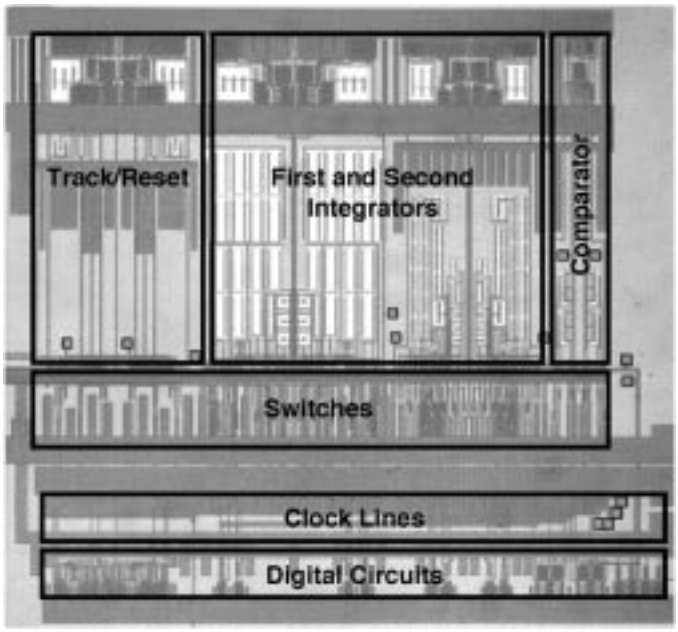

Fig. 17. Die photograph of low-voltage second-order $\Delta\Sigma$ modulator.

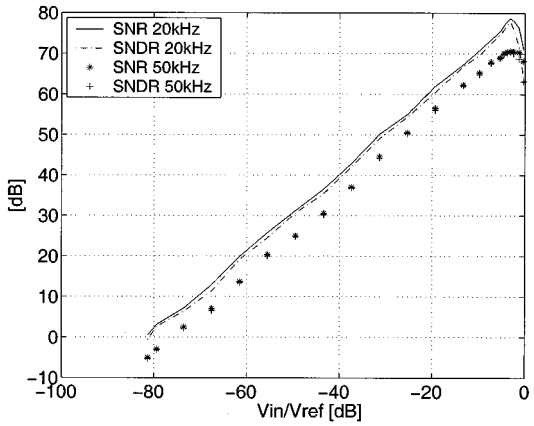

Fig. 18. SNR and SNDR for 20 and 50 kHz signal bands.

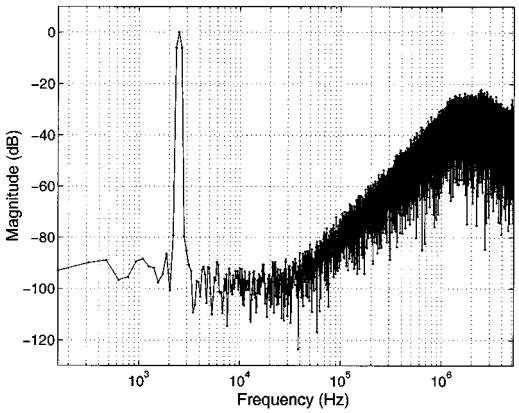

Fig. 19. Spectrum of the digital output bit stream.

V. Conclusion

Novel switched-capacitor integrators were proposed for realizing low-voltage CMOS analog circuitry. They offer potentially faster operation than existing switched opamp stages, since the amplifiers used can always operate in their linear regions. Theoretically, the sampling rate in our technique is limited only by the unity-gain bandwidth of the opamp used. A delta–sigma ADC based on the floating-supply integrator of Fig. 8 was implemented, and its test results verify that high-speed and high-accuracy operation is possible down to 1-V supply voltage.

Acknowledgment

The authors are grateful to Prof. J. Steensgaard and Prof. F. Maloberti for useful discussions, and to E. Bidari, J. Silva, L. Wu, and G. Barnes for their assistance during the design and layout of the prototype chip. They also thank AMI Semiconductor for fabricating the test chip, and the reviewers for valuable suggestions.

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