Comments and Correspondence

Comments on ""Split ADC" Architecture for Deterministic Digital Background Calibration of a 16-bit 1-MS/s ADC"

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In the above paper [1], the authors present a "split ADC" architecture that is suitable for efficient/fast background digital calibration. The use of two parallel ADCs (thus the name "split ADC") allows the input signal to be canceled by subtracting the two nominally equal output codes, thereby providing fast extraction of the calibration information. The concept and the calibration details are summarized in Figs. 2 and 5 of [1], as well as in [5]. We wish to note that the use of two parallel ADCs to cancel the input signal in the calibration process was described earlier in [2] and then demonstrated in silicon [3], [4]. The use of two parallel ADCs is summarized in Figs. 9 and 10 of [2], and also appears in Fig. 2 of [3] and Fig. 5 of [4]. Although prior papers [2] and [3] were referenced in [1], their contributions should have been more clearly stated. We acknowledge that the development of the approaches described in these papers, while similar, proceeded independently of each other and do differ in important details of implementation.

REFERENCES

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