A 0.9 V 92 dB Double-Sampled Switched-RC Delta-Sigma Audio ADC

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***Abstract*—A 0.9 V third-order double-sampled delta-sigma audio ADC is presented. A new method using a combination of a switched-RC technique and a floating switched-capacitor double-sampling configuration enabled low-voltage operation without clock boosting or bootstrapping. A three-level quantizer with simple dynamic element matching was used to improve linearity. The prototype IC implemented in a 0.13 μm CMOS process achieves 92 dB DR, 91 dB SNR and 89 dB SNDR in a 24 kHz audio signal bandwidth, while consuming 1.5 mW from a 0.9 V supply. The prototype operates from 0.65 V to 1.5 V supply with minimal performance degradation.**

***Index Terms*—Audio ADC, delta-sigma ADC, double sampling, low voltage, switched-RC.**

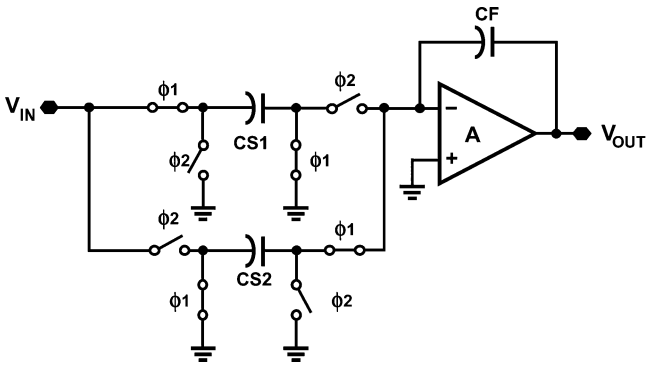

Fig. 1. Double-sampling switched-capacitor integrator circuit.

I. Introduction

THE demand for portable multimedia systems and the continued down-scaling of device dimensions resulted in rapid improvement in the performance of integrated systems. In order to reduce power consumption and the electric fields that accompany device scaling, it is necessary for circuits to operate from reduced supply voltages. Integrating both analog and digital circuits in the same process and operating with the same power supply level provides important advantages such as low cost, high performance, reduced electromagnetic interference, and portability. However, reduced supply voltage severely limits the achievable dynamic range of analog circuits. High dynamic range and low power are increasingly demanded in multimedia and communication applications. Thus, the design of analog circuits naturally comes with the challenge to maintain the desired levels of performance as the supply is lowered. A reduced supply voltage generally results in significant power savings in digital circuits. However, the power consumed in analog circuits is likely to increase because the reduced supply voltage limits the analog signal and mandates lower noise. For this reason, designing high-performance analog-to-digital converters (ADCs) that operate with a low voltage supply and low power consumption is a challenging task.

Previously proposed techniques for low-voltage circuit design [1]–[7] enabled ADCs to operate with low-voltage power supplies. However, these techniques have rarely resulted in low power consumption which is required for portable applications. Double-sampling scheme (DSS) is one possible solution for reducing power consumption. However, it requires complex bootstrapping schemes in low-voltage systems because previously proposed non-bootstrapping design techniques such as switch-opamp and opamp-reset-switching techniques [4]–[6] are applicable only to single-sampling scheme (SSS). This paper presents a high-performance audio ADC with a low-voltage DSS [8]. A fully-differential switched-RC (SRC) technique is employed in order to avoid clock bootstrapping and to overcome the issues associated with the pseudo-differential implementation in [7].

The paper is organized as follows. Conventional DSS in delta-sigma ADCs and floating switched-capacitor configuration are described in Section II. Section III presents the proposed low-voltage double-sampling technique. Section IV discusses the proposed delta-sigma ADC architecture. Section V describes the circuit implementation, followed by the description of measurement results in Section VI. Finally, conclusions are drawn in Section VII.

II. Double Sampling Technique

Double sampling techniques [9], [10], [12]–[14] can achieve twice the sampling frequency in switched-capacitor circuits without extra requirements for opamp settling time. Alternatively, the techniques allow a halving the clock frequency thereby reducing power consumption. Consequently,

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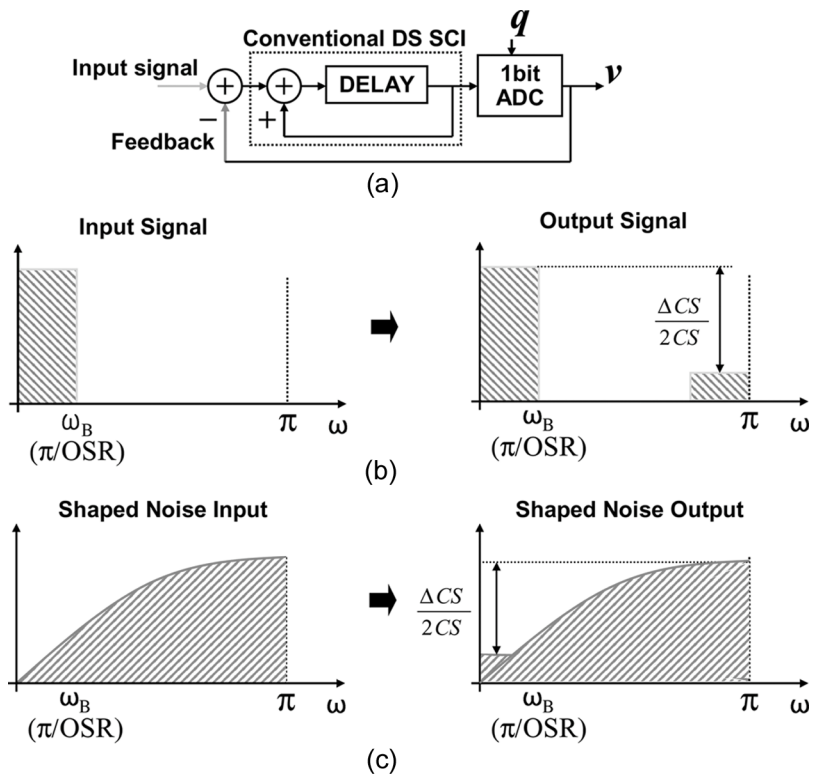

Fig. 2. Path gain mismatch effect in a double-sampled first-order delta-sigma ADC. (a) Block diagram of an input signal path. (b) Gain mismatch effect on the input signal path. (c) Gain mismatch effect on the feedback path.

double-sampling techniques can be very useful for low-power switched-capacitor circuit designs. A switched-capacitor integrator (SCI) that uses double sampling is shown in Fig. 1. During phase $\phi 1$, CS1 samples the input and CS2 transfers the charge that was sampled previously to CF. During $\phi 2$, CS1 transfers its charge to CF, and CS2 samples the input. Thus, the output is updated during both phases. The operation speed is twice as fast as the conventional single sampling integrator. However, this technique has a serious disadvantage caused by the path gain mismatch.

A. Path Gain Mismatch

If CS1 is not exactly equal to CS2, the change in the sampling capacitance from one phase to the next phase modulates the amount of the stored charge. The input-output relationship of the integrator with an ideal opamp can be written as

$$V_{\mathrm{OUT}}(n) = V_{\mathrm{OUT}}(n-1) + \frac{\overline{\mathrm{CS}}}{\mathrm{CF}} V_{\mathrm{IN}}(n-1) + \frac{(-1)^n \Delta \mathrm{CS}}{2\mathrm{CS}} V_{\mathrm{IN}}(n-1). \quad (1)$$

where $\overline{\mathrm{CS}} = (\mathrm{CS1} + \mathrm{CS2})/2$, $\Delta\mathrm{CS} = \mathrm{CS1} - \mathrm{CS2}$, and time $n = 0$ occurs when $\phi 2$ is high. The last term in (1) contains the product of the input and $(-1)^n$, which is a modulation of the input by a sampled cosine at frequency $f_S/2$. If $\mathrm{CS1} = \mathrm{CS2}$, this term is zero, and the circuit acts like an ideal discrete-time integrator. However, if $\mathrm{CS1} \neq \mathrm{CS2}$, the integrator output is the sum of the input $V_{\mathrm{IN}}(n)$ and a modulated version of the input.

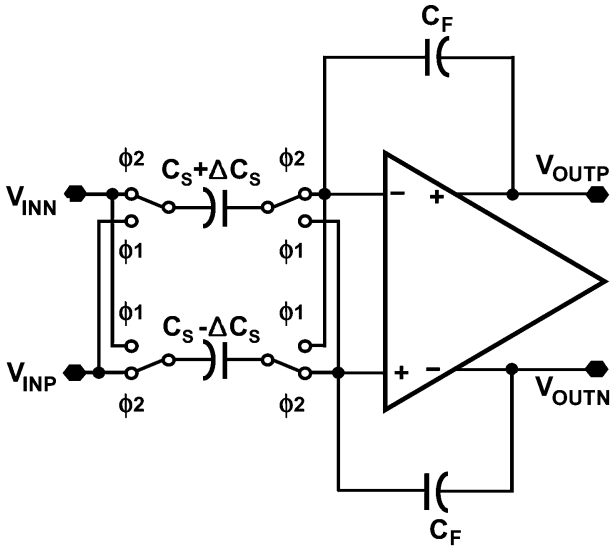

Fig. 3. Floating differential SCI.

The path gain mismatch effect is shown in Fig. 2. If the input is a low frequency signal which is band-limited by an anti-aliasing filter, the mismatch between CS1 and CS2 causes V_{IN} to be modulated to a frequency band near the half clock frequency, $f_S/2$. This effect from the input path gain mismatch is of little consequence, because the noise (modulated signal) in this high frequency band is greatly attenuated by the digital low-pass filter. However, the feedback DAC output has a large high-frequency quantization noise power as shown in Fig. 2(c). This is mixed down to the baseband due to the mismatch, which

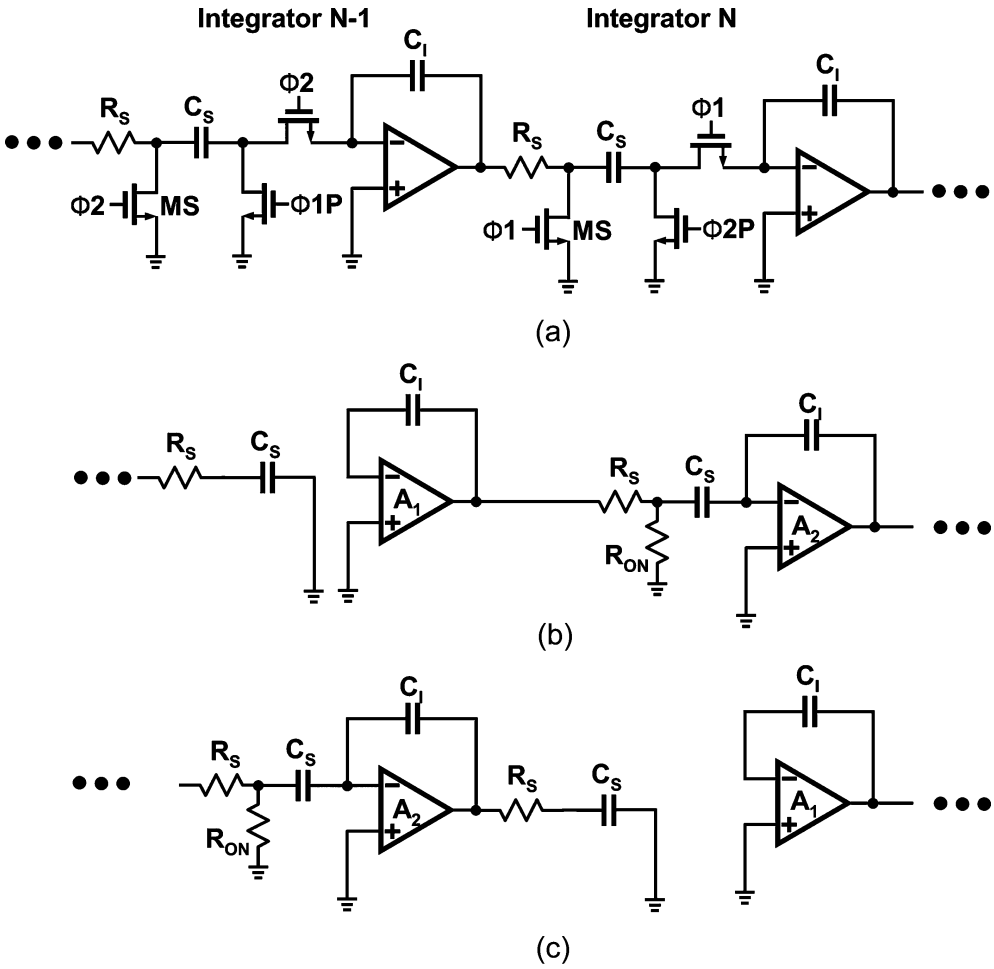

Fig. 4. (a) A single-sampling switched-RC SCI circuit. (b) $\phi 1$. (c) $\phi 2$.

increases the in-band noise power, hence decreasing the SNR drastically.

B. Floating Switched Capacitor Configuration

A modified configuration, named here the *floating switched capacitor* [14] was proposed to solve the path gain mismatch problem. As shown in Fig. 3, the SCI updates the input charge in both phases of the clock. Obviously, the effective sampling rate is twice the clock frequency. The transfer function of the fully floating SCI is given by

$$\frac{V_{\mathrm{OUT}}(z)}{V_{\mathrm{IN}}(z)} = \left(\frac{C_S}{C_F}\right)\frac{1+z^{-1}}{1-z^{-1}}. \tag{2}$$

As shown in (2), the mismatch ΔC_S does not appear, implying that the mismatch does not affect the signal processed by the integrators. On the other hand, the transfer function differs from that of a conventional SCI. The additional factor $1 + z^{-1}$ is included now in the transfer function. The zero at $F_S/2$ reduces the high frequency quantization noise and further alleviates noise folding.

III. Low-Voltage Double Sampling Technique

The double-sampling technique can be applied to many of the low-voltage design techniques. Clock boosting or bootstrapping [2], [3] can make the double-sampling technique applicable for low-voltage designs. However, they suffer from extra circuit complexity associated with bootstrapped clock driver. Switched Opamp [4] and Opamp Reset Switching [5], [6] techniques are not compatible with double-sampling technique, because the active component (opamp) has to work during both phases. On the other hand the switched-RC technique [7] can provide many advantages if it is used in a low-voltage double-sampling design. First, the switched-RC branch provides highly linear sampling because the passive element R is very linear and constant over all input voltage unlike the conventional floating switch. Second, the double-sampling technique can be applied without the need for clock boosting or bootstrapping. Finally, the double-sampling switched-RC circuit overcomes the drawbacks inherent in the original form of the switched-RC technique. In summary, the advantages of double-sampling switched-RC technique are as follows.

- The double-sampling switched-RC technique provides a constant input impedance, that of the SCI, because the previous stage output load condition is kept the same during both phases.
- The opamp DC gain and the feedback factor in an integrator circuit are the same during both phases, because the opamp output load condition and closed loop conditions are the same.

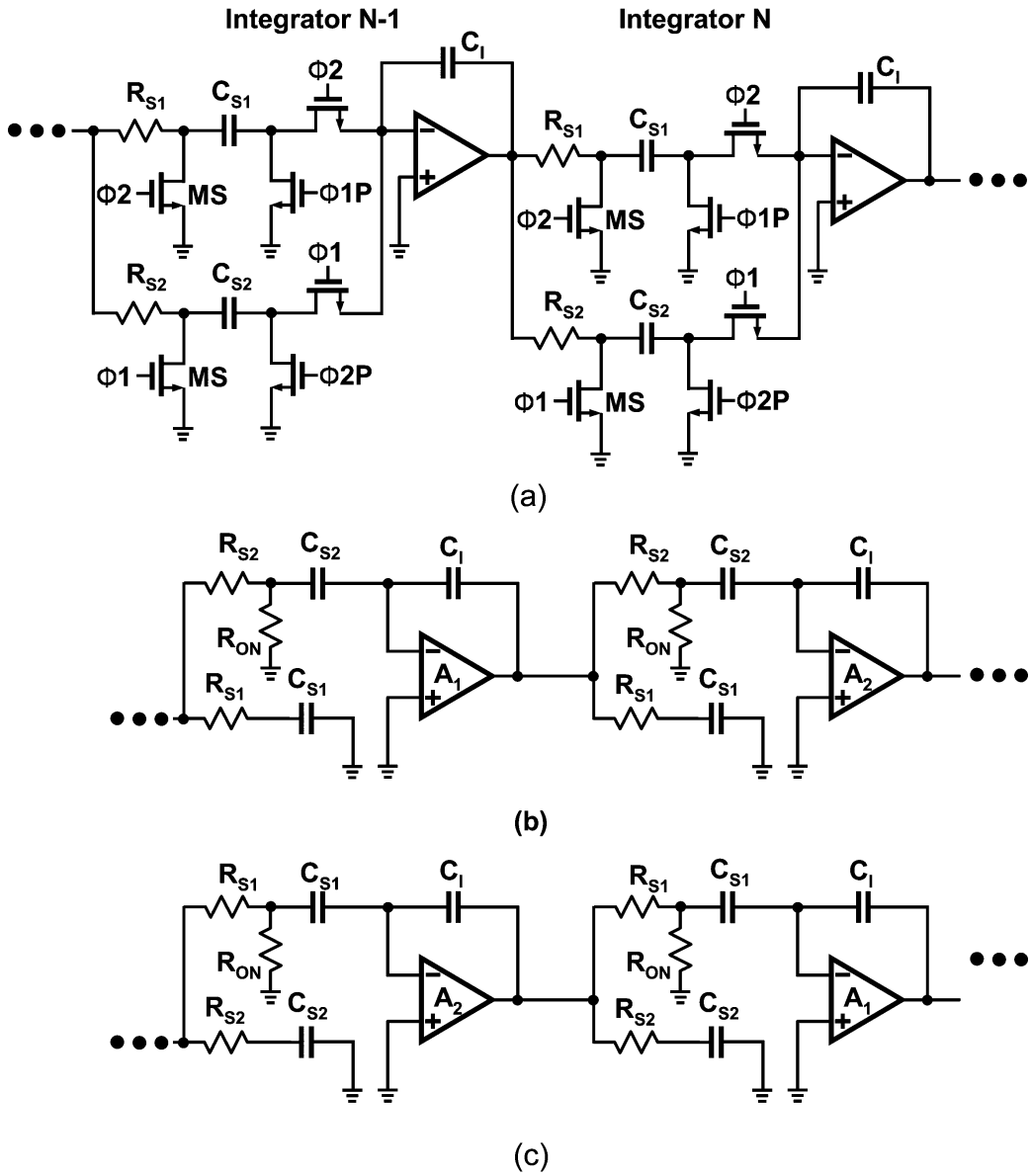

Fig. 5. (a) A double-sampling switched-RC SCI circuit. (b) $\phi 1$. (c) $\phi 2$.

- The double-sampling switched-RC circuit is less sensitive to gain error effect than the single sampling scheme.

In order to illustrate this, consider the single-sampled switched-RC integrator shown in Fig. 4. The output voltage of this integrator can be written as

$$V_{\mathrm{OUT}}(z)\cdot z^{-\frac{1}{2}} = V_{\mathrm{OUT}}(z) + \frac{C_S}{C_I}\cdot V_{\mathrm{IN}}(z)\cdot(1-\alpha) + \frac{C_S}{C_I}\cdot\alpha\cdot V_{\mathrm{IN}}(z)\cdot\left(1-z^{-\frac{1}{2}}\right) \quad (3)$$

where the gain error factor is

$$\alpha = \frac{R_{\mathrm{ON}}}{R_S + R_{\mathrm{ON}}} \quad (4)$$

and R_{ON} is the on-resistance of the MS switch.

The output voltage of the integrator in (3) has two non-ideal terms. The gain reduction factor α in the second term does not affect the overall linearity of the delta-sigma loop if R_{ON} is very small and linear. Second, the first-order shaped input in the third term is added to the input. The third term in (3) can be expressed as follows:

$$\begin{aligned} V_{\mathrm{IN}(N)}(z)\cdot\left(1-z^{-\frac{1}{2}}\right) &= V_{\mathrm{OUT}(N-1)}(z)\cdot\left(1-z^{-\frac{1}{2}}\right) \\ &= \left(\frac{A_2}{A_2+1}-\frac{A_1}{A_1+1}\right)\cdot V_{\mathrm{CI}} \\ &\cong \frac{1}{A_1}\cdot V_{\mathrm{OUT}(N-1)}(z) \end{aligned} \quad (5)$$

where $V_{\mathrm{IN}(N)}$ and $V_{\mathrm{OUT}(N)}$ are the input and output signals of the Nth stage integrator, A_1 and A_2 are the amplifier DC gains in the two clock phases $\phi 1$ and $\phi 2$, and V_{CI} is the voltage across the feedback capacitor CI of $N-1$th stage integrator.

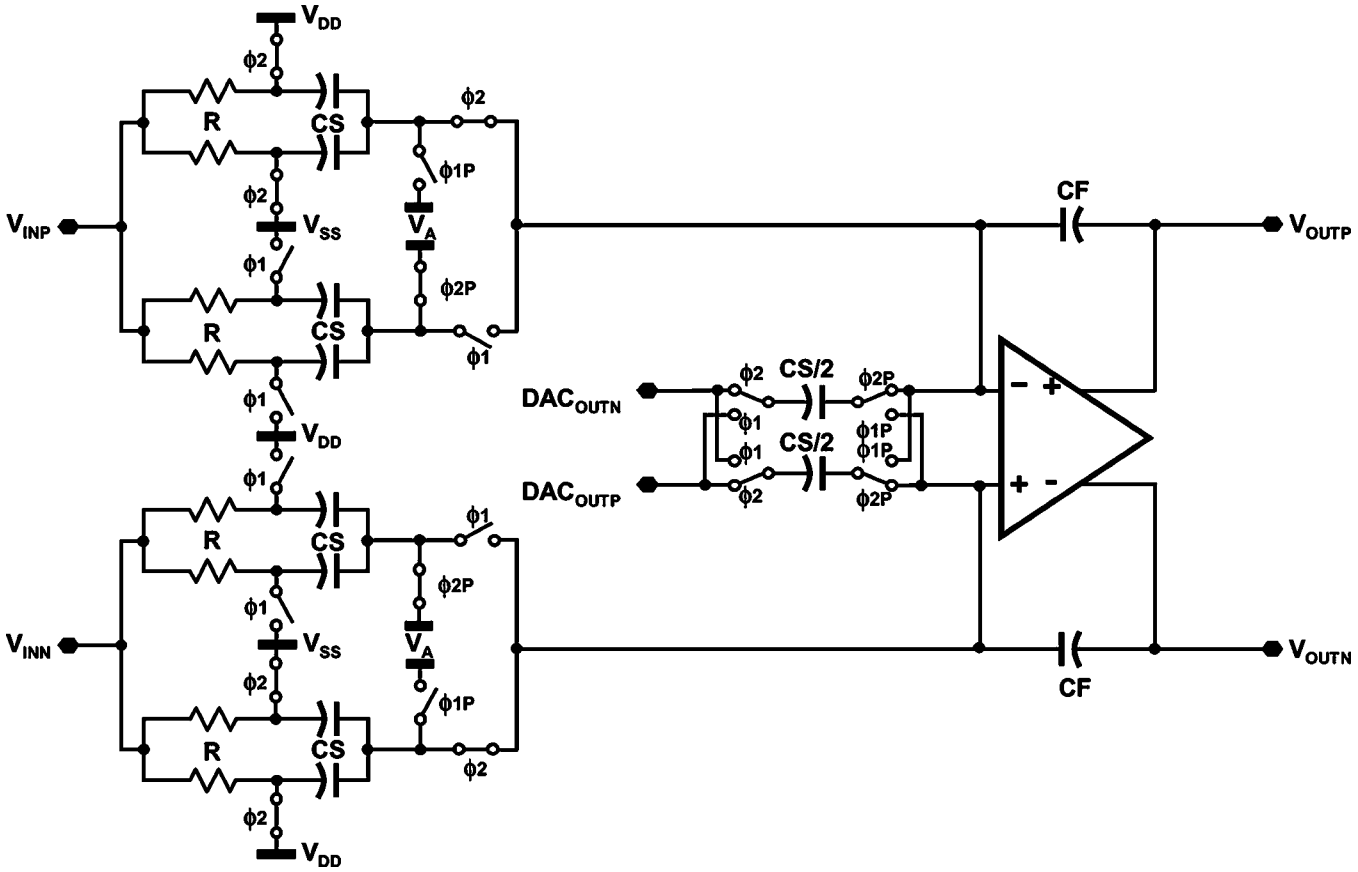

Fig. 6. Proposed fully differential low-voltage double-sampling integrator.

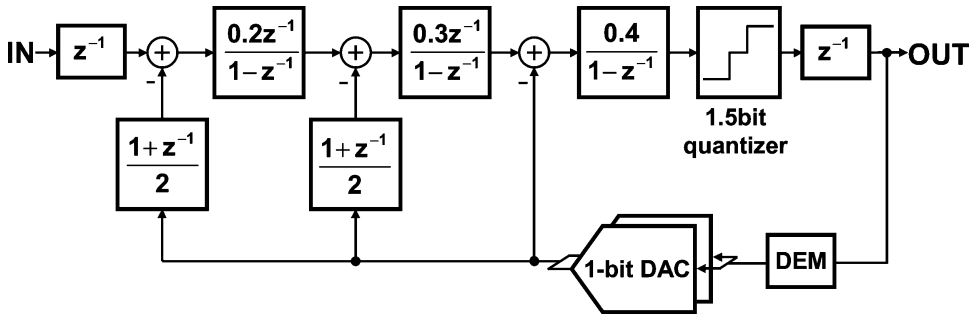

Fig. 7. Third-order DS delta-sigma ADC topology.

Operational amplifiers are widely used for SCI implementation. The amplifier DC gains A_1 and A_2 of single-sampling SCIs are not the same in the two clock phases. In the circuit of Fig. 4, the resistor R_S in switched-RC sampling network is an additional load during $\phi 1$, and this will result in a much lower DC gain A_1 than A_2. The difference between A_1 and A_2 is significant if the output resistance of typical operational amplifier is in the range from 50 kΩ to 100 kΩ, and the resistance value in switched-RC branch for audio speed operation is in the range from 5 kΩ to 10 kΩ. Even if a delta-sigma ADC has sufficiently high oversampling ratio (OSR), the third term is not properly cancelled for the reason explained above. The integrators are driven by the previous stages which have also different amplifier DC gains during the two clock phases. That will add the input referred DC offset and a nonlinear factor, because the amplifier gain A_1 in $\phi 1$ is a function of amplifier output voltage level. However, the additional first-order-shaped term in the proposed DSS, as shown in Fig. 5, can be cancelled with sufficiently high OSR because the gains A_1 and A_2 will be almost same. The gain mismatch between the two clock phases in a DSS is only affected by the resistor mismatch, which can be made small. According to SPICE simulation results of SCIs in this design, the THD of integrator output in SSS SCI and DSS SCI were -81.9 dB and -107.0 dB. The linearity of DSS is much better preserved despite the resistive loading imposed by the switched-RC method because a fixed load is maintained over both phases (unlike SSS switched-RC).

The fully differential SCI circuit with the proposed low-voltage double-sampling technique is shown in Fig. 6. A split switched-RC input branch [7] is used to keep the

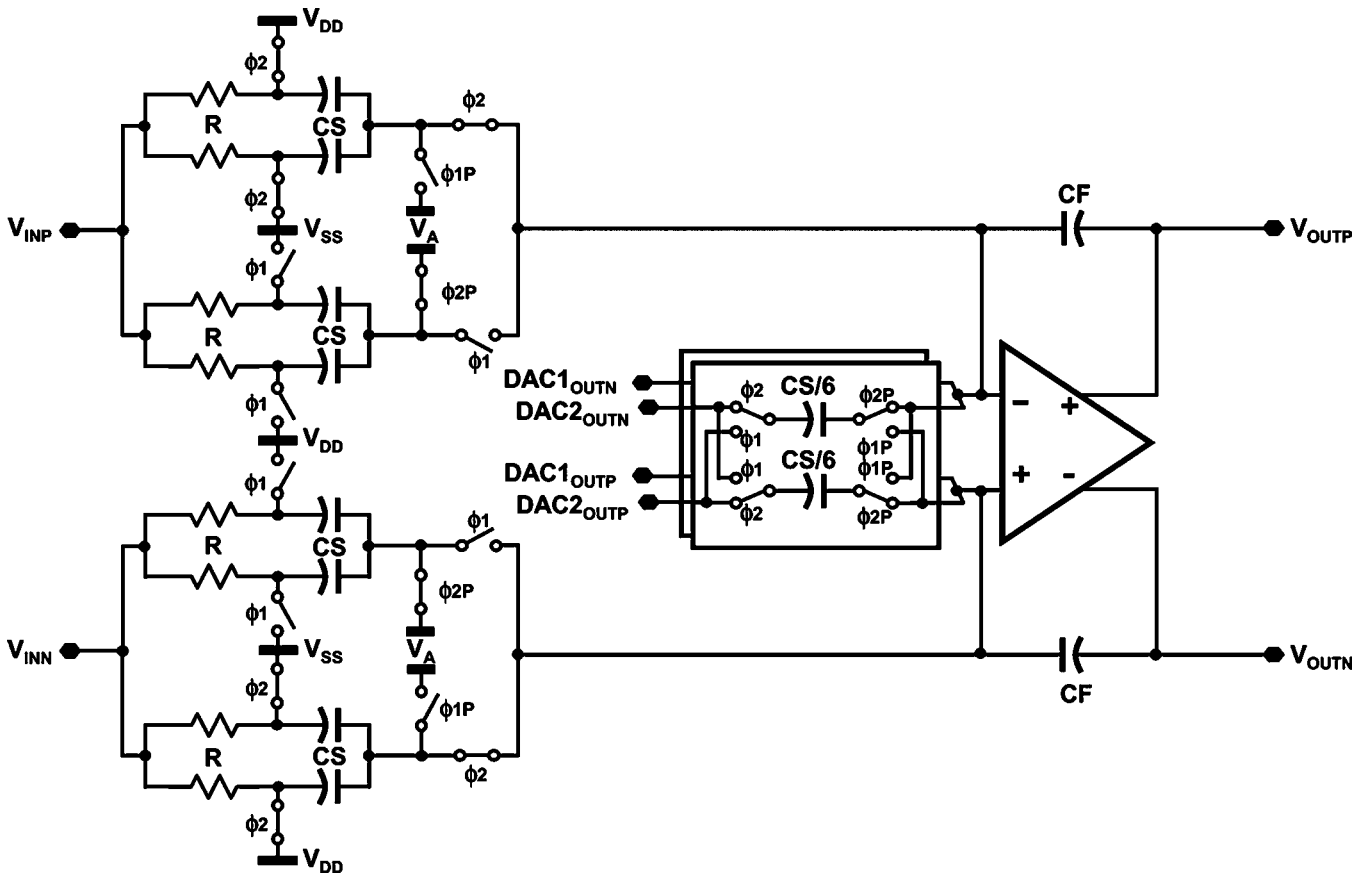

Fig. 8. Proposed low-voltage DS integrator.

common mode level of the integrator constant. During the integrating phase, half of the sampling capacitor is connected to $V_{\rm DD}$, while the other half is connected to $V_{\rm SS}$. This results in a constant common-mode level of half $V_{\rm DD}$ for the integrator during both phases, avoiding any need for additional level-shifting circuits.

IV. Proposed Architecture

A. Topology Selection

The proposed low-voltage double-sampling technique combined with switched-RC supports highly linear sampling without floating switch problems. A high-performance low-voltage double sampled audio $\Delta\Sigma$ ADC was designed with the proposed technique. The theoretical signal-to-noise ratio (SQNR) is given by

$$\mathrm{SQNR}_{\mathrm{MAX}} = 6.02N + 1.76 + (20L + 10)log_{10}\mathrm{OSR} - 10log_{10}\frac{\pi^{2L}}{2L+1} \quad (6)$$

where L is the order of a delta-sigma modulator, and N is the number of quantizer bit resolution. The maximum SQNR equation is based on many assumptions including no quantization noise overload, white noise over all input range of quantizer, no DAC mismatches, ideally shaped noise transfer function, infinite amplifier gain, etc. By contrast, the practical simulation results include all possible non-idealities. Thus, the actual SQNR ends up being much lower than the theoretical maximum SQNR. Single-loop delta-sigma topology offers several advantages for low-power, low-voltage operation, such as circuit simplicity and insensitivity to non-ideal circuits. However, this topology requires a higher order for a given oversampling ratio (OSR) to achieve high SQNR. System-level simulations indicate that a third-order 1.5-bit (three-level) single-loop topology with double sampling offers one of the best tradeoffs between the required clock frequency, amplifier bandwidth, and signal-to-noise ratio (SNR) for the target audio ADC. The block diagram of the single-loop third-order delta-sigma ADC with a 1.5-bit quantizer is shown in Fig. 7. The loop coefficients are determined from behavioral simulations and are set to [0.2, 0.3, 0.4]. The modulator with these coefficients is very tolerant to coefficient mismatches caused by capacitance mismatches and the inherent gain error of the switched-RC technique.

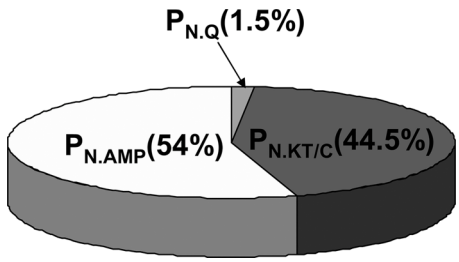

Fig. 9. Noise distribution of the delta-sigma ADC.

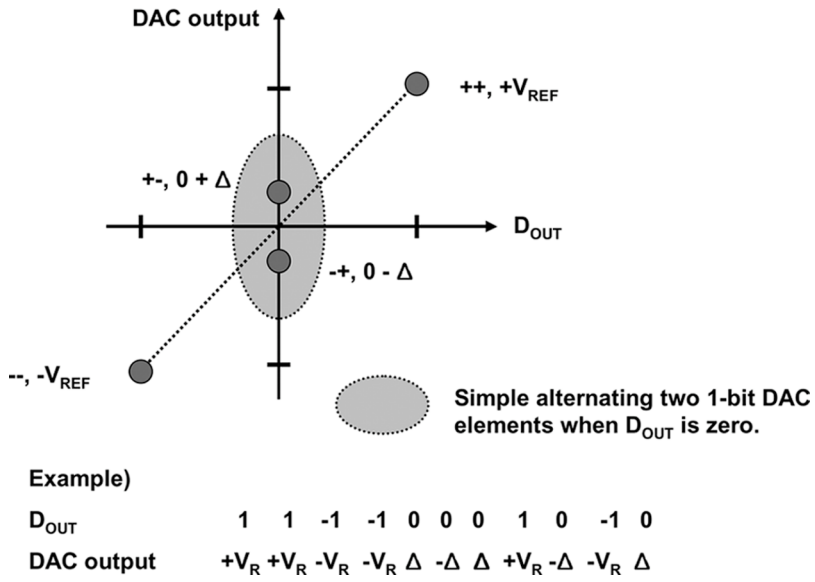

Fig. 10. Low-power DEM for three-level DAC.

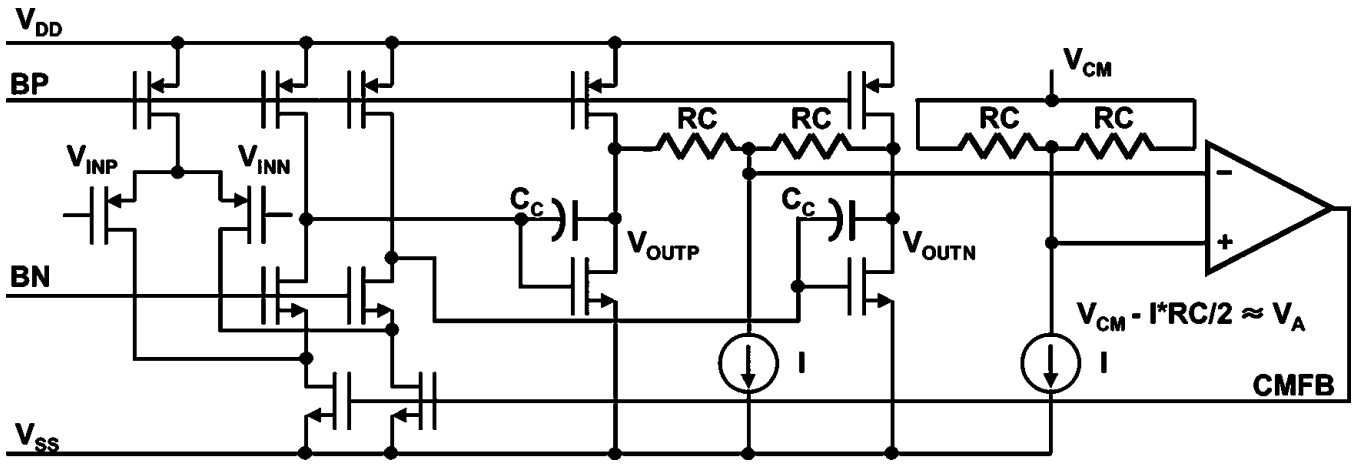

Fig. 11. Opamp with the proposed low-voltage CMFB.

One major disadvantage of the conventional double sampling is noise folding due to path gain mismatch. The path gain mismatch in the forward signal path does not degrade performance significantly. However, in the feedback path, it degrades the SNR due to noise folding into the signal band. The integrator circuit used in this design is shown in Fig. 8. Double sampling switched-RC branches are employed in the forward signal path, while fully-floating switched-capacitor branches that are insensitive to gain mismatch are utilized in both the first and second feedback paths [14]. The delta-sigma ADC full scale input range is 1.1 Vpp differential for 0.825 V or higher supply voltage level. The differential reference voltages are up-scaled to 1.65 Vpp ($V_{\mathrm{REFP}} = V_{\mathrm{DD}}/2 + 0.4125\ \mathrm{V}$, $V_{\mathrm{REFN}} = V_{\mathrm{DD}}/2 - 0.4125\ \mathrm{V}$) by a factor of 1.5. For 0.825 V and lower supply voltage, the reference voltages, V_{REFP} and V_{REFN} are same as the supply voltage and ground. The up-scaled reference voltage results in reduced size of feedback DAC path capacitors. This results in two advantages: reduced input referred noise from the feedback DAC side and better floating switch operations. Conventional double sampling is used in the third integrator feedback path, because the use of conventional DSS eliminates the stability issues caused by the additional pole introduced by the fully-floating switched-capacitor configuration. Even though the required SNR is 90 dB, the simulated peak SQNR is 110 dB for this topology. It is necessary to minimize the quantization noise contribution in order to leave some margin for other less predictable noise sources such as flicker, kT/C, and amplifier thermal noises.

B. Noise Budgeting

Many performance metrics of data converters such as SNR, SNDR, and dynamic range (DR) are related to power. Once the maximum signal power was estimated in system level simulation by deciding the reference voltage level, the allowed total noise power can be calculated based on the desired DR. The total noise power can be expressed as

$$P_{\mathrm{Ntotal}} = P_{\mathrm{NQ}} + P_{\mathrm{NAMP}} + P_{\mathrm{N}kT/C} \tag{7}$$

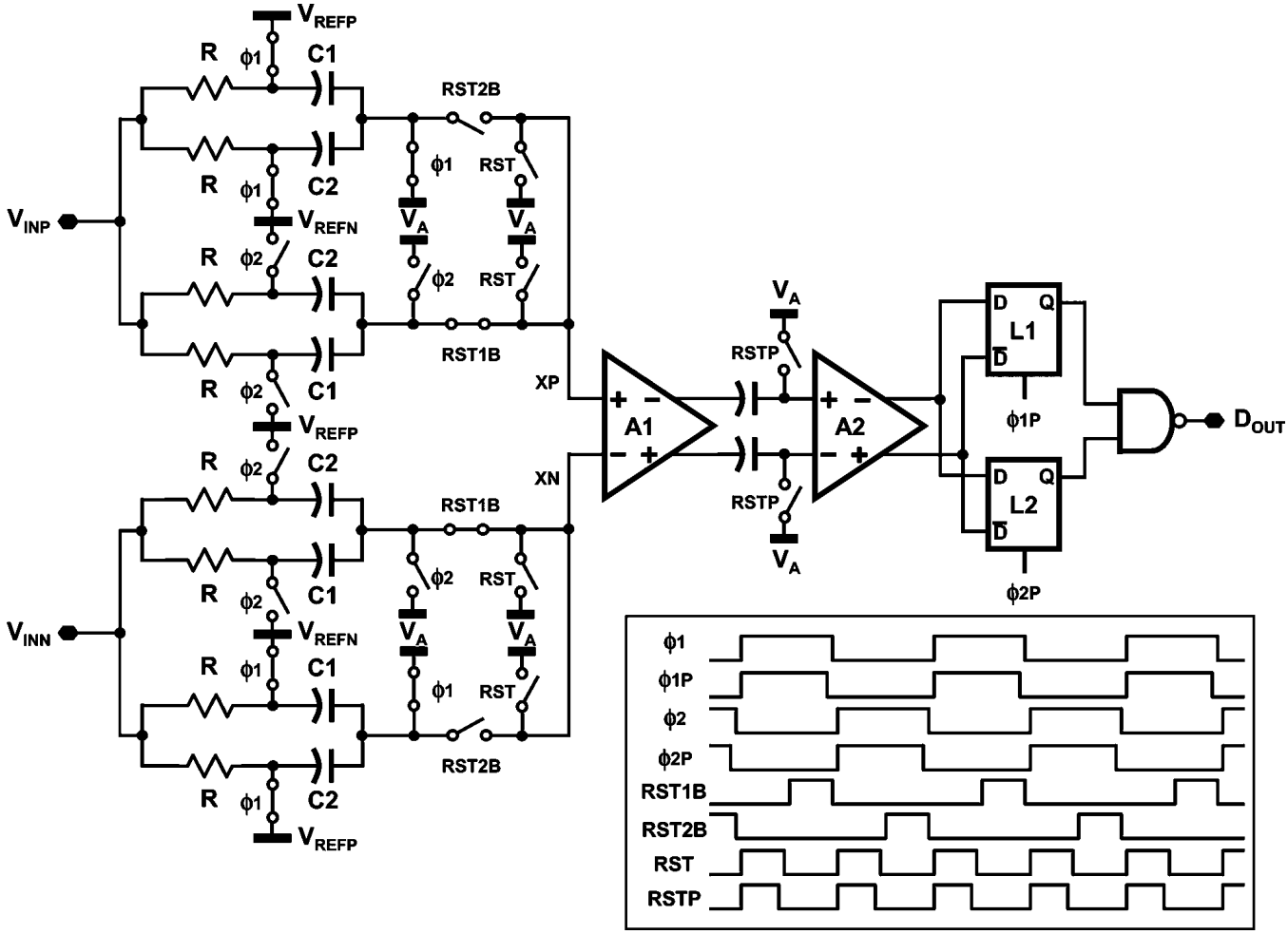

Fig. 12. Proposed low-voltage comparator.

where P_{Ntotal} is the total in-band noise power, P_{NQ} is the in-band quantization noise power, P_{NAMP} is the in-band amplifier noise power, and $P_{\mathrm{N}kT/C}$ is the in-band kT/C noise power. The noise power from DAC reference is ignored, because that can be easily suppressed in audio applications. As described in the previous subsection, the quantization noise is already small enough to be ignored. So, the dynamic range can be written as

$$\mathrm{DR} = \frac{P_{\mathrm{INMAX}}}{P_{\mathrm{Ntotal}}} \cong \frac{V_{\mathrm{INMAX}}^2}{2} \frac{1}{(P_{\mathrm{NAMP}} + P_{\mathrm{N}kT/C})} \cong \frac{V_{\mathrm{INMAX}}^2}{2\,(P_{\mathrm{NAMP}} + 2kT/(C_S \cdot \mathrm{OSR}))} \tag{8}$$

where V_{INMAX} is the maximum input amplitude of the ADC, and C_S is the sampling capacitance of the first integrator. The kT/C noise is easily controlled by sizing the capacitors in the integrators. The sampling capacitance of the first integrator is 6 pF which was decided after minimizing the amplifiers noise. The amplifier's noise has two major sources, thermal noise and flicker noise. The flicker noise in a low-pass delta-sigma modulator is very critical because it is dominant at low frequencies. Several techniques to reduce or cancel this low-frequency flicker noise exist, such as correlated double sampling and chopper stabilization techniques. However, these techniques require hard-to-implement low-voltage switched-capacitor circuitry. For this reason, the prototype avoided using flicker noise suppression techniques by simply increasing the geometric sizes of those transistors which are the main sources of the $1/f$ noise. Then, the thermal noise is the only dominant source of amplifier noise. The final noise distribution is shown in

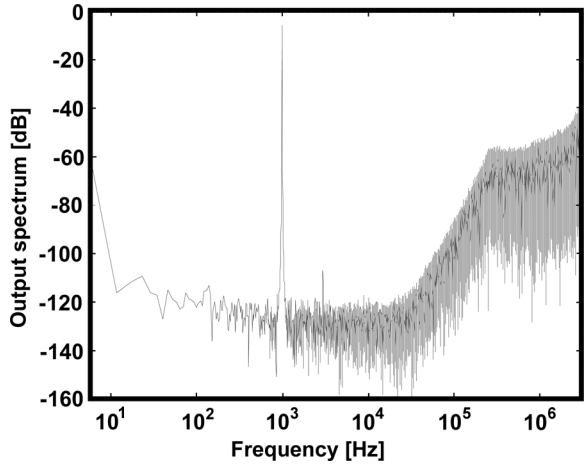

Fig. 13. Measured output spectrum.

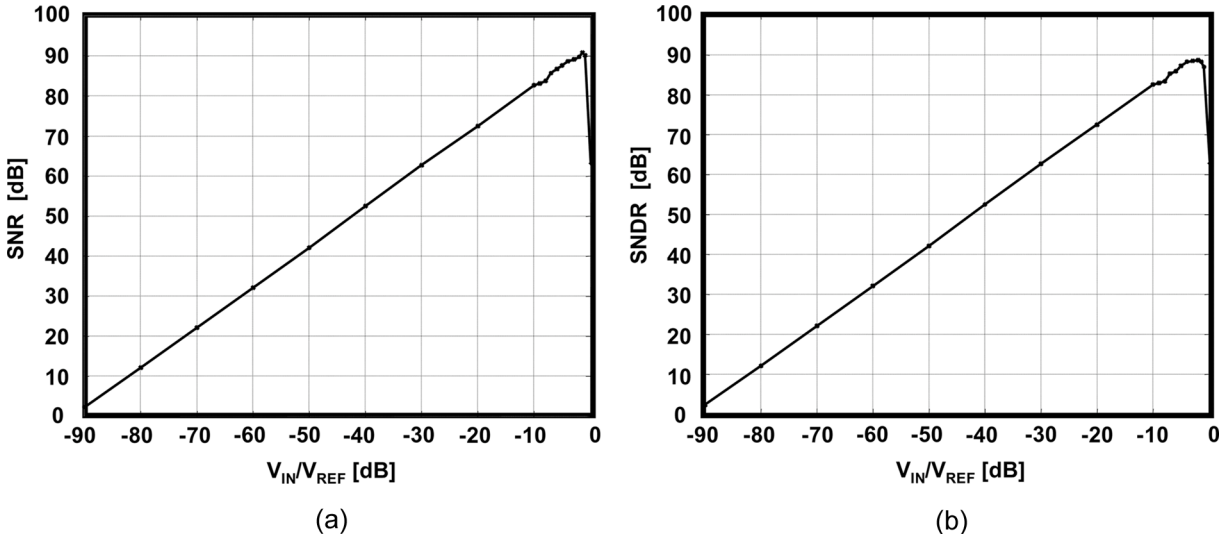

Fig. 14. (a) SNR versus input level. (b) SNDR versus input level for a 0.9 V supply voltage.

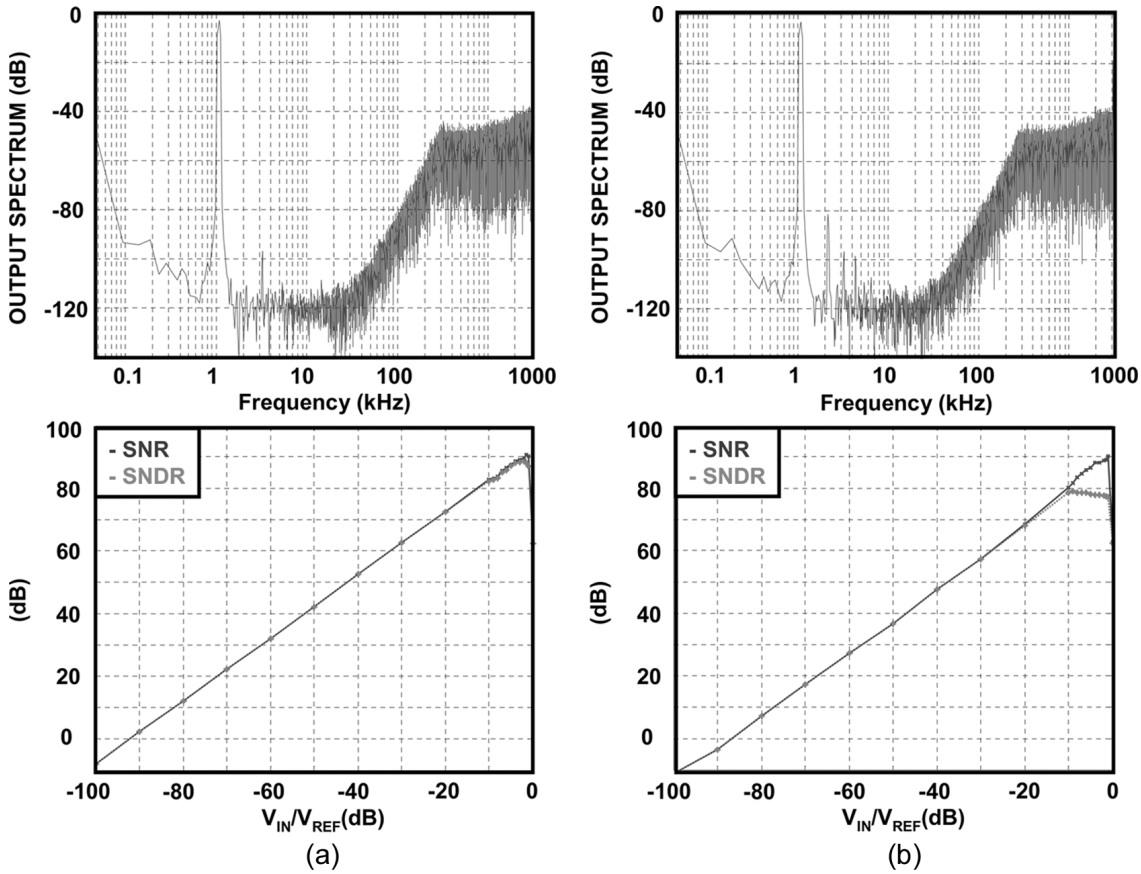

Fig. 15. Output spectra and SNR/SNDR versus input level plots (a) with DEM and (b) without DEM.

Fig. 9. The power consumption of the first integrator amplifier is 0.9 mW which is 60% of total power consumption.

C. Simple Dynamic Element Matching Scheme for Three-Level Quantizer

According to (6), using a three-level (1.5-bit) quantizer and a three-level DAC can easily improve SQNR by 3 dB, and more importantly improves the stability of the loop. However, once the number of the DAC levels is more than two, the DAC is no longer intrinsically linear. The nonlinear three-level DAC causes even harmonics of the DSM output in the frequency domain, unless dynamic element matching (DEM) is used, which implies extra hardware cost. However, the three-level DAC allows the use of a simple DEM scheme suitable for low-voltage operation. In this scheme, the two 1-bit DAC elements are interchanged whenever the delta-sigma ADC output

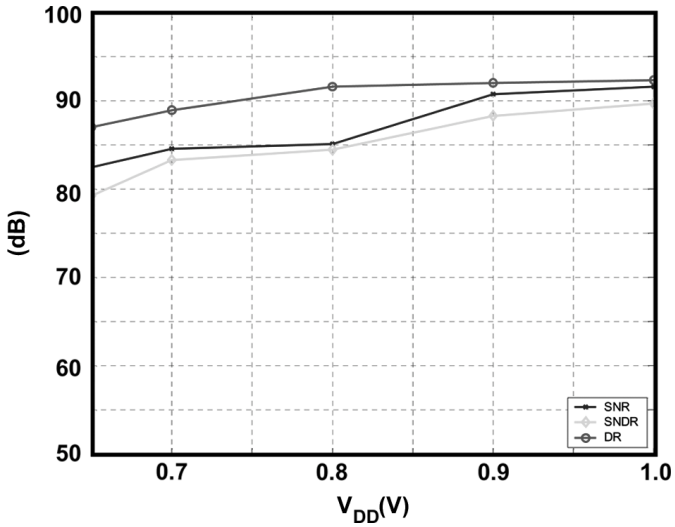

Fig. 16. SNR, SNDR, and DR versus $V_{\rm DD}$ plot.

equals the middle code as depicted in Fig. 10. The behavioral simulation result indicates that the proposed DEM achieves almost the same performance as that of a perfectly linear DAC.

V. Circuit Implementation

A. Low-Voltage Fully-Differential Opamp

Pseudo-differential opamps are frequently used in low-voltage applications to overcome the difficulty with realizing the low-voltage common-mode feedback (CMFB) required for a fully-differential structure. However, the pseudo-differential configuration suffers from several drawbacks, including increased noise, higher power consumption, larger area, and reduced PSRR/CMRR. In order to avoid these issues, a fully-differential amplifier with a low-voltage CMFB was employed. The amplifier consists of a folded-cascode first stage for low input common-mode voltage, and a common-source second stage for wide output swing. As shown in Fig. 11, an additional current source is used to shift the output common-mode level from $V_{\rm CM} = V_{\rm DD}/2$ to within the input common-mode range of the folded-cascode single-stage CMFB amp which is similar in [11].

B. Low-Voltage Comparator Design

Fig. 12 illustrates the circuit diagram of the low-voltage double-sampled comparator used in the 1.5-bit quantizer. It consists of a split switched-RC input sampling network, a preamplifier A1 and a level-shifting amplifier A2 along with the two comparator latches L1 and L2. The decision levels are set by appropriately scaling capacitors C1 and C2, and the offset is cancelled at the output of the preamplifier A1. The input common-mode level of A2 can be set as low as ground potential. This comparator can be used to realize a low-voltage multi-level quantizer without needing floating switches. Unlike the existing low-voltage comparator design in [7], the proposed comparator can save passive components, make the circuit simpler and less noisy by removing the summing node and the additional branch for reference voltage level injection.

TABLE I
Measured Performance Summary of the Audio Delta-Sigma ADC

Power supply voltage	0.65 V	0.9 V
Power consumption	1.1 mW	1.5 mW
Input range	0.87 V_{PP} (diff.)	1.1 V_{PP} (diff.)
Peak SNR	83 dB	91 dB
Peak SNDR	79 dB	89 dB
Dynamic range	87 dB	92 dB
Signal bandwidth	24 kHz	
Sampling frequency	6.144 MHz	
Clock frequency	3.072 MHz	
Oversampling ratio	128	
Active die area	1.6 X 0.9 mm^2	
Technology	0.13μm CMOS	

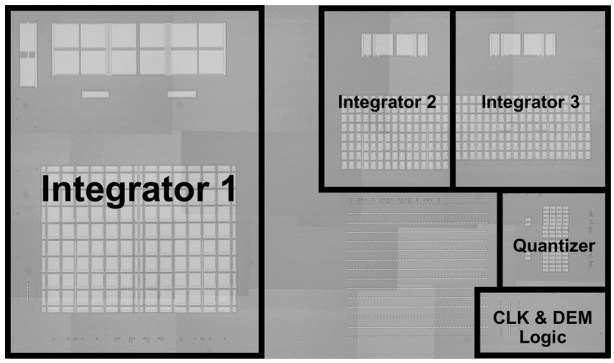

Fig. 17. Chip photograph of the delta-sigma audio ADC.

TABLE II
Performance Comparison

	V_{DD} [V]	DR [dB]	BW [kHz]	Power [μW]	CMOS [μm]	FOM [dB]
Keskin [5]	1	80	20	5600	0.35	116.3
Ahn [7]	0.6	82	24	1000	0.35	125.8
Pun [15]	0.5	74	25	300	0.18	123.2
Peluso[16]	0.9	77	16	40	0.5	133.0
Yao[17]	1	88	20	130	0.18	139.9
This work	0.9	92	24	1500	0.13	137.0

VI. Measurement Results

The ADC was fabricated in a 0.13 μm CMOS technology. The measured output spectrum with a -6 dBFS 1 kHz sinusoidal input signal and a 0.9 V supply voltage is shown in Fig. 13. The measured SNR and SNDR versus input signal level characteristics are shown in Fig. 14. Fig. 15 verifies that the proposed DEM results in improved output linearity. The ADC can operate with supply voltages in the range of 0.65 V to 1.5 V with minimal performance degradation, as depicted in Fig. 16. The measured performance summary is presented in Table I. This prototype achieves 91 dB SNR, 89 dB SNDR, and 92 dB dynamic range with a 0.9 V supply voltage. With a 0.65 V supply, 83 dB SNR, 79 dB SNDR, and 87 dB dynamic range were measured. The chip micrograph is shown in Fig. 17. The active die area is 1.6×0.9 mm^2. Table II compares the proposed delta-sigma ADC with previously reported sub-1-V

delta-sigma ADCs [5], [7], [15]–[17]. The figure of merit (FOM) in the table is defined as

$$\mathrm{FOM} = \mathrm{DR}_{\mathrm{dB}} + 10log_{10}\frac{\mathrm{BW}}{P} \tag{9}$$

where DR, P, and BW are dynamic range, power, and bandwidth, respectively. Compared to other sub-1-V audio ADCs, the proposed ADC achieves the highest DR while maintaining good FOM.

VII. Conclusion

A low-voltage $\Delta\Sigma$ ADC using double-sampling switched-RC branches was realized. The low-voltage double-sampling technique doubles the OSR as compared to conventional design, without extra power consumption and without increasing the clock frequency. Thus, this technique allows power reduction for achieving a given performance. A prototype 0.9 V 92 dB delta-sigma audio ADC was implemented in a 0.13 μm CMOS process to prove the validity of the proposed technique. The measured results verify the effectiveness of the proposed technique to achieve low-voltage, low-power, and high-accuracy performance. The prototype IC includes opamps with a low-voltage CMFB circuits, a novel low-voltage quantizer circuit, and a low-power DEM for three-level quantizer.

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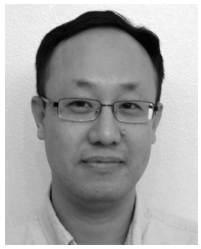

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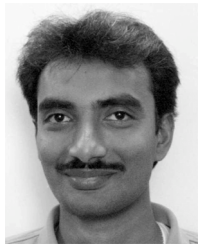

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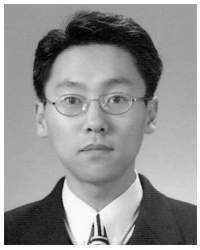

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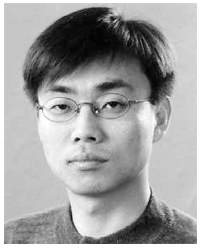

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