A CMOS Self-Calibrating Frequency Synthesizer

William B. Wilson, *Member, IEEE*, Un-Ku Moon, *Senior Member, IEEE*, Kadaba R. Lakshmikumar, *Member, IEEE*, and Liang Dai, *Student Member, IEEE*

***Abstract*—A programmable phase-locked-loop (PLL)-based frequency synthesizer, capable of automatically adjusting the nominal center frequency of the voltage-controlled oscillator (VCO) to an optimum value is described. In fully integrated PLLs, the VCO output frequency should be tunable over a wide range of frequencies, covering the desired range of the synthesizer output frequencies, for all processing variations and operating conditions. A wide tuning range realized by making the VCO gain K_o large has the unwanted effect of increasing the phase noise at the output of the VCO, and hence the PLL as well. In this work, the wide tuning range is realized by digital control, with process variability managed through self-calibration. The PLL is only required to pull the oscillator output frequency to account for the digital quantization, temperature variations, and some margin. This allows the K_o to be small, with better noise performance resulting. The prototype self-calibrating frequency synthesizer, capable of operating from 80 MHz to 1 GHz, demonstrates a measured absolute jitter of 20-ps rms at 480-MHz operating frequency. The prototype IC is fabricated in a 0.35-μm 3-V digital CMOS process.**

***Index Terms*—Frequency synthesizer, low jitter, phase-locked loop.**

I. Introduction

THIS PAPER describes a self-calibration concept applied to an integrated frequency synthesizer. As in most other ICs that are mixed-signal in nature, integrated frequency synthesizers operate over a wide range of process and temperature variations, as well as a large range of input and output conditions. Often, one accepts a degraded noise performance, in exchange for ensuring operation over a larger range of operating conditions. The self-calibration concept allows for designing low-noise frequency synthesizers, while not compromising the frequency range over which the synthesizer can operate.

This concept is best understood when seen from the viewpoint of how noise is generated, accumulated, and filtered within a phase-locked loop (PLL). While it is common knowledge that a typical PLL acts as a low-pass filter for noise present on the input clock, it is less well articulated that a PLL is a high-pass filter for noise generated within the oscillator. Reviewing some basic theory allows an understanding of how the self-calibration concept can result in lower noise in frequency synthesizers. This is presented in Section II of this paper.

For noise, the most sensitive block in a frequency synthesizer is the oscillator, typically in the form of a voltage-controlled oscillator (VCO). The output frequency of an oscillator must typically cover a wide range of frequencies for a limited range of input control voltage, implying a high gain. In Section III, we introduce a digitally programmable VCO which allows us to cover a very wide range of output frequencies, while simultaneously keeping a very low control voltage to output frequency gain (oscillator gain).

The digital word required by our VCO is generated by the PLL during a self-calibration cycle. By running a digital algorithm, described in Section IV, as part of the standard frequency and phase-lock acquisition process, the output free-running center frequency of the oscillator can be adjusted to be very close to the desired PLL output frequency. This minimizes the frequency pulling required of the feedback loop, allowing for a very low input voltage to output frequency gain. The oscillator pull-range has to be adequate to cover the frequency quantization in the digitally controlled VCO, as well as the frequency variation of the oscillator with temperature and power-supply voltage. However, all process variations are compensated for by the self-calibration technique.

Section V of this paper presents the measurements of our prototype IC, at several operating frequencies, and in Section VI we offer some conclusions about the self-calibrating concept as applied to PLLs and frequency synthesizers.

II. Noise Transfer Functions in PLLs

A. Classical Analysis of a Closed-Loop PLL

The following sections review the classical frequency domain analysis of noise transfer functions in PLLs. This fundamental material is included for review in order to demonstrate how the self-calibration concept can be used to design lower noise PLLs. In the following discussions, we will refer to Fig. 1.

As shown in the figure, four distinct transfer functions may be developed, the first being the input-to-output jitter transfer function and the remaining three corresponding to the intermediate nodes where input noise sources may be modeled. While it is certainly possible to combine noise sources into equivalents, as in [8], we chose to consider three noise inputs to better illustrate the noise-related benefits of the self-calibration concept. In addition, to keep the mathematics simple, we neglect the parasitic capacitance shunting the loop filter to ground, and the parasitic pole(s) found in the VCO.

The closed-loop transfer function of Fig. 1 can be found as

$$H(s)=\frac{\Theta_o(s)}{\Theta_i(s)}=N\frac{\left(\frac{K_dK_o}{C}\right)(1+sRC)}{s^2+s\left(\frac{K_dK_o}{C}\right)RC+\frac{K_dK_o}{C}} \quad (1)$$

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W. B. Wilson and K. R. Lakshmikumar are with Lucent Technologies, Bell Laboratories, Allentown, PA 18103 USA.

U.-K. Moon is with Oregon State University, Corvallis, OR 97330 USA.

L. Dai is with the Department of Electrical Engineering, University of Minnesota, Minneapolis, MN 55455 USA.

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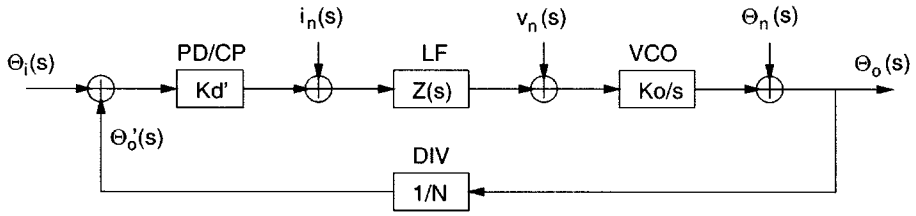

Fig. 1. Small-signal analysis block diagram.

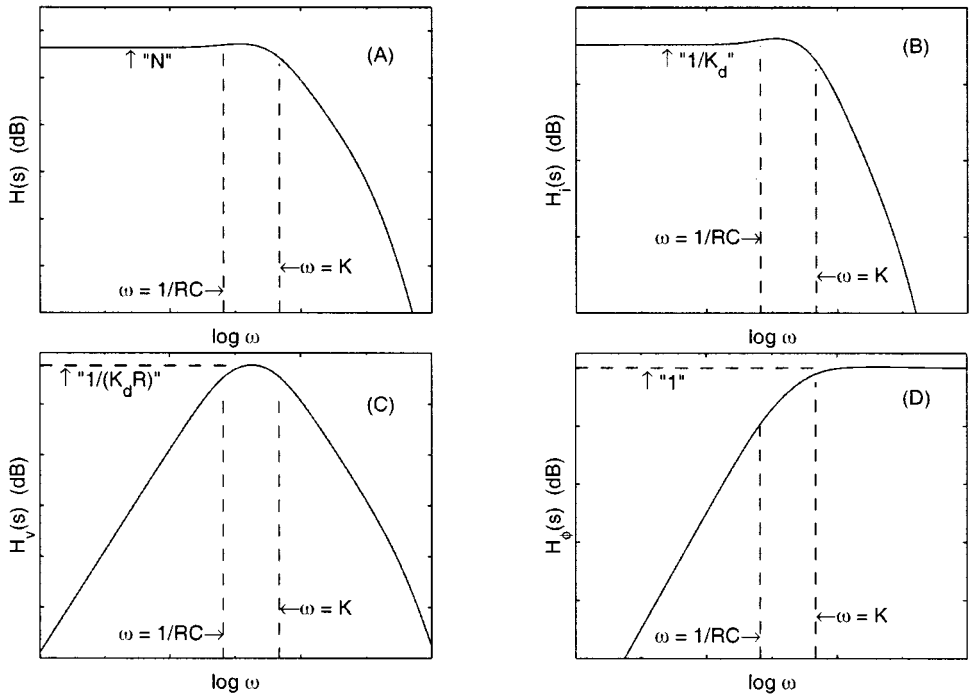

Fig. 2. Classical frequency-domain PLL noise analysis.

where loop-filter transfer function and combined effective phase-detector gain are

$$Z(s) = \frac{1 + sRC}{sC} \quad \text{and} \quad K_d = \frac{I_p d}{2\pi N} \quad \text{and} \quad K_d' = \frac{I_p d}{2\pi}$$

consistent with a series *RC* loop filter used in a typical charge-pump PLL [5] with charge-pump current I_p (d is a constant for a given system).

This can be compared to the classical two-pole system transfer function

$$H(s) = N\frac{2\zeta\omega_n s + \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{2}$$

where the N accounts for the desired frequency multiplication and $\omega_n = \sqrt{K_d K_o / C}$ and $\zeta = (R/2)\sqrt{K_d K_o C}$. This is shown graphically in Fig. 2(a) for a slightly overdamped system ($\zeta > 1$ with two closely separated real poles). For an overdamped system, the −3-dB bandwidth, $K = K_d K_o R$, is approximately the second pole of the transfer function $H(s)$.

B. Transfer Functions for Various Equivalent Noise Sources

The transfer functions from various input nodes shown in Fig. 1 may be derived to yield

$$H_i(s) = \frac{\Theta_o(s)}{i_n(s)} = \frac{\left(\frac{K_o}{C}\right)(1 + sRC)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{3}$$

$$H_v(s) = \frac{\Theta_o(s)}{v_n(s)} = \frac{sK_o}{s^2 + 2\zeta\omega_n s + \omega_n^2} \tag{4}$$

$$H_\theta(s) = \frac{\Theta_o(s)}{\Theta_n(s)} = \frac{s^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{5}$$

These transfer functions are plotted for closely separated poles in Fig. 2(b)–(d). (Note please, the plots incorporate a third pole within the PLL, commonly associated with the loop-filter ripple bypass capacitor.)

It is reasonable to assume that the equivalent noise sources at the loop filter voltage $v_n(s)$ and the charge pump current $i_n(s)$ are white and Gaussian. Practical causes of these noises sources might include the thermal noise in the current which is sampled to the output of the charge pump, as well as the thermal noise of the loop filter resistor. Also, any thermal noise sources in the

circuitry used to bias the ring oscillator can be scaled back to an equivalent noise voltage at the input to the oscillator. Also, equivalent to the noise source $v_n(s)$, noise sourced at the VCO output $\Theta_n(s)$ has power spectrum[1] proportional to $1/f^2$. The assumptions employed here particularly ignore the $1/f$ noise that is often a significant source of noise in CMOS PLLs. Each of these noise sources are then scaled by their respective transfer functions (magnitude squared), when referred to the output as power spectral density of the phase noise resulting from each particular noise source.

C. Discussion

When the noise power spectral density is multiplied by the power gain and integrated over frequency, we obtain the power of the output jitter. If we assume that both i_n and v_n are white Gaussian noise and the VCO phase noise $\overline{\theta_n^2}/\Delta f = K_\theta/f^2$, the power of the output phase noise due to i_n, v_n, and θ_n is given by

$$\phi_{n,i}^2 = \frac{1}{2\pi}\int_0^\infty \frac{\overline{i_n^2}}{\Delta f}\,|H_i(j\omega)|^2\,d\omega = \frac{(\overline{i_n^2}/\Delta f)\omega_n}{2\pi K_d^2}\Gamma_i(\zeta) \tag{6}$$

$$\phi_{n,v}^2 = \frac{1}{2\pi}\int_0^\infty \frac{\overline{v_n^2}}{\Delta f}\,|H_v(j\omega)|^2\,d\omega = \frac{(\overline{v_n^2}/\Delta f)K_o^2}{2\pi\omega_n}\Gamma_i(\zeta) \tag{7}$$

$$\phi_{n,\theta}^2 = \frac{1}{2\pi}\int_0^\infty \frac{\overline{\theta_n^2}}{\Delta f}\,|H_\theta(j\omega)|^2\,d\omega = \frac{2\pi K_\theta}{\omega_n}\Gamma_\theta(\zeta) \tag{8}$$

where Γ_i, Γ_v, and Γ_θ are only dimensionless functions of ζ.

One of the most well-known techniques to reduce the PLL output phase noise is to increase the loop bandwidth ω_n by increasing the value of K_d. It can be seen from (6) to (8) that when ω_n and K_d are increased by the same factor, the phase noise transferred from i_n, v_n, and θ_n is reduced. As seen from (1), the jitter present at the input clock is low-pass filtered. This indicates that more phase noise from the input clock will transfer to the output with larger loop bandwidth. Fortunately, however, it does not cause a problem when the input is a clean clock source with negligible phase noise.

On the other hand, the -3-dB loop bandwidth cannot be increased indefinitely. The maximum loop bandwidth is restricted by the update rate of the phase detector. In general, it has approximately to be less than $1/10$ of the phase detector update rate to avoid instability. The loop bandwidth has to be further limited when there is significant phase noise in the input clock that needs to be attenuated. In that case, an optimal loop bandwidth is desirable to minimize the total output phase noise. Once the -3-dB loop bandwidth is fixed in the design, any increase in K_d has to be balanced with a reduction in K_o.

Reducing K_o makes the VCO less sensitive to the noise at the control port. However, it may not affect the amount of noise generated within the oscillator, nor does it necessarily improve the power supply and substrate noise rejection internal to the VCO. Therefore, a low-noise oscillator with good power supply and substrate noise rejection is a prerequisite to low-noise PLL design. Commonly, voltage regulators and separate supply rails with off-chip filtering are used, and such considerations are beyond the scope of this paper. In the designs where a large frequency tuning range is required for the PLL, the VCO has to operate with a wide range of bias current. In general, a low bias current causes degradation of the oscillator phase noise performance. This makes the optimal design of the PLL loop parameters more crucial. In our design, the PLL loop bandwidth is maximized for all operating frequencies. Hence, the phase noise due to sources internal of the PLL is reduced to the largest extent.

Finally, it should be noted that reducing K_o in combination with increasing loop filter component R (keeping constant bandwidth) will also reduce the phase modulation of any systematic ripple present on the loop filter voltage due to sources such as power supply noise. However, the phase modulation from the ripple in the loop filter voltage caused by static phase offset [8] is not affected by this K_o and R combination for constant bandwidth. This assumes that the dominant causes of static phase offset can be modeled as a leakage current at the output of the charge pump. Well-designed phase/frequency detectors introduce little static phase offset, and for a well-designed charge pump, the up and down currents match extremely well compared to displacement currents resulting from charging and discharging the parasitic and gate capacitances as the up and down currents are turned on and off. These displacement currents deliver a fixed amount of charge per cycle of the reference clock to the loop filter, and may be modeled as a leakage current. Thus, only increasing K_d, combined with lowering K_o for constant loop bandwidth, will reduce the phase modulation resulting from static phase offset.

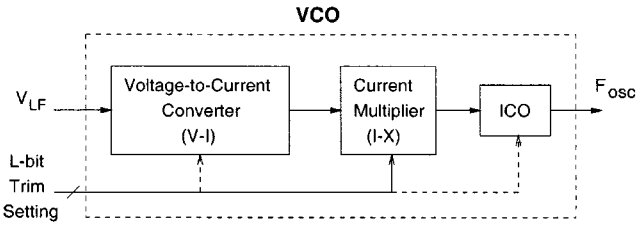

Fig. 3. Digitally programmable VCO.

III. Design of Oscillator and PLL

This section describes a CMOS ring oscillator which has a large frequency range and generates very little phase noise. It also describes in general terms the rest of the components comprising the PLL core.

A. Oscillator Design

The VCO is made up of a voltage-to-current converter (*V–I*), current multiplier (IX), and current-controlled oscillator (ICO), as shown in Fig. 3. The VCOs L-bit programmability is contained within the current multiplier, which equivalently operates as a weighted current mirror, and as a pedestal current (dc) within the *V–I* converter. The programmability may be distributed over all

[1]More detailed discussions elsewhere [2], [3] show that the output-referred phase noise $\Theta_n(s)$ is Lorentzian.

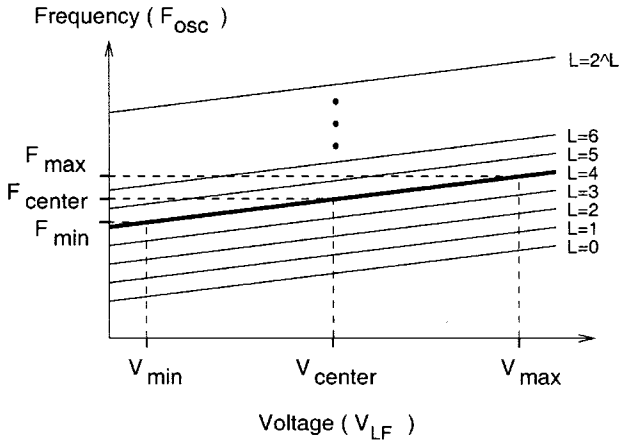

Fig. 4. 2^L operating modes of VCO.

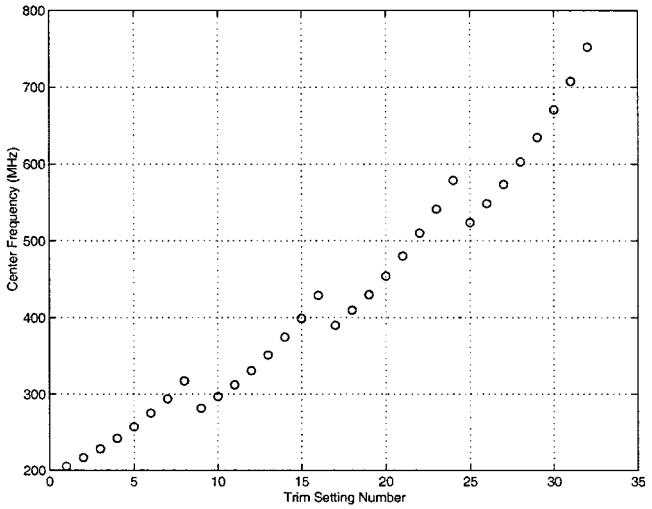

Fig. 5. Measured VCO frequency versus L-bit control (input to VCO at nominal/mid-level).

three blocks, and extending the programmability to the ICO may be considered, especially if an inherently smaller tuning-range structure is used for the oscillator, as in [11]. Previous efforts [1], [10] used either a fixed control word or a dual-loop structure to achieve similarly programmable ring oscillators at much lower frequencies. Our structure requires no externally provided control word, and we tune the VCO directly to avoid the interference resulting from a second oscillator running at a slightly offset frequency from the desired one, as in [10].

The VCO as a whole can simply be viewed as a block which has 2^L operating modes. This is illustrated in Fig. 4. Depending on the process variation and desired operating frequency, one of the operating modes may be chosen by the L-bit digital control. When an appropriate operating mode is selected for the normal operation, the net result is the input control voltage to output frequency transfer function small enough for low sensitivity to noise, and large enough to compensate for temperature and power supply variations that are relatively small in comparison to process variation, as well as the quantization error between adjacent modes.

Note that the transfer function need not be linear nor monotonic. As long as the magnitude of the frequency steps controlled by the L-bits are relatively small in comparison to the continuously tunable range of frequencies from the loop-filter control voltage, the calibration algorithm, described in the following section, will find the desired operating mode, and the oscillator will have enough pull-range to acquire phase lock. Shown in Fig. 5 is the measured transfer function of the overall VCO with the input of the *V–I* converter set to mid-level yielding the oscillator center frequency for that trim setting. Observe that the resulting output frequency of the VCO with respect to the L-bit ($L = 5$ in this implementation) control word is neither linear nor monotonic. The available set of discrete frequencies are sufficient for our needs and intended by design.

In our implementation, a wide-frequency-range ICO is used [7]. This was chosen because of some nice tunability and sensitivity behaviors of the ICO. Shown in Fig. 6 are the details of the circuit. As described in [7], the diode-tied MOSFET in parallel with the current source provides a nice symmetrical load for the differential pair devices in the delay cells. This symmetric load maintains a relatively steady signal swing that has reduced sensitivity to process and temperature variations and a wide range of operating frequencies.

B. PLL Core

As seen in the block diagram in Fig. 9, we have implemented a conventional charge-pump PLL in a frequency synthesizer configuration. The input divider is 3 bits, the feedback divider is 8 bits, and there is a $\div 2$ prescalar (not shown). Synchronous custom dividers were implemented using a polycell approach to minimize noise contributions which are described in [4]. The phase-frequency detector (PFD) is a conventional type-IV, with a keep-alive circuit [9] to linearize the response in the dead zone.

The schematic of the charge pump is shown in Fig. 7. Current sources $I_{\rm UP}$ and $I_{\rm DOWN}$ are switched in response to the output of the PFD. Transistors M1 and M2 are cascode devices to minimize any feed-through on to the loop filter. The output voltage can swing to about 2 $V_{\rm sat}$ from either supply rail. This large swing helps again to reduce the K_o of the oscillator.

A single-ended on-chip loop filter is used to avoid noise coupling inherent in bringing the loop filter voltage off-chip, and to eliminate the need for any components external to our macrocell.

In order to reduce the sensitivity of the loop gain to resistance variations, the *V–I* converter is implemented incorporating a resistor that is matched to the resistor that is used in the loop filter [6]. The schematic is shown in Fig. 8. The n-channel differential pair (M1–M2) has a linear range for voltages ranging from $V_{gs} + V_{\rm sat}$ to V_{dd}. Similarly, the p-channel pair (M3–M4) has a range that includes ground. One side of each of the differential pairs is connected to a reference voltage VRF which is typically equal to half the supply voltage. The other transistor's gate is connected to VRF or the loop filter voltage VLF, based on the output of the comparator. For example, if VLF is larger than VRF, then VLF is connected to M1, and both the transistors in the p-channel pair are connected to VRF. Thus the n-channel pair provides a current proportional to VLF while the p-channel pair puts out a constant current. The roles of the p- and n-channel pairs reverse for VLF less than VRF. The

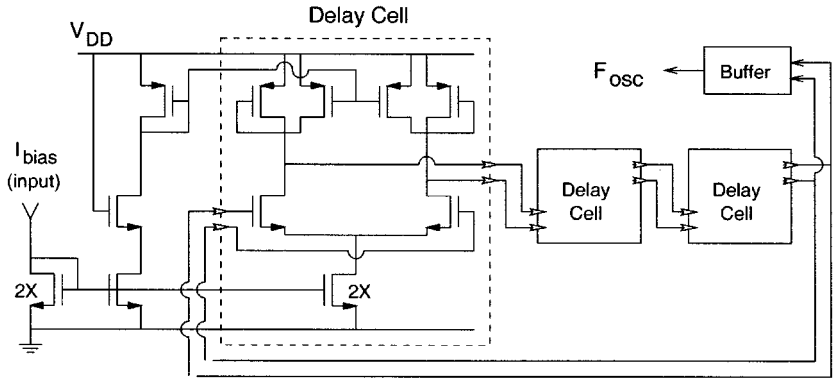

Fig. 6. Current-controlled oscillator.

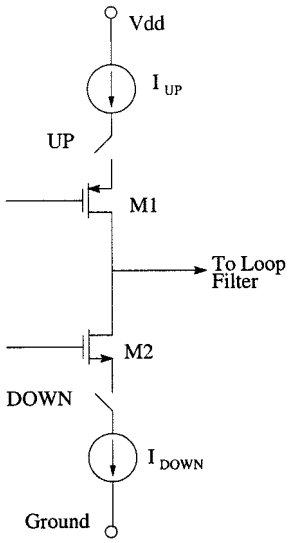

Fig. 7. Charge pump.

current from the two pairs are finally added and applied to the ICO. Any mismatch or offset in the pairs can cause a discontinuity in the transfer characteristic. This could result in excessive jitter. Therefore, a small amount of hysteresis is introduced into the comparator. This will insure that the output current is a continuous function of the voltage for a sufficient region around any lock-in voltage on the loop filter.

IV. Self-Calibration Algorithm and Implementation

As described, Fig. 9 shows the block diagram of the charge-pump PLL. This figure contains an extra set of blocks in parallel starting from the input of the PFD. The output of this upper parallel path is an L-bit word controlling the VCO. The lower path is just a portion of the ordinary PLL with additional switches SW1 and SW2. As described in the figure, the only programmable block is the VCO. The switches SW1 and SW2 are used to break the normal operating loop of the PLL when calibration takes place.

At power-up, a power-up detect circuit (not shown) will send a reset/calibrate signal to this PLL block. The upper parallel path only responds to this signal and starts the calibration with L-bits initialized to zero, and stops when optimum setting (of the L-bit word) is reached. If self-calibration is to be repeated after the IC is powered up, if for example, the values of the dividers M and N are changed, then the reset/calibrate signal is also asserted. During calibration, SW2 is closed and SW1 is opened in order to place a fixed reference voltage (mid-level) to the input of the VCO. According to the L-bit control to the VCO, the open-loop VCO will produce a free-running center frequency at the output, and corresponding divided frequency at node V at the output of the feedback divider (by N). Given a desired input reference frequency and the input divider (by M), the frequency at node R reflects what we would like the frequency at node V to match. By stepping through the values of L-bit control word to the VCO, and measuring whether the frequency at node V is greater or less than frequency at node R, a desired optimum operating mode of the VCO may be selected.

In this prototype IC, the upper calibration path is simply a set of two counters put to a race side by side. If the node R counts faster and finishes the race before the node V, the L-bit control is incremented to speed up the VCO. Naturally, the counter length determines the limited accuracy of the frequency comparison. The initial phase offset between R and V will have a minimal influence on the accuracy of the comparison provided that the length of the counters is long enough. Once the node V wins the race, the L-bits are frozen for the normal operation of the PLL and the calibration circuit is disabled until the reset/calibrate is reactivated by power-up or the alternate single-bit digital control. The complete self-calibration algorithm is illustrated in the flowchart of Fig. 10.

A modified version of the algorithm also exists. The same counters for R and V are used. However, once the node V wins the race, a comparison will be made between the VCO center frequency with the current control word setting and the previous setting. A decision will be made so that the center frequency closer to the desired value is chosen. We have successfully implemented this modified version in other PLLs.

The calibration algorithm described above employs a *sequential* search, and the frequency difference between nodes V and R are *truncated* to a single bit (high or low). It is not difficult to implement a *binary* search to speed up the total calibration time. Also, a wide variety of circuits to perform frequency comparison exist, including the PFD and charge pump inside the main PLL loop, in addition to the frequency detector and digital accumulator shown in the figure. We found the simplified

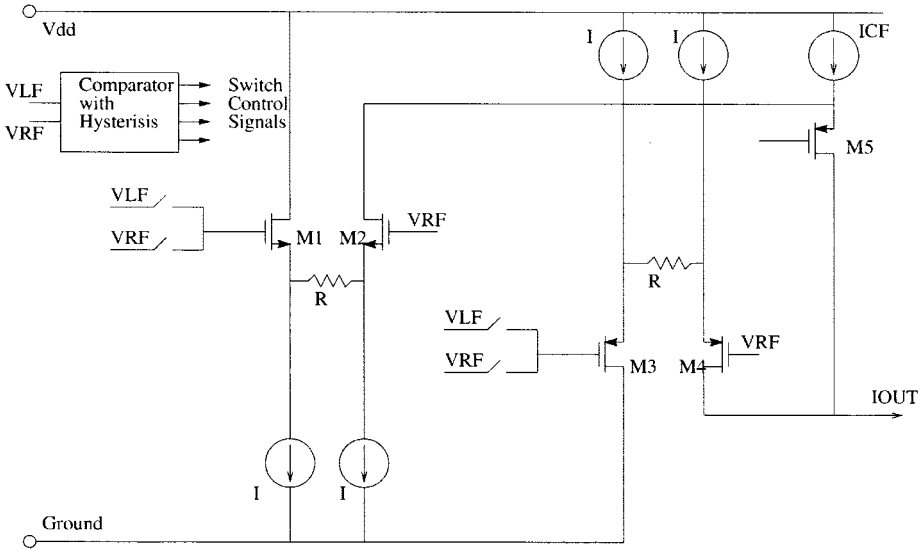

Fig. 8. *V–I* converter.

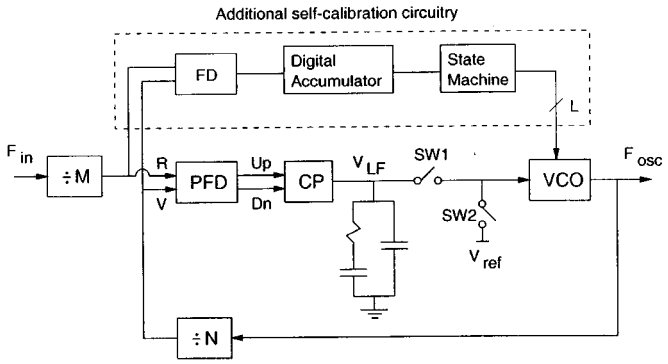

Fig. 9. Self-calibrating PLL.

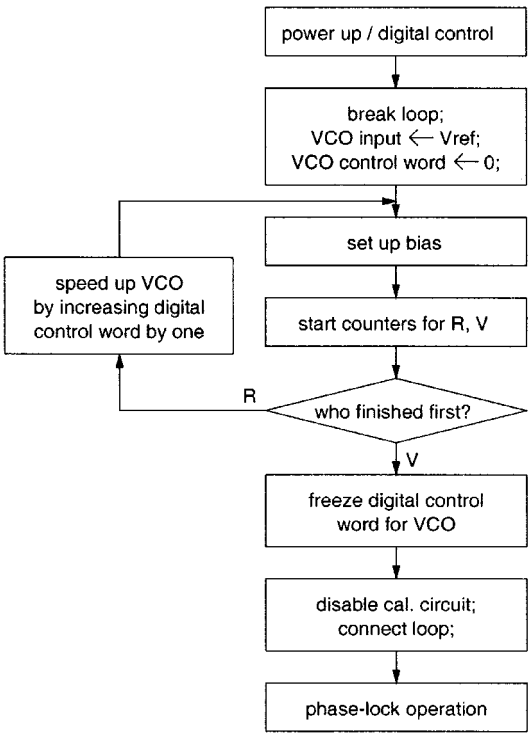

Fig. 10. Flowchart for self-calibration algorithm.

algorithm to be more than sufficient in accuracy and speed for the targeted applications in mind, without adding any performance-degrading load to the sensitive analog loop filter.

V. Measurement Results

The die photo of the prototype IC is shown in Fig. 11. The main PLL structure is in the middle of the die, composed of *V–I*, the PFD/charge pump and the loop filter. The ring oscillator is located in the upper left, and the autotrim logic and high-speed dividers are in the upper right corner. In the lower portion are low-noise voltage and bias current generators.

Measurements show that this frequency synthesizer operates from 80 MHz to 1 GHz. The PLL 3-dB loop bandwidth was measured to be 420 kHz with a 4.86-MHz phase-frequency update rate and 311-MHz operating frequency.

Shown in Fig. 12 is the jitter measurement for 560-MHz operating frequency with phase-frequency update rate of 40 MHz. The plot displays 26.8-ps rms of *absolute*[2] jitter (from the reference input clock to the oscillator output clock). At the operating frequency of 480 MHz, with phase-frequency update rate of 40 MHz, the measured absolute jitter rms is less than 20 ps and the commonly quoted self-triggered measurement of *period* jitter is less than 4-ps rms (deduced from a longer time-delay measurement).

Next, multiple absolute jitter measurements were taken for operating frequencies of ∼220, ∼330, and ∼440 MHz, while varying phase-frequency update rate (this is proportional to loop bandwidth). The control word from the self-calibration logic was held constant for all measurements at each particular output frequency to hold K_o constant. The inversely proportional absolute jitter relationship to the square root of loop bandwidth

[2]Approximate *absolute* jitter is obtained in measurement by triggering off the low-jitter crystal oscillator reference input to PLL, and collecting a histogram of the PLL output clock edges. The true absolute jitter is bound (always smaller) by this measurement.

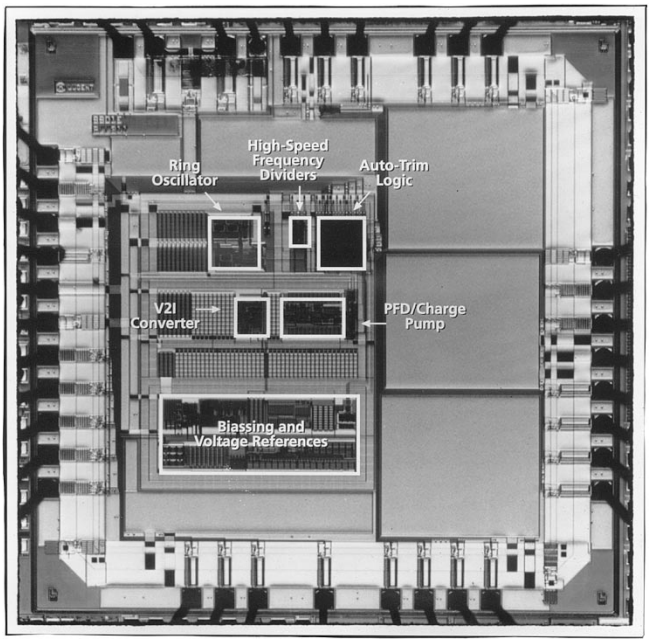

Fig. 11. Die photograph of the prototype IC.

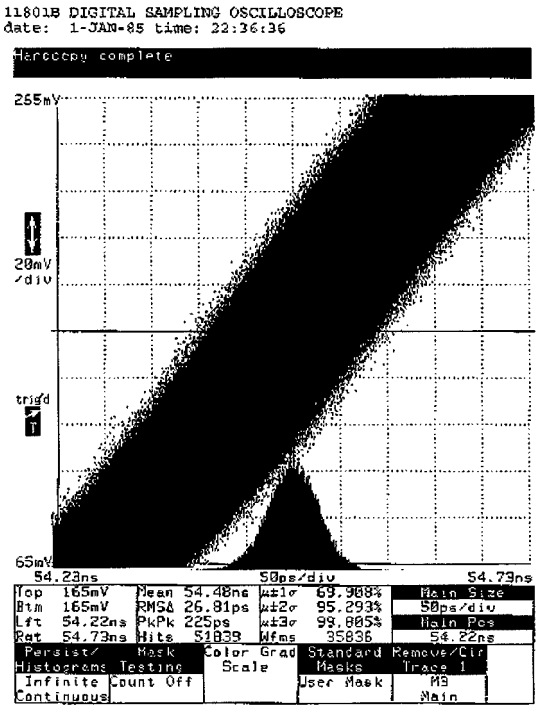

Fig. 12. Measured rms jitter at $f_{osc} = 560$ MHz.

is clearly observed in Fig. 13. The dashed line in the figure is the ideal curve for rms jitter that is inversely proportional to the square root of loop bandwidth ($\propto 1/\sqrt{\text{bandwidth}}$).

Our final jitter measurements were made by increasing the value of the charge pump current and the adjusting oscillator gain to keep the loop bandwidth contstant. The charge pump current was increased by a factor of 2 by increasing the bias current generated in our biassing section using an integrated trimming circuit. (A copy of the bias current is measurable off-chip.) This bias current feeds the oscillator as well as

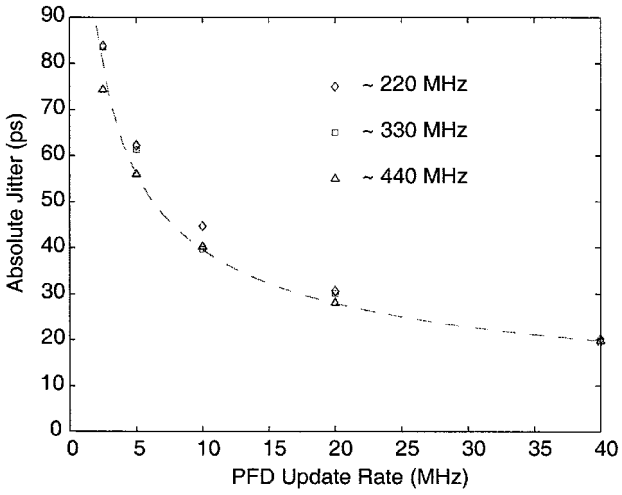

Fig. 13. Measured absolute jitter versus phase-frequency update rate (f_{PFD}).

TABLE I
MEASURED JITTER RESULTS

Measurement	Value	Conditions
Absolute Jitter	32 ps *rms*	nominal $I_p K_o$, Fin = 40 MHz, Fosc = 720 MHz
Absolute Jitter	26.82 ps *rms*	nominal $I_p K_o$, Fin = 40 MHz, Fosc = 560 MHz
Absolute Jitter	$<$ 20.0 ps *rms*	nominal $I_p K_o$, Fin = 40 MHz, Fosc = 480 MHz
Period Jitter	$<$ 4 ps *rms*	nominal $I_p K_o$, Fin = 40 MHz, Fosc = 480 MHz
Absolute Jitter	23.5 ps *rms*	low I_p, high K_o, Fin = 40 MHz, Fosc = 240 MHz
Absolute Jitter	16.0 ps *rms*	high I_p, low K_o, Fin = 40 MHz, Fosc = 240 MHz

the charge pump. Referring to Fig. 3, the pedestal current generated in the *V–I* converter has now been doubled. Holding the control bits driving the *V–I* converter constant, we manually adjusted the remaining control bits to exactly halve the gain of the current multiplier. This restores the original amount of current into the ICO maintaining the same oscillator frequency operating point and small-signal oscillator gain. Please note that the gain of the *V–I* is nominally unaffected by the value of the pedestal current, which is set by the current source ICF (center frequency) in Fig. 8. Thus, the only change to the overall VCO gain is the gain of the current multiplier, which has been exactly halved. This combines with the doubling of the charge pump current to leave our PLL bandwidth unchanged. The measured absolute jitter was reduced from 23.5-ps rms for the low-charge-pump-current high-oscillator-gain case to 16.0-ps rms for the high-charge-pump-current low-oscillator-gain

case.[3] The input frequency was 40 MHz and the oscillator frequency was 240 MHz. This 32% reduction in absolute jitter demonstrates that reducing K_o and increasing I_p to maintain a constant loop bandwidth lowers the absolute jitter in our PLL.

Our measured jitter results are summarized in Table I.

VI. Conclusion

A self-calibration technique that may be used in any PLL structure has been demonstrated in the prototype IC fabricated in a 0.35-μm 3-V digital CMOS technology. The automatic self-calibration of the VCO initiated at the device power-up allows a robust and optimized PLL design which is able to overcome a significant amount of process variation. Additionally, a self-calibrating VCO can have a lower value of K_o than would otherwise be allowed, and this can result in lower jitter in applications where the PLL loop bandwidth is either fixed or maximized. If the PLL jitter is dominated by internal device noise, as opposed to power-supply noise, the amount of jitter reduction from self-calibration of the VCO is significant. We have chosen a simpler form of self-calibration algorithm and a better-known VCO structure in this prototype IC, but this self-calibrating and reconfigurable PLL concept is adaptable to all PLLs or tunable oscillator structures.

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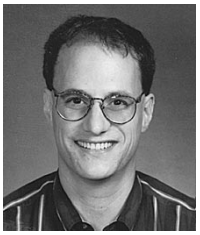

William B. Wilson (S'83–M'86) received the B.S.E.E. degree from Syracuse University, Syracuse, NY, in 1983, and the M.S.E.E. degree from Duke University, Raleigh, NC, in 1985.

In 1986 he became an Analog Product Engineer with Digital Equipment Corporation, Hudson, MA, and in 1988 he joined Bell Laboratories, Reading, PA, as a Member of Technical Staff engaged in analog/mixed-signal circuit design for 10Base-T, 100Base-T, and other local area network technologies. In 1999 he was appointed as a Distinguished Member of Technical Staff, and is currently involved in designing high-frequency low-noise PLLs, as well as CODECs for wire-based communications systems at Bell Laboratories, Allentown, PA.

Mr. Wilson is a member of Eta Kappa Nu and Tau Beta Pi.

Un-Ku Moon (S'92–M'94–SM'99) received the B.S. degree from the University of Washington, Seattle, the M.Eng. degree from Cornell University, Ithaca, NY, and the Ph.D. degree from the University of Illinois, Urbana-Champaign, all in electrical engineering, in 1987, 1989, and 1994, respectively.

From February, 1988, to August, 1989, he was a Member of Technical Staff at AT&T Bell Laboratories, Reading, PA. During his stay at the University of Illinois, he taught a microelectronics course from August, 1992, to December, 1993. From February, 1994, to January, 1998, he was a Member of Technical Staff at Lucent Technologies, Bell Laboratories, Allentown, PA. Since January, 1998, he has been with Oregon State University, Corvallis. His interest has been in the area of analog and mixed analog-digital integrated circuits. His past works incude highly linear and tunable continuous-time filters, telecommunication circuits including timing recovery and analog-to-digital converters, and switched-capacitor circuits.

Kadaba R. Lakshmikumar (S'82–M'86) received the B.E. and M.E. degrees in electrical communication engineering from the Indian Institute of Science, Bangalore, India, in 1974 and 1976, respectively, and the Ph.D. degree in electrical engineering from Carleton University, Ottawa, ON, Canada, in 1985.

From 1976 to 1981, he worked at Bharat Electronics Limited, India, as a designer of analog integrated circuits. He joined Bell Laboratories, Murray Hill, NJ, in 1985. In 1993 he was appointed as a Distinguished Member of Technical Staff. He is currently a Technical Manager leading a team engaged in the design of gigabit-rate transceivers. His other interests include data converters and communication systems design.

Dr. Lakshmikumar received the Canadian Commonwealth Scholarship in 1981.

Liang Dai (S'96) was born in Beijing, China, in 1971. He received the B.S. degree from Beijing University, Beijing, in 1995 and the M.S.E.E. degree from the University of Minnesota, Minneapolis, in 1998. He is currently working toward the Ph.D. degree in electrical engineering at the University of Minnesota.

He worked as a summer intern at Lucent Technologies, Allentown, PA, in 1998 and 1999. His research interest is in analog and RF IC design for communications systems.